Amstrad

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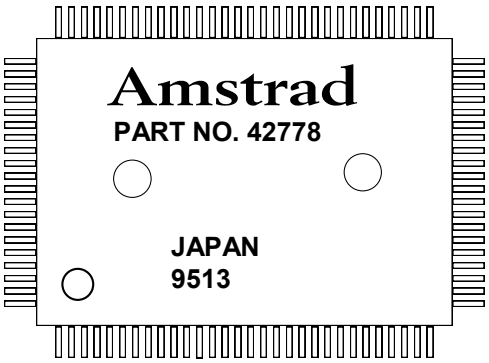


"Anne"

ASIC Specification

Version	1.2
Date	27 July, 2019
Written by	SD Gane

Contents

1. Related Documents

IBM "Personal System/2 Technical Reference", Keyboard Section

Winbond "W83787 Super-I/O Data Sheet"

Zilog "Z80 Microprocessor Family User's Manual"

Zilog "Z80 Microprocessor Family Data Book"

2. Introduction

This document defines and describes the Amstrad "Anne" ASIC. This ASIC is intended to be used in conjunction with a PC Super-IO chip to build "Anne", a replacement for the ageing PcW range.

The ASIC allows various flavours of Annes to be built, with different memory options and different display options. The ASIC provides a colour option, but it is not anticipated that it will be used in the near future if ever.

3. Summary

3.1. Clock Generation

The ASIC has a 48MHz clock input (CK48), from which it derives the following clock signals:

- A 24MHz pixel rate clock for the display subsystem. This is provided at the PCK output, and is intended to be used by the Super-IO chip.
- A 16MHz clock for the Z-80. This is not normally available outside the ASIC.

Additionally, there is a 32.768kHz crystal oscillator (pins XT1 and XT2) for the real time clock.

3.2. Processor

The ASIC contains an NEC NZ70008H macrocell, which is essentially a Z-80, running at a clock frequency of 16MHz. It is allowed to run at full speed, except that wait states are added to memory cycles as described under "memory" below, to allow the use of available low cost semiconductor memory devices. Also, extra wait states are added to DRAM cycles which collide with accesses to the memory by the display controller or with refresh cycles. No wait states are added to I/O or Interrupt Acknowledge cycles except those automatically added by the Z-80.

3.3. Memory

The Z-80's 64K logical address space is expanded to 4MB of physical address space by a paged memory mapping system. The logical address space is divided into four 16K regions, into each of which any of the 256 pages of physical memory may be mapped .

The upper half of the physical memory space (A21 = 1) is allocated to up to 2MByte of DRAM. Physically, the memory can be either a single 512K x 8, or two or four 1M x 4, or a single 2M x 8, to provide 0.5, 1 or 2MByte of RAM.

The lower half of the physical memory space (A21 = 0) is allocated to non-multiplexed, asynchronous (i.e. Flash, ROM, SRAM, etc.) memory. Chip select signals are provided for one, two or three memory sites. The first 64K of this space is write protected. (WR is not generated when A20…A16 are all low, unless IORQ is active. This means that WR is not generated for the first 64K of DRAM space either, but DRAM writes still work because MWE is generated.)

3.3.1. Memory Timing

For the DRAM, the memory timings are fixed in the ASIC, such that one wait state is added to M1 cycles only. (Additional wait states occur if accesses are coincident with memory accesses by the display controller or with refresh cycles.) 70ns DRAM devices are required.

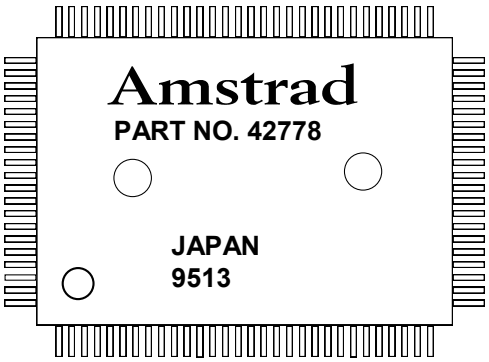
For the flash/ROM memory, two sets of jumpers are provided (for A20 = 0 and A20 = 1 respectively), to select between:

- One wait state on M1 cycles only, for 90ns access time memories (96ns limit)
- One wait state on all cycles, for 120ns memories (127ns limit)
- Two wait states on M1 cycles, one on others, for 150ns memories (158ns limit)
- Two wait states on all cycles, for 180ns memories (190ns limit)

3.4. The Super-I/O chip

The ASIC interfaces almost gluelessly to a 'Super-IO' chip (as used on an IBM compatible PC-AT), which provides most of the general purpose I/O devices. Description of the facilities provided are outside the scope of this document, but typically include:

- Floppy disc controller.
- Two serial communications ports.
- Bi-directional, parallel printer port.
- IDE hard disk drive interface.



3.5. Technology

The Anne ASIC is built using NEC's CB-C7 FT, 0.8µm CMOS, triple layer metal, cell-based technology. An NZ70008H macrocell is built using full-custom technology, and the remaining silicon area is filled with a "sea" of transistors which are connected together by custom metal layers, much like a modern gate array.

Anne uses a C37 master, providing approximately 85,000 grids (NEC's unit of silicon area), of which the NZ70008H macrocell uses a little over 40,000, leaving around 45,000 grids (equivalent to around 45000 MOS transistors) for custom logic. Almost 24,000 grids are used for custom logic, yielding a utilisation factor of 54%, which is quite low for triple-layer metal.

The Anne ASIC is packaged in a 100 pin, 20 x 14mm rectangular Plastic Quad Flat package (PQFP) with 0.65mm lead pitch, and all 100 pins are used. The full NEC part number is uPD96123GF-002-3BA.

3.6. Device Marking

The ASIC is marked with the following information:

← The Amstrad logo
← The Amstrad part number, 42778

← The Country of Origin
← The Date and Batch Code

4. Detailed Description

4.1. Memory Interface

The ASIC contains four read-write memory mapping registers, one for each 16K bank of logical memory space. Each register defines which of 256 possible memory pages is to be used for read/write access. At reset, the register for logical addresses 0000h-3FFFh is cleared, so that page zero is mapped in. The others are undefined.

When accessing memory, the CPU supplies address bits A0-A13 directly, and the appropriate mapping register supplies the upper address lines, UA14-UA21. Thus the address space is extended to 2^{22} bytes, or 4MB. UA21 is not available outside the ASIC, but is used internally to select between DRAM and ROM (etc.).

For the ROM area (A21 = 0) the ASIC can provide address lines UA14-UA21 and a single chip select (RCS), or the upper two address lines can be traded for additional chip select signals, to support one 2MB, two 1MB, or three 512KB devices. This is controlled by J5 and J6:

J5	J6	Mode	UA20	UA19	Chip select activated
OUT	IN	1-chip	X	X	RCS / RCS0
OUT	OUT	2-chip	0	X	RCS / RCS0
			1	X	UA20 / RCS1
IN	OUT	3-chip	0	0	RCS / RCS0
			0	1	UA19 / RCS2
			1	0	UA20 / RCS1
			1	1	Illegal - Both RCS1 and RCS2

For the DRAM area, the ASIC provides a single RAS line, two CAS lines and ten multiplexed address lines MA0-MA9, or one of the CAS lines can be replaced by an additional MA line by fitting jumper J7.

J7	Mode	UA20	CAS0 function	CAS1 function
IN	1 bank	X	CAS	MA10
OUT	2 banks	0	CAS	Not Selected
		1	Not Selected	CAS

Without J7 fitted, 4M DRAMS organised as 512K x 8 or as 1M x 4 can be used, or (with J7 fitted) 16M DRAMS organised as 2M x 8 and with 2K refresh cycles can be used. 4K refresh parts are unsuitable because they require 12 row address lines. The DRAM address multiplex is configured as follows

Pin	**MA10**	**MA9**	**MA8**	**MA7**	**MA6**	**MA5**	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**
Row	UA20	A9	UA18	UA17	UA16	UA15	UA14	A13	A12	A11	A10
Col	UA20	UA19	A8	A7	A6	A5	A4	A3	A2	A1	A0

4.2. Display Controller

The Display Controller provides a pixel-based display, similar to the VGA display on an IBM PC, with a resolution of 480 lines of 640 monochrome pixels. A system of indirection pointers (one for each scan line) allows rapid rolling and scrolling of the display, and also program the colour mode for each line. Any line can be in one of three modes: 640 dots and 2 colours, 320 dots and 4 colours, or 160 dots and 16 colours. The display controller fetches pixel information from DRAM, and also performs DRAM refresh. The data rate is 24 MBit/s regardless of the display mode.

A jumper (J4) must be fitted to allow RGB video to get out of the ASIC. Without J4, only the Green video output is available.

4.2.1. VDU Screen Memory

The display controller can access memory in the first 256K bytes of RAM, of which it uses up to 37.5K bytes as screen refresh memory. A pointer table starting at a fixed location in RAM holds the start addresses for each of the 480 scan lines, which in turn consist of 80 consecutive bytes.

For each scan line, the byte indexed by the scan line pointer table is displayed at the leftmost position on the screen. The next 79 subsequent bytes provide the information for the scan line, from left to right across the screen. The format of the data within a byte depends on the colour mode selected:

4.2.1.1. Mode 0 (Monochrome or 2-colour mode)

In this mode, the eight bits in a byte represent eight pixels on the screen, such that a '1' selects colour 1 and a '0' selects colour 0, and D7 is the leftmost pixel.

4.2.1.2. Mode 1 (4-colour mode)

In this mode, the four pairs of bits in a byte represent four pixels on the screen, and select colours 0 to 3 according to the binary value of the bit pair. D7 and D6 define the leftmost pixel.

4.2.1.3. Mode 2 (16-colour mode)

In this mode, the two nibbles in a byte represent two pixels on the screen, and select colours 0 to 15 according to the binary value of the nibble. D7 - D4 define the leftmost pixel.

4.2.2. Scan Line Pointer Table

The scan line pointer table occupies 960 bytes starting at physical address 20FC00h (i.e. an offset of 3C00h into page 3). It holds the start addresses for each of the 80 byte scan lines. This allows the 37.5K screen data to be positioned within the 47K contiguous block made up by pages 1 and 2 and the remainder of 3, if so desired. The two high bits of the pointer into this table are readable via the keyboard status register, to give an indication of where on the screen the dispaly controller is scanning.

The table consists of 480 entries each of 2 bytes, interpreted by the display controller as follows:

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	A11	A10	A9	A8	A7	A6	A5	A4
1	M1	M0	A17	A16	A15	UA14	A13	A12

A17…A4 Define the position in RAM of the first of 80 consecutive bytes of pixel data to be used for one scan line. Note that A21 is always one (to select RAM) and that A20…A18 and A3…A0 are always zero. Only the bottom 16 bits of the address are incremented between fetches: thus a scan line can not cross a 64K byte boundary.

M1 and M0 define the colour mode:

M1	M0	Mode	Number of colours	Resolution
0	0	0	2	640
0	1	1	4	320
1	X	2	16	160

4.2.3. Video Control Register

This write only register enables, disables or inverts the video, and sets the border colour. It is undefined at reset, but this is unimportant because the 'float video' switch in the system control register is set, so that the video outputs are high impedance.

Writing a '1' to D7 switches the display to reverse video mode, in which each '1' pixel in mode 0 is displayed in colour 0, and each '0' pixel in mode 0 is displayed in colour 1. The border is displayed in colour 1, rather than the specific border colour. Writing a zero restores normal operation.

Writing a '1' to D6 enables display of video until a '0' is written to disable it. Blanking the screen in this way forces the whole display area and the border to be displayed in border colour. Note that blanking a reverse video display forces all pixels and the border to be in colour 1.

Bits D4…D0 define the border colour. For monochrome operation, this should normally be set to black.

This register is undefined at reset. Bit D5 is unused and has no effect.

4.2.4. Colour Palette

The ASIC contains 16, five bit, write only registers which define colours 0 to 15, in addition to the border colour described above. The palette registers are defined such that writing to I/O address ENh defines colour N. By providing three states for each of the VR, VG and VB ASIC outputs, 27 colours or grey scales are available. Without J4 fitted, only VR is active, so only 3 grey levels are available. The 27 colours are:

Number	Green	Red	Blue	Colour	Grey Value
00, 01 04, 05	Z	Z	Z	Light Grey	13
02, 03	0	Z	Z	Magenta	4
06, 07	1	Z	Z	Pastel Green	22
08	0	0	Z	Blue	1
09	0	0	0	Black	0
10	0	Z	1	Mauve	5
11	0	0	1	Bright Blue	2
12	0	Z	0	Red	3
13	0	1	0	Bright Red	6
14	0	1	Z	Purple	7
15	0	1	1	Bright Magenta	8
16	1	0	Z	Sea Green	19
17	1	0	0	Bright Green	18
18	1	Z	1	Pastel Cyan	23
19	1	0	1	Bright Cyan	20
20	1	Z	0	Lime Green	21
21	1	1	0	Bright Yellow	24
22	1	1	Z	Pastel Yellow	25
23	1	1	1	Bright White	26
24	Z	0	Z	Cyan	10
25	Z	0	0	Green	9
26	Z	Z	1	Pastel Blue	14
27	Z	0	1	Sky Blue	11
28	Z	Z	0	Yellow	12
29	Z	1	0	Orange	15
30	Z	1	Z	Pink	16
31	Z	1	1	Pastel Magenta	17

4.2.5. Horizontal Display Timing

The display is essentially a VGA, but modified to use a pixel rate of 24MHz rather than the usual 25.175MHz or thereabouts. The 24MHz pixel clock is divided by 16 to produce a 1.5MHz character clock. At each character clock rising edge, the video shift register is loaded with 16 bits of pixel data. Every fourth clock, the register is advanced four places. Multiplexers select which of the four leading bits are fed to the colour select logic, depending on the colour mode. Data is fetched from RAM when required for display. During blanking intervals, no data is fetched and the shift register is loaded with rubbish.

Each horizontal line consists of 50 periods of 1.5MHz, giving a line rate of exactly 30kHz. SYH (Horizontal sync) from the ASIC is driven low for 6 clocks, i.e. 4µs. A

CAS-before-RAS DRAM refresh occurs during the first of each pair of clocks during this time, such that there are three refresh cycles per line. This occurs for every line on the display.

During the 480 displayed lines, data is fetched for display. In the first clock after SYH finishes, the appropriate pointer table entry is fetched. In the second clock after SYH, no data is fetched, but the VDU data address generator is initialised. For the following 40 clocks, data is fetched from the DRAM. Each word is actually displayed during the clock period following that during which it is fetched. At the end of this are two cycles with no DRAM fetch. These processes takes a total of 50 clocks, giving the 30kHz line rate. The border is eight pixels (half a character clock) wide, at each end of the displayed data.

4.2.5.1. DRAM Arbitration

DRAM arbitration is controlled by the 1.5MHz character clock. In any period of this clock, the display system may require to read or refresh the DRAM. For the first half of the clock period (333ns or 5 1/3 CPU T-states) the display system politely requests the DRAM. If the CPU commences an IORQ cycle (IO access or Interrupt Acknowledge) or commences an MREQ cycle which does not require DRAM, then the display system will perform its DRAM access completely transparent to the CPU. During the second 333ns period, the display system demands DRAM access. As soon as the DRAM controller is idle (i.e. after completing any CPU cycle currently underway) the display system will perform its DRAM access. If the CPU then tries to access DRAM again, it will be put into a wait state until the DRAM controller is idle.

DRAM cycles are controlled by the 48MHz clock. 7, 8, and 9 clocks are required for CPU, refresh and VDU cycles respectively.

4.2.6. Vertical Display Timing

The vertical timing generator is clocked by the leading edge of SYH. Each frame consists of 525 lines at 30kHz, giving a frame rate of 57.14Hz. For 480 lines, pixel data is displayed. Eight scan lines either side of the data make up the border, leaving 29 lines (966.67µs) during which the display is blanked. For the duration of these 29 lines, the frame flyback bit in the system status register is set. SYV (Vertical sync) from the ASIC is driven low for 2 line periods, commencing 2 line periods into the blanking interval.

4.2.6.1. Display System Interrupts

The display system produces an interrupt at the leading edge of SYV, and at two other occasions per frame, so that there is an interrupt once every 175 lines or 5.83ms. A readable counter records up to 15 missed interrupts, so that software need not respond instantly. IRQ0 is active whenever the count is non-zero. The counter is automatically cleared on reading, and will not increment past 15. Hardware timing prevents a timer interrupt occurring simultaneously with a read of the counter. IRQ0 cannot be masked. The counter is set to one by the first M1 cycle after the ASIC is released from reset.

4.3. Real-Time Clock

The real-time clock incorporated in the ASIC maintains time by means of a 32kHz oscillator. To allow operation when power to everything except the ASIC is off, all ASIC outputs are either forced to a low state or a high impedance state whenever the Power On Reset (PORN) input is low. Of course, the RTC continues to count through reset. Provided all inputs are static and held at GND or VDD, the ASIC should use little enough power to maintain the time and date by way of a 3 Volt lithium battery. (Most ASIC pins have on-chip pull-down resistors to help in achieving this.)

The 32kHz oscillator is divided down to 1Hz by a 15-bit ripple counter, known as the prescaler. The upper eight bits of this are readable by the CPU, to give a count of 1/256 seconds. A series of counters then count seconds and minutes (0 - 59), hours (0 - 23), days (1 to 28, 29, 30 or 31 as appropriate), and months (1 - 12). Finally, the rollover of the month from 12 to 1 increments a seven-bit year counter. The two low bits of the year select the number of days in February, so that years divisible by four are leap years. This is correct between March 1900 and February 2099.

There is a one-bit control register for the RTC, writeable as bit D0 of the prescaler, and readable (inverted) as the RTC Invalid status bit. When a zero is written to the control bit, or the PS (power sense) pin is sensed low, the prescaler is held reset, which prevents the RTC from counting, and the RTC Invalid status bit (bit 7 of the year register) is set. The RTC must be stopped when setting the time. It should be remembered that, even when stopped, a change in a register value can cause an increment of the next register, because only the prescaler is held halted. Working from least significant to most significant when setting is usually sufficient, except near the end of a month. The RTC can only be restarted by writing a one to the control bit.

It is left to the CPU to calculate day of week, to ensure that the time has not changed during reading, and that correct values are set into the RTC registers.

4.4. System Control and Status Channels

The ASIC contains a write-only System Control register, and read only System Status and Jumper Status registers.

4.4.1. System Control Register

When this port is written, the four LS bits define an opcode. The four MS bits are ignored except for commands XFh. The opcodes are listed below. An asterisk after the opcode indicates the state at reset.

X0h	No effect
X1h	Generate immediate system reset (see note below)
X2h	Connect IRQ6 input to /NMI (disconnect from /INT)
X3h	Connect IRQ6 input to /INT (disconnect from /NMI)
X4h *	Disconnect IRQ6 input from both /INT and /NMI
X5h	Set Floppy Disk Controller terminal count
X6h *	Clear Floppy Disk Controller terminal count
X7h	Drive video output(s)
X8h *	Float video output(s)
X9h	No effect
XAh	No effect
XBh	Bleeper On - generate 3.75kHz tone
XCh *	Bleeper Off
XDh	No effect
XEh	No effect
XFh *	Set 4-bit output port to value X (All bits are zero at reset)

Command xFh causes the four MS bits D7…D4 to be written to the general purpose output port, so that they appear at pins PP3…PP0 respectively, which are intended for power supply control or any other feature. Note that when J4 is fitted PP3 and PP2 are unavailable, and are replaced by the VR and VB (Red. and Blue video) outputs respectively.

It is not recommended that the "X1" command is used, because the on-chip pull down resistors on the device pins UA14…UA20 and RCS are not strong enough to discharge any PCB track capacitance quickly enough, and the configuration links may not be read correctly. If this facility really is required, external pull-down resistors are required for any link which must read a zero state.

4.4.2. System Status Register and Interrupts

The main function of this register is to identify the source of interrupts. Each bit is set when the corresponding interrupt is active, e.g. bit 4 is set whenever IRQ4 is active. The CPU interrupt signal is active whenever any of the IRQ bits in this register is active. (For IRQ6, the "Connect IRQ6 input to INT" command must also have been issued.) The exception is bit 2, which indicates that frame flyback is active. This bit is true for 966.67µs, and ends 272µs before the monitor starts displaying pixel data at the top of the screen.

IRQ7, IRQ6, IRQ4 and IRQ3 are active when the ASIC pins of the same name are driven high. These are intended for connection to pins of the same name on a Super IO chip, such that they represent interrupts from the parallel port, floppy disk controller, and the serial IO channels respectively.

IRQ5 is active when the INT pin on the ASIC is driven low. This is intended to be driven from any other interrupting devices (such as an IDE disk drive) using a wired-AND connection.

IRQ1 and IRQ0 are generated on chip, by the keyboard interface and the display controller respectively.

4.4.3. Jumper Status Register

The bits in this register reflect the configuration jumpers, which are read at reset from the RCS and UA14…UA20 pins (see the pinout appendix).

J7 configures the ASIC pins CAS1/CAS and CAS0/MA10, as described under 'Memory Interface' above.

J6 and J5 configure the ASIC pins RCS/RCS0, UA20/RCS1, and UA19/RCS2, as described under 'Memory Interface' above. J5 and J6 must not both be fitted.

J4 configures the ASIC pins PP3/VR and PP2/VB as described under 'System Control Register' and 'Colour Palette' above.

J3 and J2 set the number of wait states for physical addresses 1XXXXh.
J1 and J0 set the number of wait states for physical addresses 0XXXXh.

J1 (J3)	J0 (J2)	Wait States
0	0	One wait state on M1 cycles only
0	1	One wait states on all cycles
1	0	Two wait states on M1 cycles, one on others
1	1	Two wait states on all cycles

4.5. Keyboard interface

The ASIC communicates with the keyboard via a bi-directional, synchronous, serial link, using the pins KDA and KCL. In normal operation, an interrupt (IRQ1) is

generated when a byte is received from the keyboard, and reading the byte from the keyboard data port clears the interrupt. Thus keyboard data can be read very easily. Writing to the keyboard is a little more tricky.

4.5.1. Keyboard shift register

There is an eleven bit register, eight bits of which (the data bits) can be read or written at I/O address F4h. Note that writing to the shift register sets the parity bit, start bit and stop bit to 0, 0 and 1 respectively ready for transmission. Reading the shift register clears the interrupt and busy status bits and resets the interface ready for reception.

4.5.2. Keyboard control/status register

This is a read-write register located at I/O address which provides access to the remaining three bits of the shift register (parity, start, stop) and various control functions.

Bit	Output Function	Input Function
7	Set Parity bit	Read Parity bit
6	No effect	Read Stop bit
5	No effect	Read Start bit
4	No effect	Read Busy status
3	No effect	VDU Pointer address bit 9
2	Reset Interface	VDU Pointer address bit 8
1	Force Keyboard Clock	
0	Transmit mode	

Bits 1 and 0 are true read/write bits, the others are not. For example, the Parity bit (as read via bit 7) is cleared by writing the shift register, and set by writing a '1' to bit 7.

4.5.3. Keyboard receive procedure

This is the process for data reception from the keyboard. The CPU's intervention is minimal. At reset, the keyboard clock and data will be high, which is the idle state.

- The keyboard senses the idle condition on the clock and data lines, and begins transmitting. The BUSY status register bit becomes set.
- The keyboard completes its transmission, which causes interrupt IRQ1 to be set.
- The CPU responds to the interrupt by simply reading the shift register, which clears the BUSY bit, clears the interrupt, and resets the interface.

- Optionally, the CPU can read the start bit, stop bit and parity bit to check for errors. There is no hardware parity checking. It is up to the CPU to calculate what the parity should be, and compare that with the parity bit in the status register, but the CPU does have "JP PO,nn" and "JP PE,nn" instructions! Keyboard data has odd parity, so the parity bit in the status register should only be set when the shift register data itself has even parity.

4.5.4. Keyboard transmit procedure

This is the process for data transmission to the keyboard. The CPU's intervention is rather greater than for reception, but this is a much less frequent occurrence.

- First, the CPU must check that the interface is not BUSY. Any in-progress transfer from the keyboard which has progressed far enough to set BUSY status should be allowed to complete. (If BUSY becomes true between this stage and the next, there is no problem as long as only a few microseconds have elapsed.)
- The CPU forces the keyboard clock low, by writing 02 to the control register. The keyboard responds by releasing the bus.
- The CPU writes data to the shift register. This prepares the entire 11-bit stream, setting the start bit and parity bit to zero, and the stop bit to one.
- A minimum of 60μs after forcing the clock low, the CPU sets TX state, which connects the shift register to the data line. It should also reset the interface (because forcing the clock low would otherwise cause loss of synchronisation) and if necessary set the parity bit. All this can be achieved by writing 07 (or 87 if the data written to the shift register has even parity). This step causes a negative data transition, which the keyboard sees as a start bit.
- The CPU then releases the clock line by writing 01.
- Within 15ms the keyboard starts to take the data, and BUSY is set. Within a further 2ms, the keyboard finishes taking the data and interrupt IRQ1 is set.
- The CPU must respond to the interrupt by writing to the status register to reset the interface, and clear the TX bit, by writing 04.

4.5.5. Keyboard holdoff

The CPU can prevent the keyboard from sending it data by holding the clock line low. It should check for not BUSY before setting the Force Keyboard Clock bit. The keyboard will not send data until the clock is released again. The interface must be reset after this.

4.6. Super-I/O Chip Interface

The ASIC provides an almost glueless interface to a Super-I/O (SIO) chip, providing a range of peripheral functions previously provided on the PcW main board or as options via the expansion bus. The SIO device provides address decoding suitable for an IBM PC with an I/O space of 1024 ports, so the ASIC presents the SIO with a modified address, to enable a port map more suitable for a Z-80. The address inputs to the SIO device are derived from the CPU address as follows:

SIO Address	CPU Address	
AEN	/A7 & /A6	(SIO selected for 00h-3Fh)
SA9	A5 + A4	
SA8	A5 + A3	
SA7	A5 & /A4 + /A5 & A3	
SA6	(As SA8)	
SA5	(As SA8)	
SA4	A3	
SA3	A5	
SA2…SA0	A2…A0	

The mapping of Z-80 address to Super-IO address is shown in this table.

Z-80 Address	S-IO Address	Comment
00-07	000-007	Nothing selected
08-0F	1F0-1F7	IDE CS0
10-17	200-207	Games port at 201
18-1F	3F0-3F7	FDC and IDE CS1
20-27	3E8-3EF	Serial Port 2 (IRQ3)
28-2F	3F8-3FF	Serial Port 1 (IRQ4)
30-37	368-36F	Nothing selected
38-3F	378-37F	Parallel Printer 378-37A

AEN Typically requires inverting, because the AEN pin on the Winbond W83787 device is active low, although this is not stated in the data sheet.

4.7. Test Logic

There are two types of test logic: Logic to allow external access to the Z-80 macro, or to allow use of an external Z-80, etc, via the TSTN and EMUN pins, and logic to put internal circuitry into special test modes, via illegal states on normal input pins.

4.7.1. The EMUN and TSTN pins.

Four modes are selectable via these pins. To acheive normal operation, TSTN should be left open (it has a strong on-chip pull-up resistor) or tied high. EMUN must be high. The modes are:

TSTN = 1, EMUN = 1. Normal operation. The on-chip Z-80 CPU is used, and the ASIC behaves as described in this document.

TSTN = 1, EMUN = 0. Emulation mode. The on-chip Z-80 CPU is disabled, and an external Z-80 emulator can be used instead. Some of the pins are redesignated as shown in Appendix B, but otherwise the ASIC behaves as described in this document. Note that the ASIC can not be operated at full speed in this mode, because the timings for a real Z-80 are too imprecise. The ASIC uses minimum power in this mode, with reset (PORN) active and the 48MHz clock stopped.

TSTN = 0, EMUN = 1. Z-80 test mode. The on-chip Z-80 CPU is connected directly to pins on the ASIC, allowing it to be separately tested. Many ASIC functions are unavailable. This mode is intended only for NEC factory test purposes.

TSTN = 0, EMUN = 0. Leakage test mode. Those I/O pins which are used for Z-80 test are put into a high impedance state, allowing leakage measurements. There is no practical use for this mode.

4.7.2. Real-Time clock test Modes.

With the ASIC in Emulation Mode, asserting and then releasing the condition whereby RD, WR and IORQ are all low at the same time toggles in and out of RTC test mode. The high address lines then take on special functions:

A8	Increment 1/256 seconds register
A9	Increment seconds register
A10	Increment minutes register
A11	Increment hours register
A12	Increment days register
A13	Increment months register
A14	Increment years register

4.7.3. Display Controller test Modes.

With the ASIC in Emulation Mode, asserting and then releasing the condition whereby RD, WR and MREQ are all low at the same time toggles in and out of Display Controller test mode. The high address lines then take on special functions:

A8	Clock the BEEP counter (Beep ÷ 8)
A9	Clock the Horizontal Counter (Normally clocked at pixel rate ÷ 16)
A10	Clock the first Vertical counter (Normally clocked at line rate)
A11	Clock the second Vertical counter (Normally clocked at line rate ÷ 15)
A12	Clock the Pointer Address generator (Normally clocked at line rate)
A13	Clock the upper four bits of the Pointer Address generator

In addition, the ASIC pin assignments are modified as follows:

The functions of BEEP and PP1 are restored, i.e. the effect of EMUN on these pins is negated. The signals which would normally emerge via pins PP3/VR and PP2/VG are rerouted to SA7 and SA8 respectively. The three-state enables for PP2 and PP3 are OR'ed together and routed to SA9. The colour information (R, G, B and their respective three-state enables), before resynchronisation to the pixel clock, is routed to pins UA19 to UA14. Note that UA19 exists only when J5 is not fitted.

Appendix A I/O Address Maps

On-Chip I/O Address Map

Address	Output	Input
00h-DFh	Available for Off-Chip peripherals	
E0h-EFh	Colour Palette registers	Available for Off-Chip peripherals
F0h	Memory map for 0000h-3FFFh region	
F1h	Memory map for 4000h-7FFFh region	
F2h	Memory map for 8000h-BFFFh region	
F3h	Memory map for C000h-FFFFh region	
F4h	Keyboard Data shift register	
F5h	Keyboard Control	Keyboard Status
F6h	No effect	Jumper Status
F7h	Video Control	Timer Interrupt Counter
F8h	System Control	System Status
F9h	RTC Control Register	RTC 1/256 Seconds Register
FAh	RTC Seconds Register	
FBh	RTC Minutes Register	
FCh	RTC Hours Register	
FDh	RTC Days Register	
FEh	RTC Month Register	
FFh	RTC Year Register	RTC Year and Invalid Time Flag

Super-IO Chip Address Map

Address	Output	Input
08h-0Fh	IDE Hard Disk Task File Registers (SIO addresses 1F0h-1F7h)	
11h	IDE MSB Buffer Register (uses game port chip select)	
1Ah	FDC Digital Output Register	Undefined
1Ch	No effect	FDC Main Status Register
1Dh	FDC Data Register	FDC Data Register
1Eh	IDE Fixed Disk Control	IDE Alternate Status
1Fh	FDC Data Rate Register	FDC/IDE Digital Input Register
20h-27h	Serial Port No. 2, General Purpose (SIO addresses 3E8h-3EFh, IRQ3)	
28h-2Fh	Serial Port No. 1, Mouse (SIO addresses 3F8h-3FFh, IRQ4)	
38h	Printer data Register	Printer data Register
39h	No effect	Printer status Register
3Ah	Printer Control Register	Printer Control Register

Appendix B Pin List

Power Supply

Name	Number	Type	Description
GND	1, 28, 40, 53, 80, 84	GND	Ground
VDD	2, 29, 52, 79, 81	VDD	5V power supply

Processor, etc.

Name	Number	Type	Description	Rst
M1	91	4CD	CPU M1 (Opcode fetch) signal output M1 input in EMU mode	1 R
MREQ	70	4CD	CPU Memory Request output (input in EMU)	R
IORQ	71	4CD	CPU I/O Request output (input in EMU mode)	R
RFSH	3	4CD	Processor REFRESH output REFRESH input in EMU mode	1 R
RD	4	4CD	Processor READ strobe output (input in EMU)	R
WR	5	4CD	Processor WRITE strobe output (input in EMU)	R
WAIT AEN	74	4ZD	CPU WAIT output in EMU mode only Active high SIO address decode otherwise	R
A0…A13	7…20	4CD	CPU Address Bus output (input in EMU mode)	R
UA14…18 J0…J4	21…25	4CD	Upper address bus, from memory mapper Configuration Jumpers during reset	R
UA19 RCS2 J5	26	4CD	Upper address bit (one or two ROM mode) ROM chip select 2 (triple ROM mode) Configuration Jumper 5 during reset	R
UA20 RCS1 J6	27	4CD	Upper address bit (single ROM mode) ROM chip select 1 (multiple ROM mode) Configuration Jumper 6 during reset	R
RCS RCS0 J7	6	4CD	ROM chip select (single ROM mode) ROM chip select 0 (multiple ROM mode) Configuration Jumper 7 during reset	R
D0…D7	66…59	4C	CPU data bus	Z
IOWR	72	4	I/O Write: IORQ + WR output	0
IORD	73	4	I/O Read: IORQ + RD output	0
INT	78	4CD	Interrupt 5 input, active low Z-80 Interrupt output in EMU mode	R X

DRAM interface

Name	Number	Type	Description	Rst
MA0…MA9	37, 35, 33, 31, 30, 32, 34, 36, 38, 39	4	Multiplexed DRAM address bus	0
RAS	41	4Z	Row Address strobe	Z
CAS0 MA10	42	4Z	Column Address strobe bank 0 (J7 not fitted) DRAM address bus bit 10 (J7 fitted)	Z
MWE	43	4Z	DRAM Write Enable	Z
MD0…MD7	51…44	4CD	DRAM Data Bus	R
CAS1 CAS	54	4Z	Column Address strobe bank 1 (J7 not fitted) Column Address strobe (J7 fitted)	Z

Super-I/O Chip Interface

Name	Number	Type	Description	Rst
RMIO	55	4	Active high reset	0
PCK	58	4	24MHz clock output	0
AEN WAIT	74	4ZD	Active high address decode for 00h-30h CPU WAIT signal in EMU mode	R
SA7…SA9	77…75	4ZD	Modified address lines	R
IRQ3, IRQ4, IRQ6, IRQ7	87…90	CD	Interrupt inputs, active high	R
TC	67	4	Floppy disk terminal count	0

Peripheral and Miscellaneous

Name	Number	Type	Description	Rst
PORN	92	S	Power-on reset input	L
CK48	57	C	48MHz clock input	x
XT1, XT2	82, 83	special	32.768kHz oscillator for RTC	x
PS	93	SU	RTC Power Sense input	x
KCL	85	OS	Keyboard Clock	Z
KDA	86	OC	Keyboard Data	Z
BEEP ZCK	56	4	Drive signal for Beeper (normal mode) Z-80 clock output (EMU mode)	0 X
PP0	94	4	General purpose output port	0
PP1 NMI	95	4	General purpose output port (normal mode) Z-80 NMI output (EMU mode)	0
PP2, PP3 VB, VR A14, A15	96, 97	8C	General purpose output ports: J4 not fitted Blue & Red video, three-level: J4 fitted Z-80 address inputs in EMU mode	Z
VG	98	8Z	Green video output, three-level	Z
SYH	99	4	Horizontal Sync, positive going	0
SYV	100	4	Vertical Sync, positive going	0
EMUN	69	C	Low selects EMU mode for external Z-80 CPU Must also be low for minimum power drain.	L
TSTN	68	CV	For factory test only - DO NOT CONNECT	--

Notes

I/O buffers (except VDD, GND and oscillator pins) are described by up to three characters, representing the output buffer type, input buffer type, and resistor, respectively. They are described more fully in the next appendix: "Electrical Characteristics".

Output buffer type is either:

- 4 Standard 4mA (nominal) output (three-state if followed by C, S or Z)
- 8 Standard 8mA (nominal) output (three-state if followed by C, S or Z)
- O Open-drain 4mA (nominal) output

Input type is either:

- C Standard CMOS input
- S Schmitt Trigger CMOS input
- Z No input, but output buffer is three-state

Resistor is either:

- D Standard (50KΩ nominal) pull-down resistor
- U Standard (50KΩ nominal) pull-up resistor
- V Strong (5KΩ nominal) pull-up resistor

During reset (when PORN is low) most outputs are either high impedance (Z), pulled low by a resistor (R), or actively driven low (0). This is shown by the "Rst" column in the preceding tables. For minimum battery drain in standby state, pins marked with an "L" in the "Rst" column must be low.

Appendix C Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}		- 0.5 … + 6.5	V
Input/Output Voltage	V_I/V_O		- 0.5 … V_{DD} + 0.5	V_{DD}
Output Current	$\|I_O\|$	4mA output	12	mA
		8mA output	24	mA
Package Dissipation	P_T	Ta = 0…70°C	550	mW
Opertaing Ambient Temp.	T_a		0…70	°C
Storage Temperature	T_{stg}		-65…150	°C

DC Characteristics

(VDD = 5 V ± 10 %, Ta = 0 …70°C)

Symbol	Parameter	Type	Condition	Min	Max	Unit
I_{DDQ}	Static Current Consumption		$V_{IN}=V_{SS}/V_{DD}$		TBD	µA
I_{DD}	Operating Current		48MHz		110	mA
V_{IH}	High level input voltage	C		.7V_{DD}	V_{DD}	V
		S		4.0	V_{DD}	
V_{IL}	Low level input voltage	C		0	1.5	V
		S		0	0.6	
V_H	Hysteresis Voltage	S		0.3	1.5	V
V_{IC}	Input Clamp Voltage	C, S	I_I = 18 mA	- 1.2		V
I_{IL}	Low level input current	C, S, Z	$V_{IN} = V_{SS}$	- 10	10	µA
	…with pull-up	U		- 270	- 40	µA
	…with strong pull-up	V		- 2.4	- 0.4	mA
I_{IH}	High level input current	C, O, S, Z	$V_{IN} = V_{DD}$	- 10	10	µA
	…with pull-down	D		40	270	
V_{OH}	High Level Output Voltage	4, 8	I_{OL} = 0		V_{DD} -0.1	V
		4	I_{OH} = - 2mA	2.4		V
		8	I_{OH} = - 4mA			
V_{OL}	Low Level Output Voltage	4, 8, O	I_{OL} = 0		0.1	V
		4, O	I_{OL} = 4mA		0.4	V
		8	I_{OL} = 8mA			
I_{OS}	Output short-circuit Current	4, 8	V_O = 0 V 1 pin, 1 sec		-250	mA