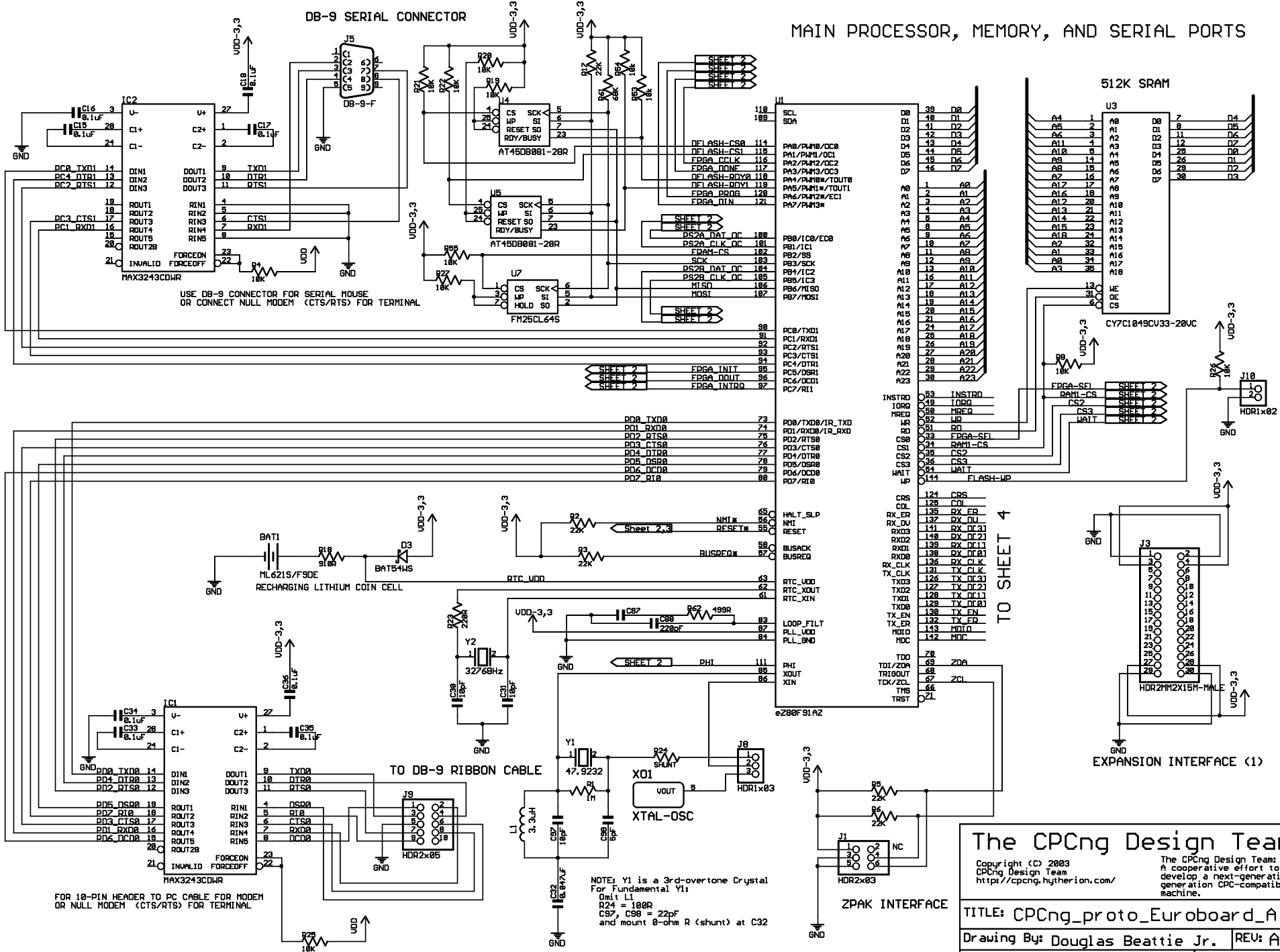


# MAIN PROCESSOR, MEMORY, AND SERIAL PORTS



**The CPCng Design Team**

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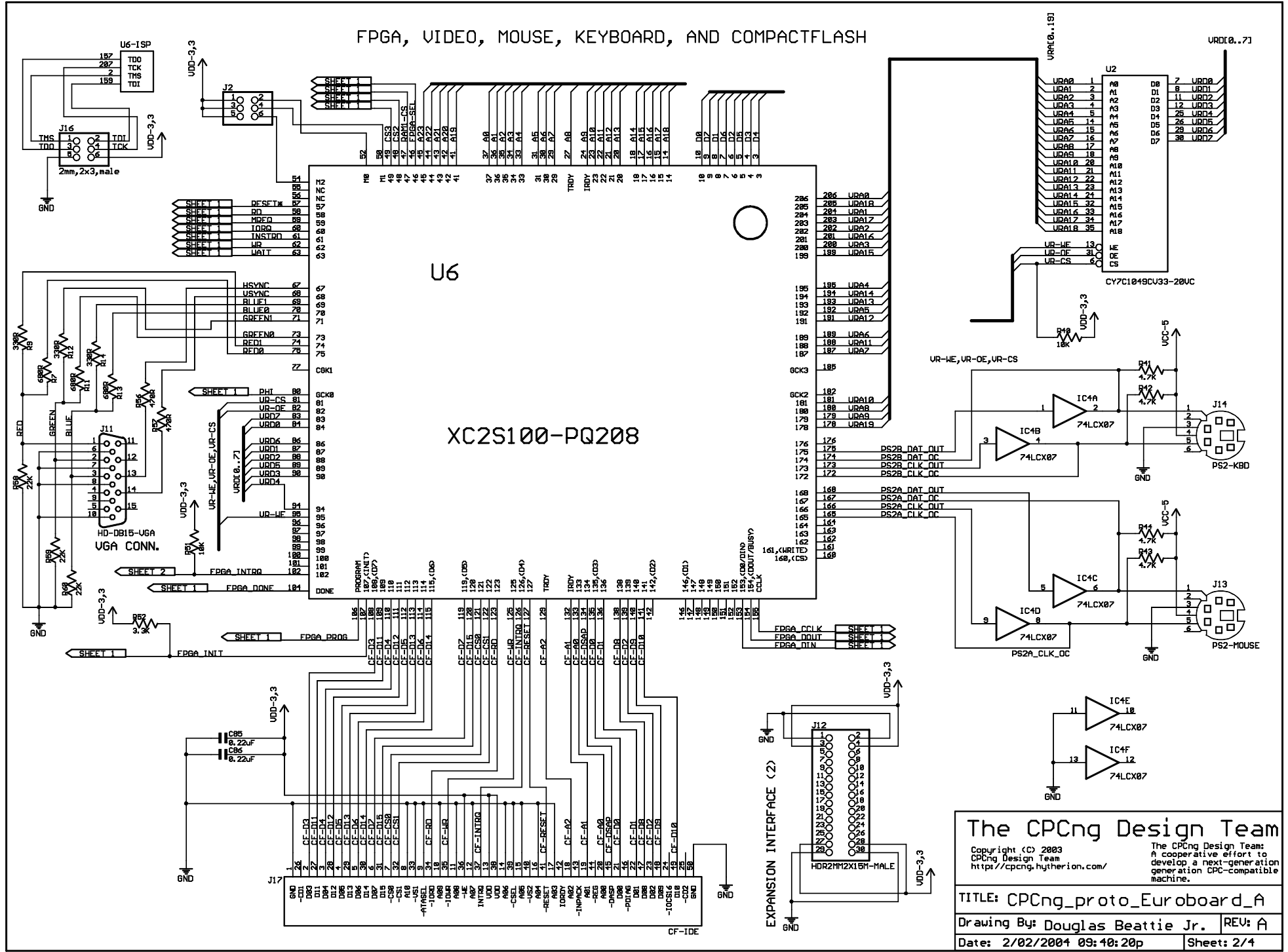
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 A cooperative effort to  
 develop a next-generation  
 generation CPC-compatible  
 machine.

**TITLE: CPCng\_proto\_Eurboard\_A**

**Drawing By: Douglas Beattie Jr. REV: A**

**Date: 2/02/2004 09:40:20p Sheet: 1/4**

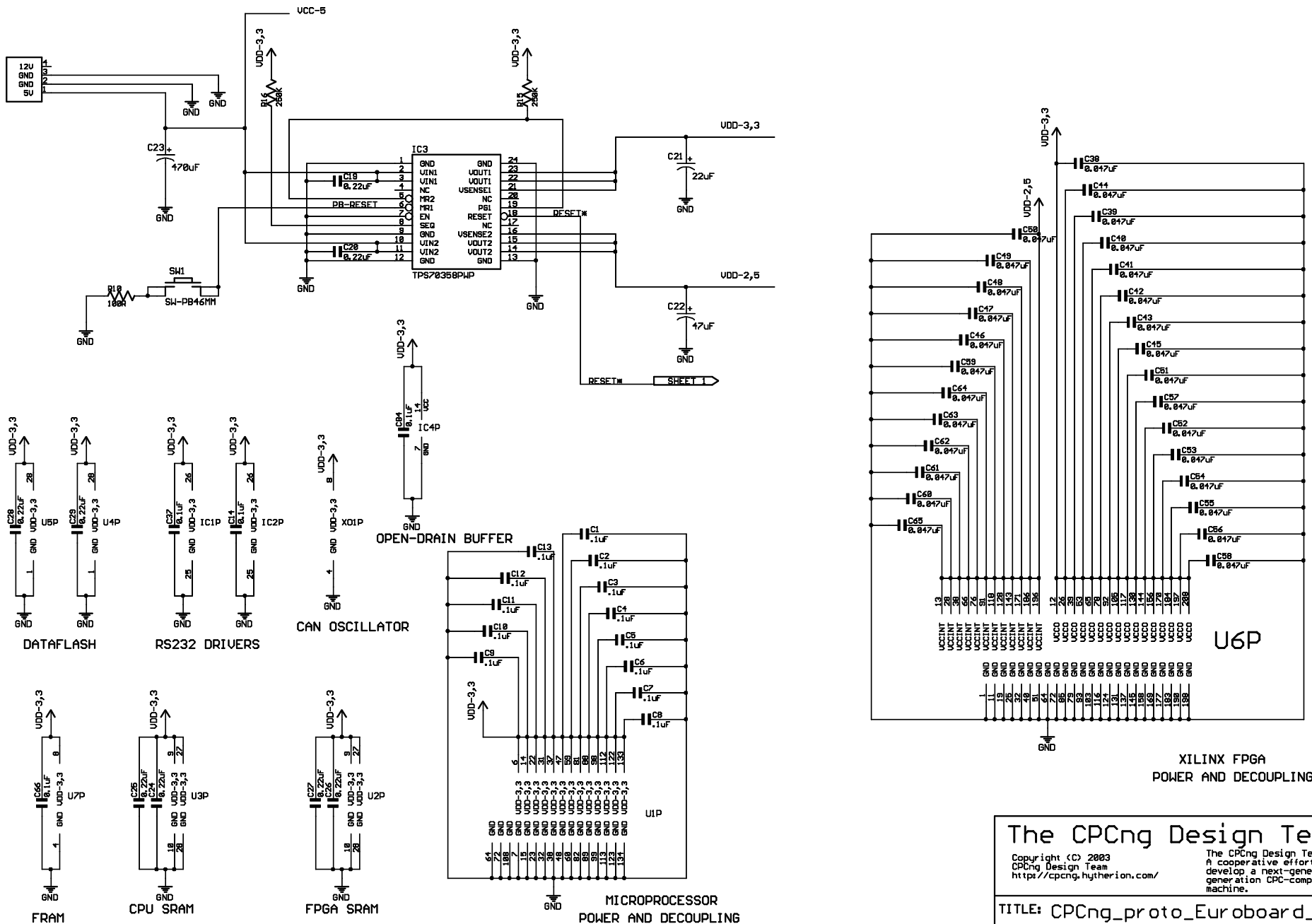
FPGA, VIDEO, MOUSE, KEYBOARD, AND COMPACTFLASH



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**Drawing By: Douglas Beattie Jr.** | **REV: A**  
**Date: 2/02/2004 09:40:20p** | **Sheet: 2/4**

# POWER SUPPLY AND RESET CIRCUIT



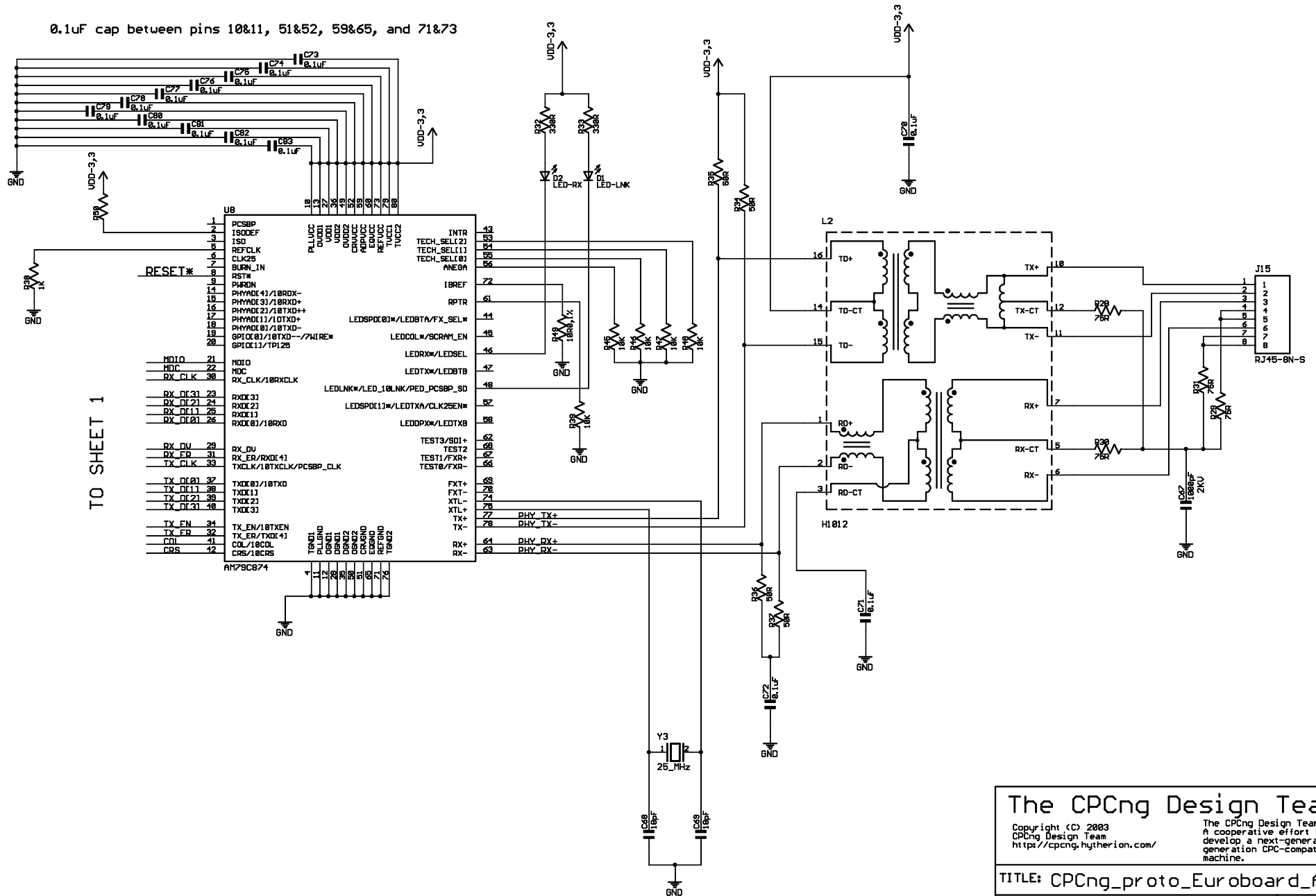
XILINX FPGA  
POWER AND DECOUPLING

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 Date: 2/02/2004 09:40:20p Sheet: 3/4

# ETHERNET PHY CIRCUIT AND CONNECTOR

0.1uF cap between pins 10&11, 51&52, 59&65, and 71&73



TO SHEET 1

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TITLE: CPCng_proto_Euroboard_A	
Drawing By: Douglas Beattie Jr.	REV: A
Date: 2/02/2004 09:40:20p	Sheet: 4/4