AMSTRAD CPC / CRTC 4

SHAKER V1.8 OUTPUT

LOGON SYSTEM 2021 / LONGSHOT

More information about CRTC in Amstrad Cpc Crtc Compendium
(“con de chat canadien”)

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UPDATE VRAM VS CRTC

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CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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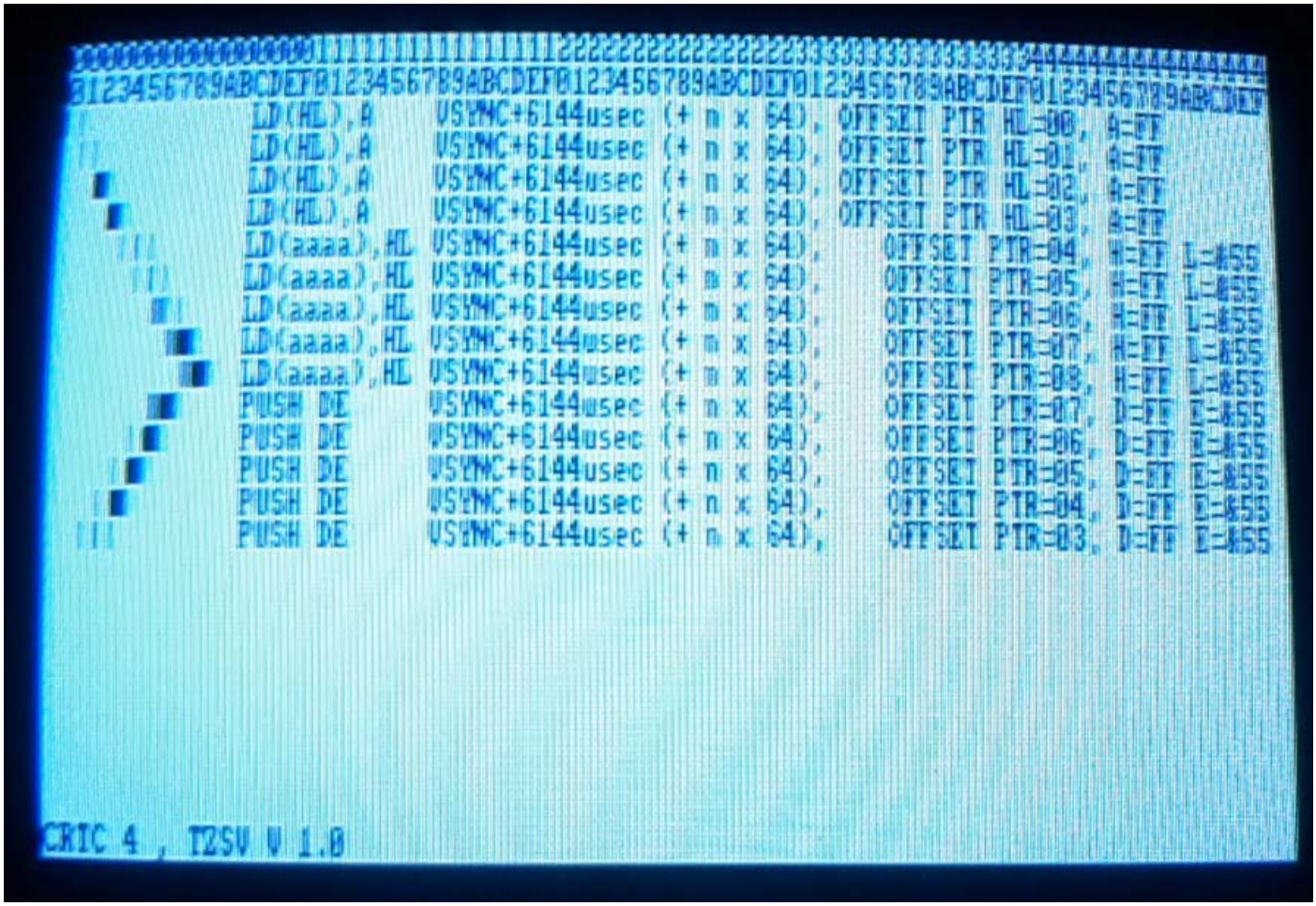

SKEW DISP ON R0 RUPTURE

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CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
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(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
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(Y) R3 UPD DURING HSYNC (8 TST)
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(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
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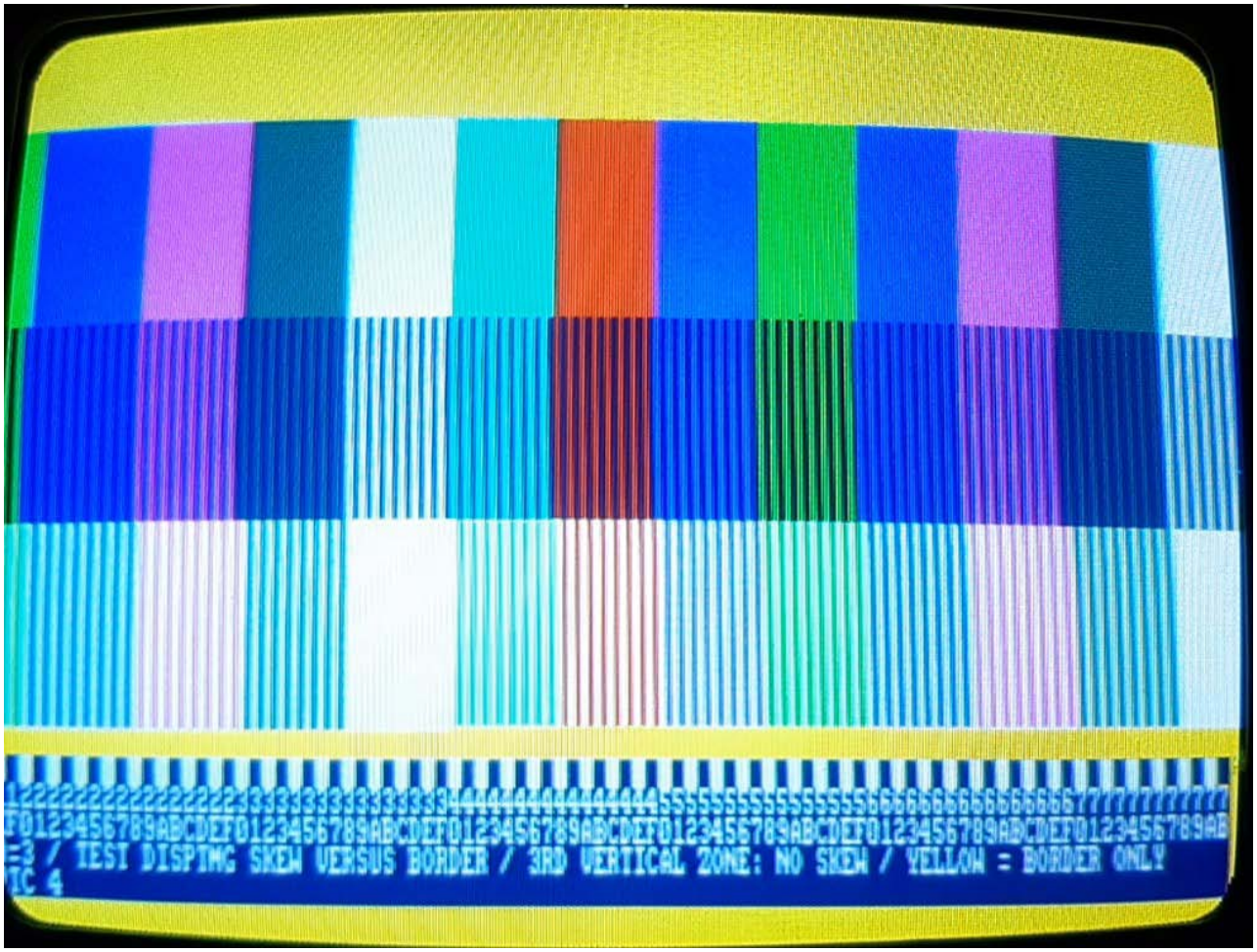
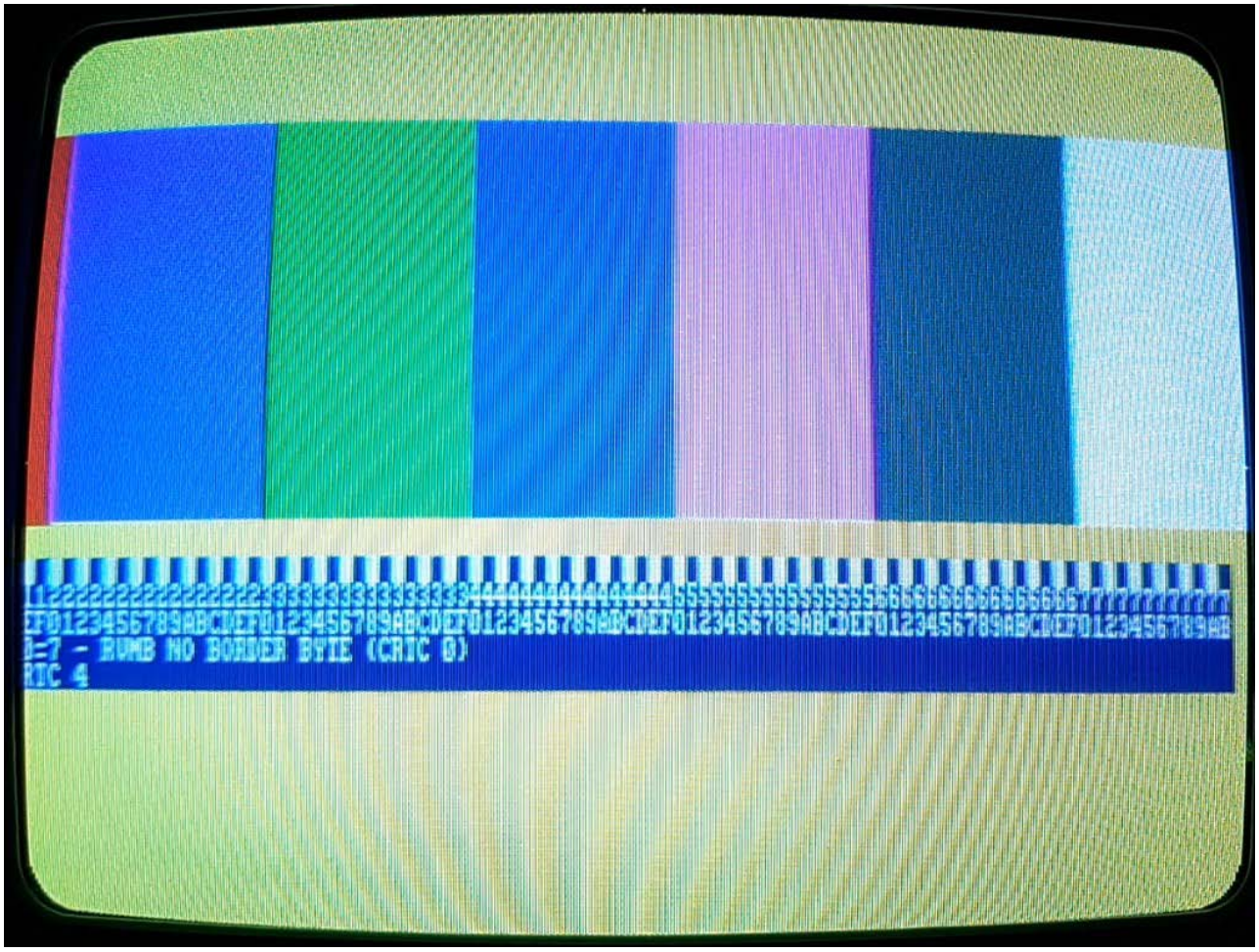
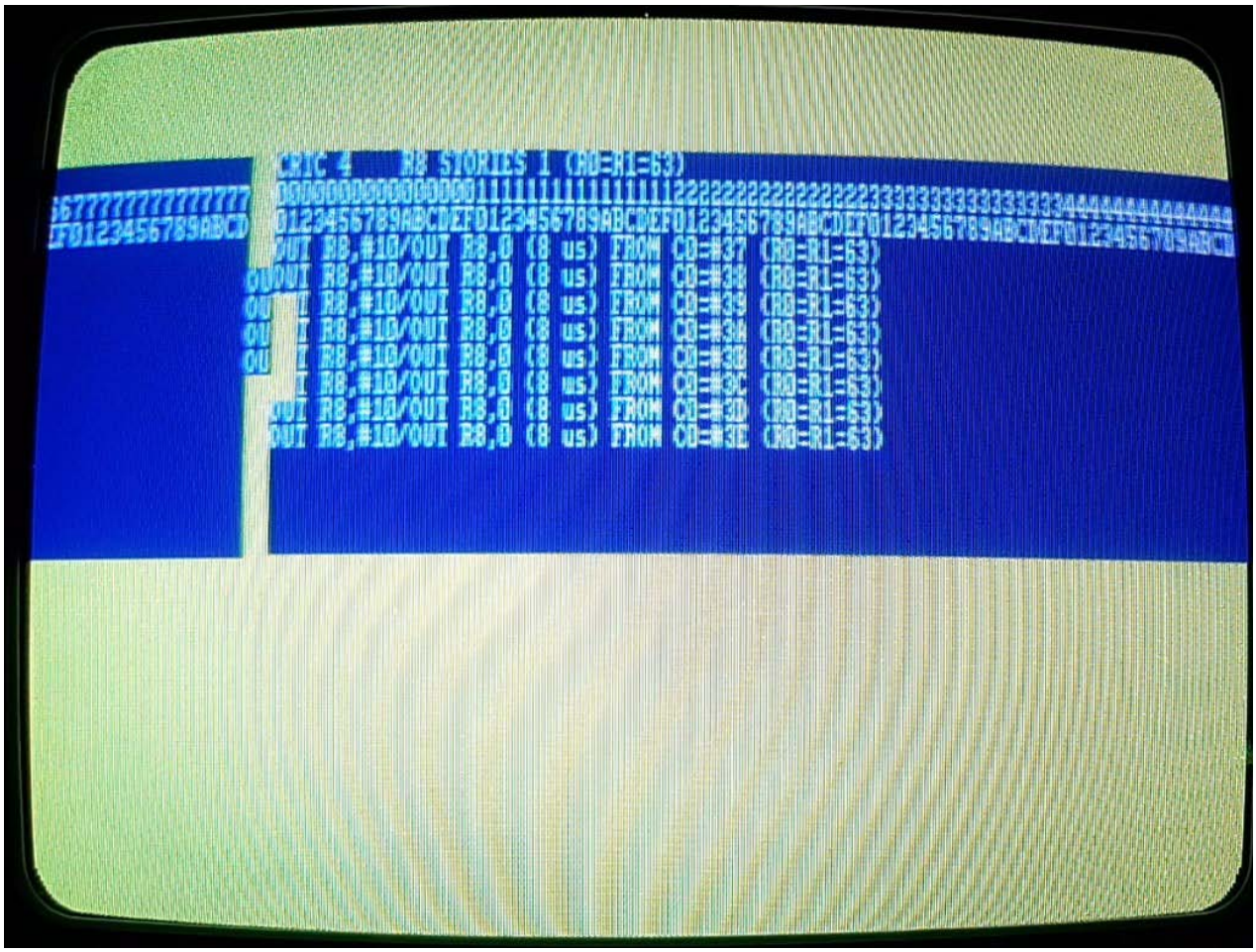
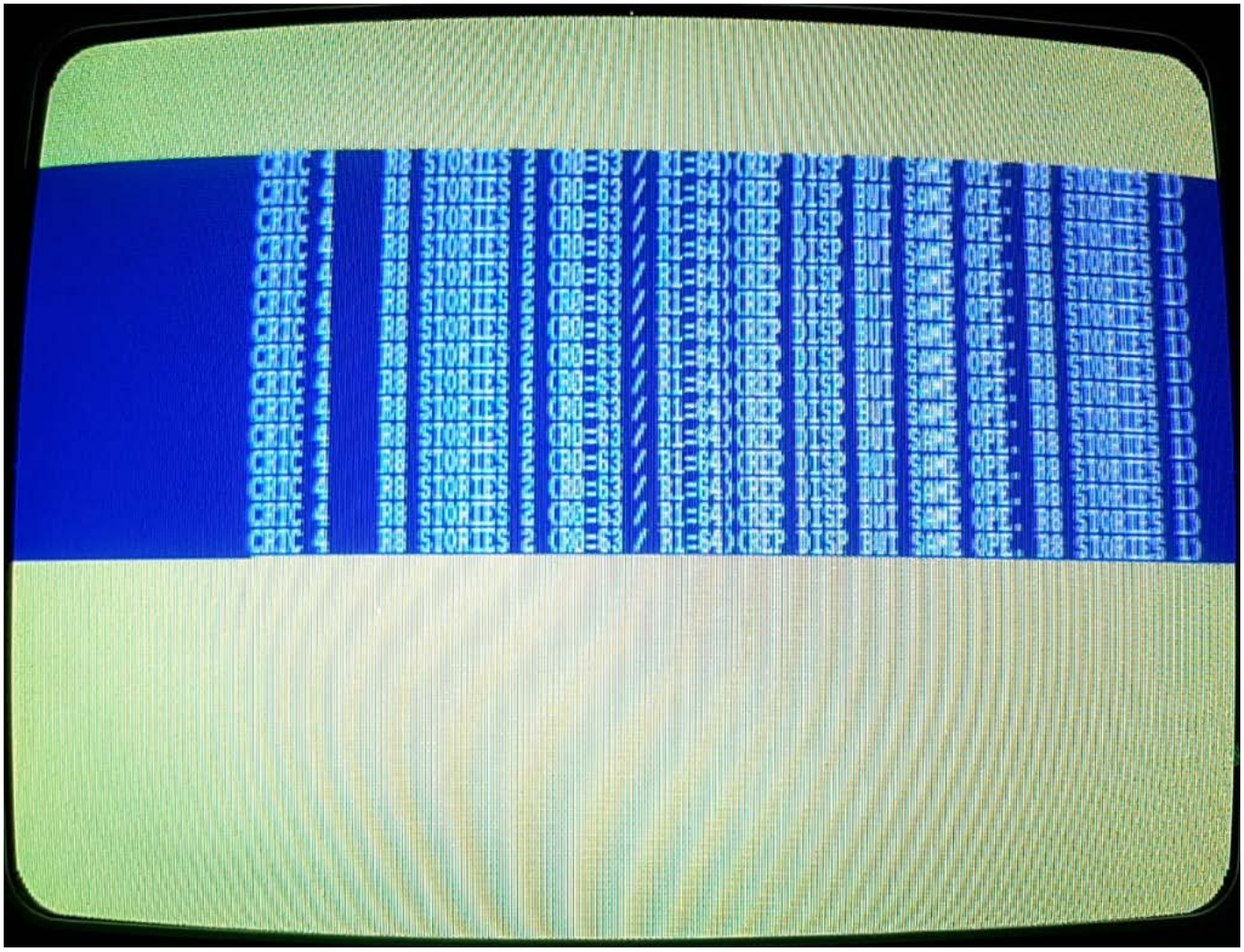
```




0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789AB
0=7 - BUMB NO BORDER BYTE (CRTC 0)
RTC 4


CRTC 4 R8 STORIES 1 (R0=R1=53)
0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#37 (R0=R1=53)
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38 (R0=R1=53)
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#39 (R0=R1=53)
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#3A (R0=R1=53)
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#3B (R0=R1=53)
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#3C (R0=R1=53)
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#3D (R0=R1=53)
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#3E (R0=R1=$3)


CRTC 4 R8 STORIES 2 (R0=63 / R1=64)(REP DISP BUT SAME OPE. R8 STORIES 1)

INTERRUPT DELAY FROM R2

```
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(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
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(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
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(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
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(Y) R3 UPD DURING HSYNC (8 TST)
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(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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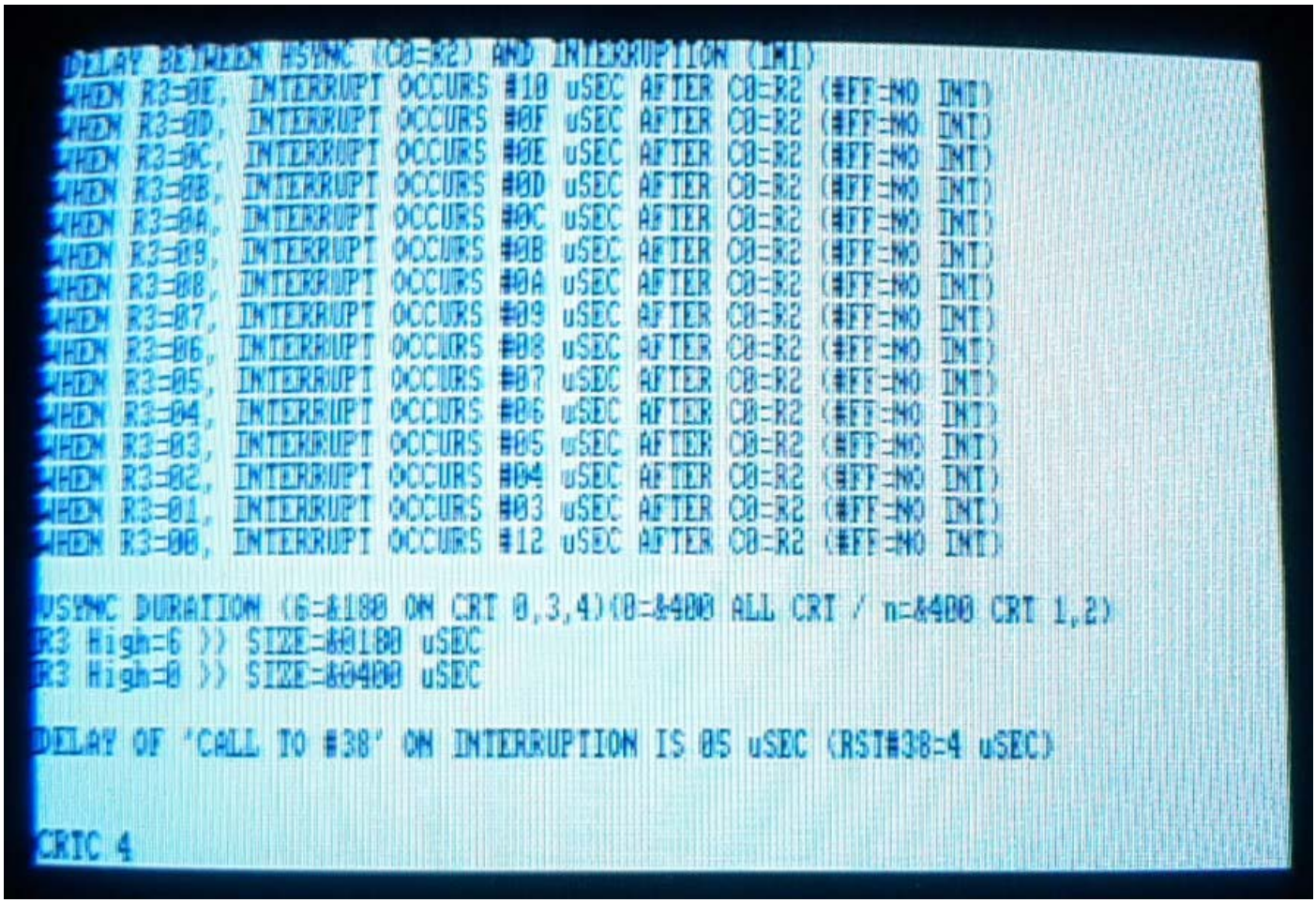
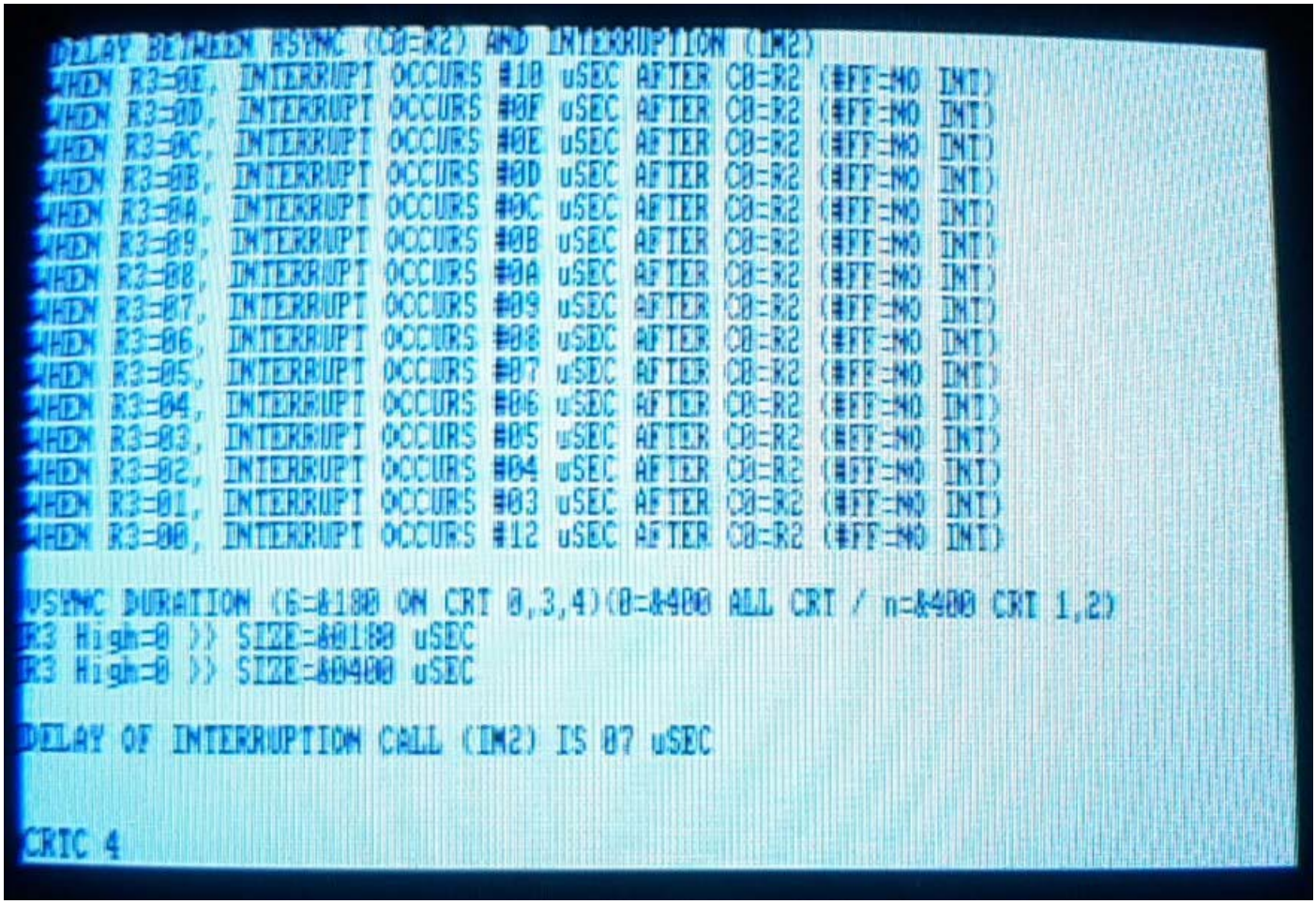
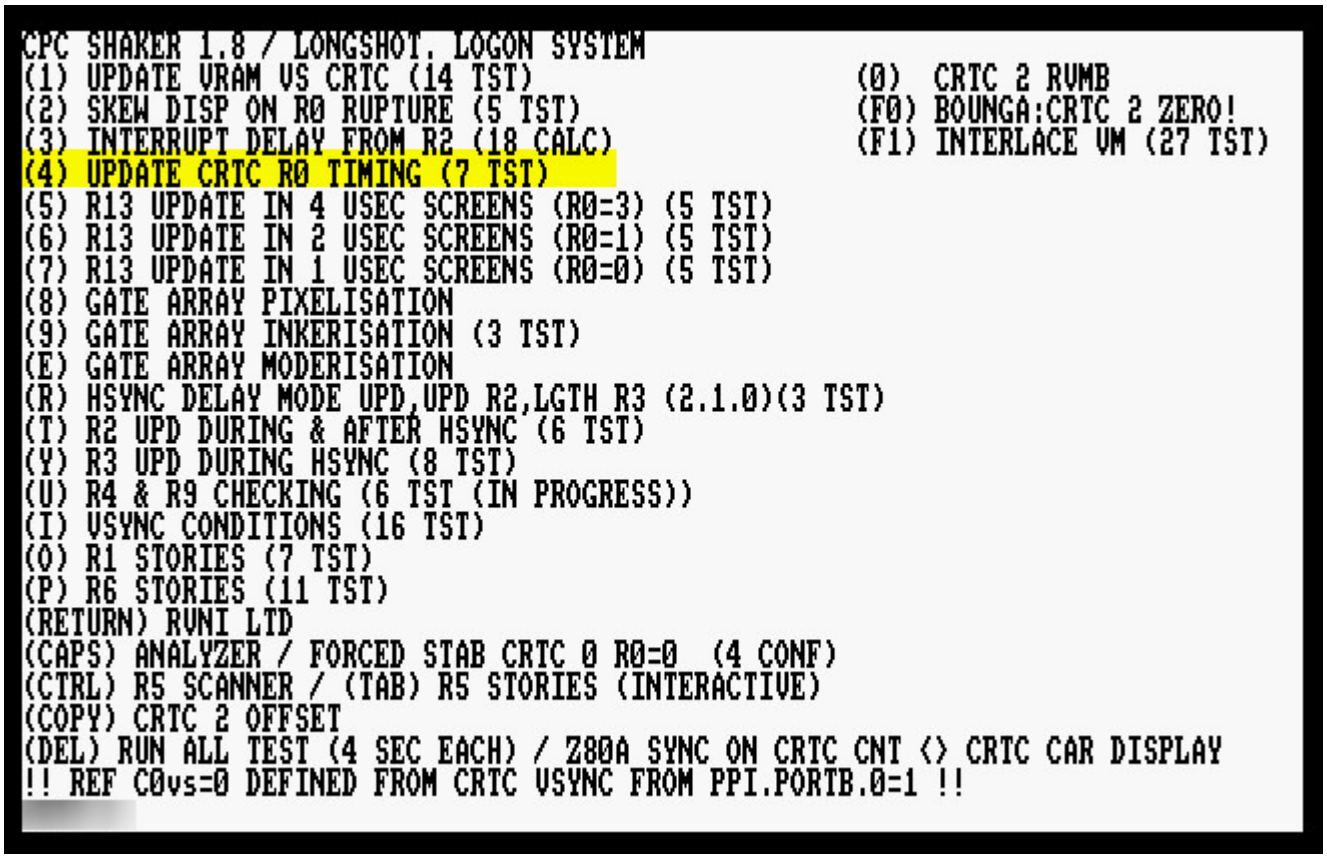
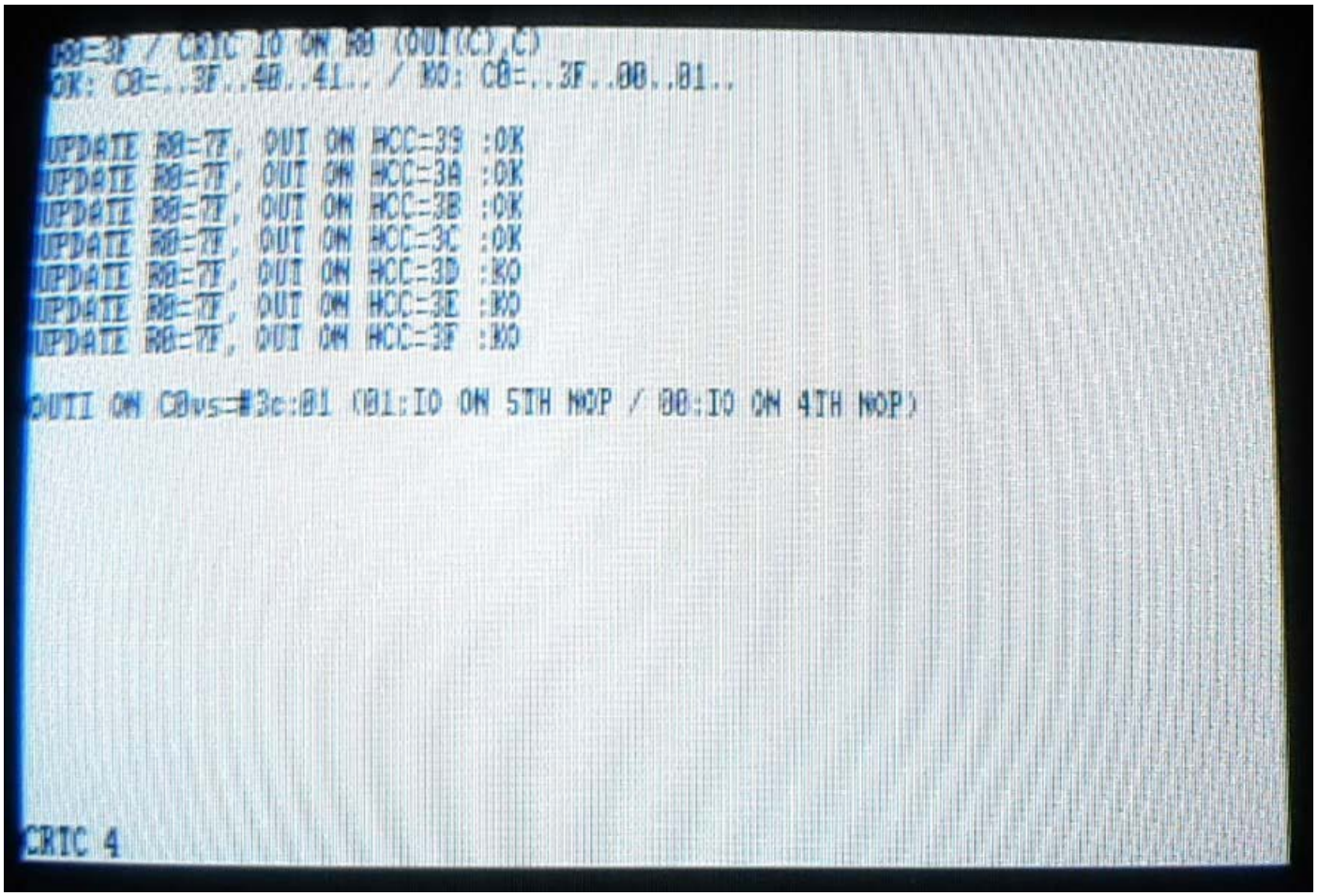



DELAY BETWEEN HSYNC (CB=R2) AND INTERRUPTION (IM2)
WHEN R3=0E, INTERRUPT OCCURS #10 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=0D, INTERRUPT OCCURS #0F uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=0C, INTERRUPT OCCURS #0E uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=0B, INTERRUPT OCCURS #0D uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=0A, INTERRUPT OCCURS #0C uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=09, INTERRUPT OCCURS #0B uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=08, INTERRUPT OCCURS #0A uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=07, INTERRUPT OCCURS #09 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=06, INTERRUPT OCCURS #08 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=05, INTERRUPT OCCURS #07 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=04, INTERRUPT OCCURS #06 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=03, INTERRUPT OCCURS #05 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=02, INTERRUPT OCCURS #04 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=01, INTERRUPT OCCURS #03 uSEC AFTER CB=R2 (#FE=NO INT)
WHEN R3=00, INTERRUPT OCCURS #12 uSEC AFTER CB=R2 (#FE=NO INT)
VSYNC DURATION (6=&100 ON CRT 0,3,4)(0=&400 ALL CRT / n=&400 CRT 1,2)
R3 High=0)) SIZE=&01100 uSEC
R3 High=0)) SIZE=&04400 uSEC
DELAY OF INTERRUPTION CALL (IM2) IS 07 uSEC
CRTC 4

UPDATE CRTC R0 TIMING





R13 UPDATE IN 4 USEC SCREENS (R0=3)

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
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(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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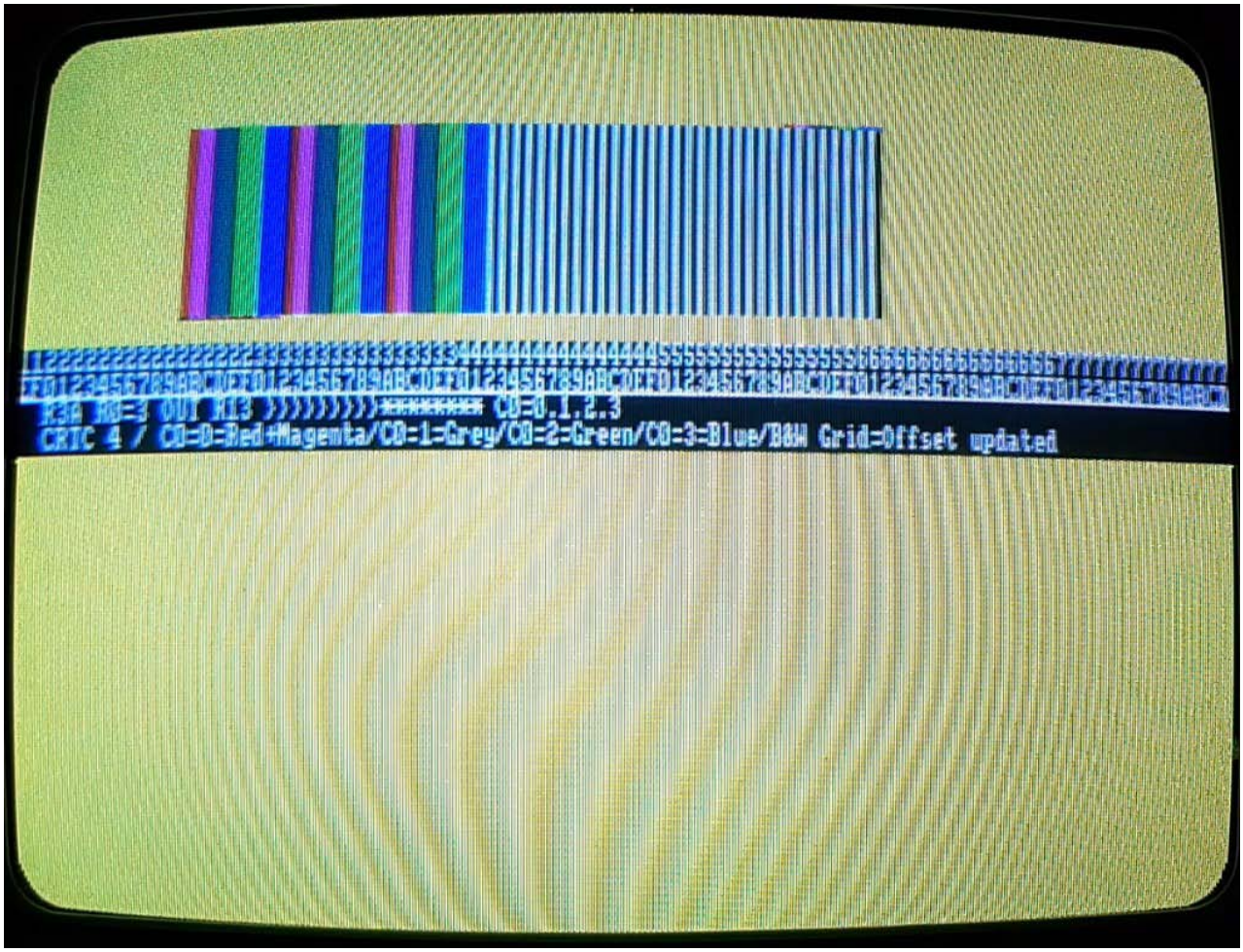
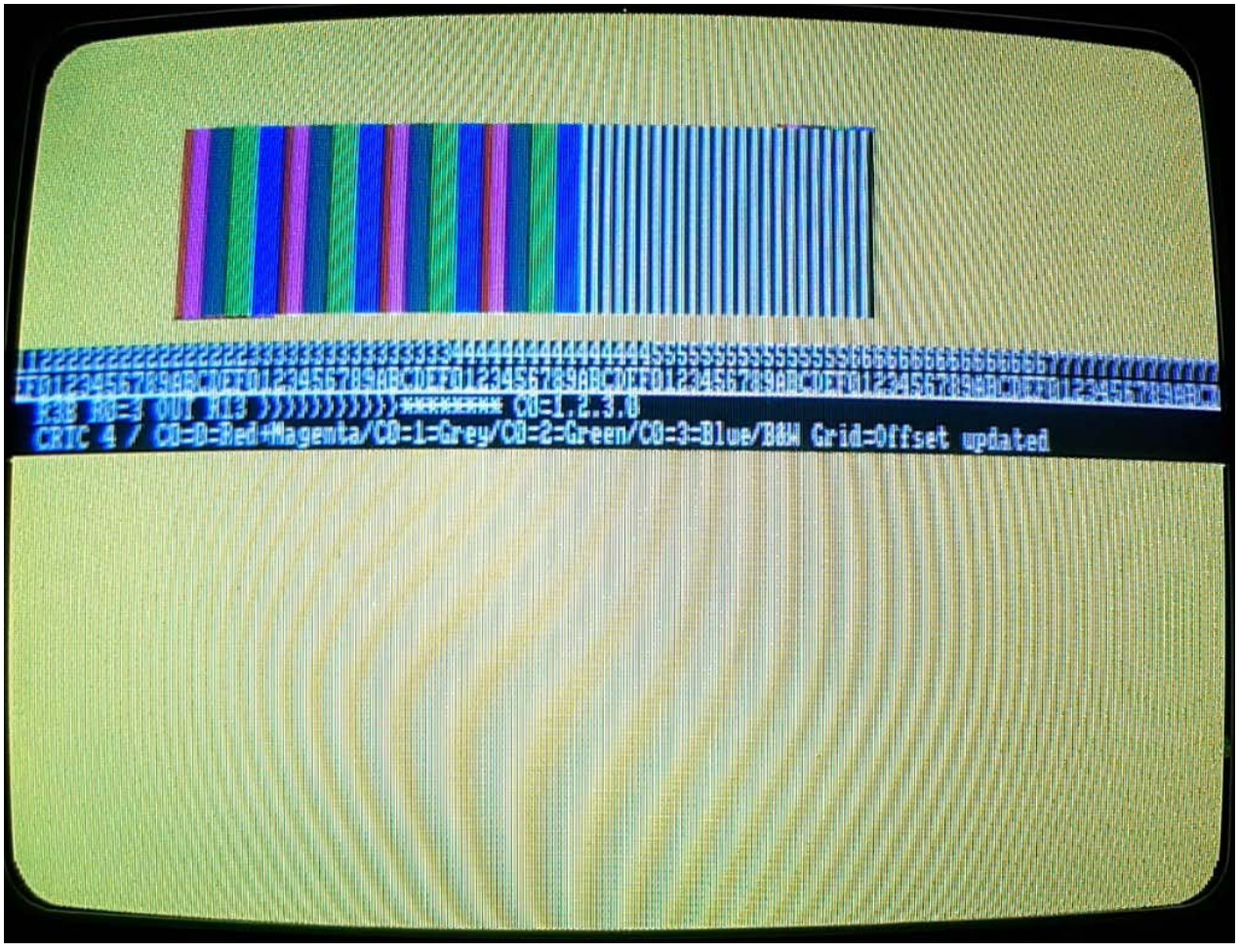
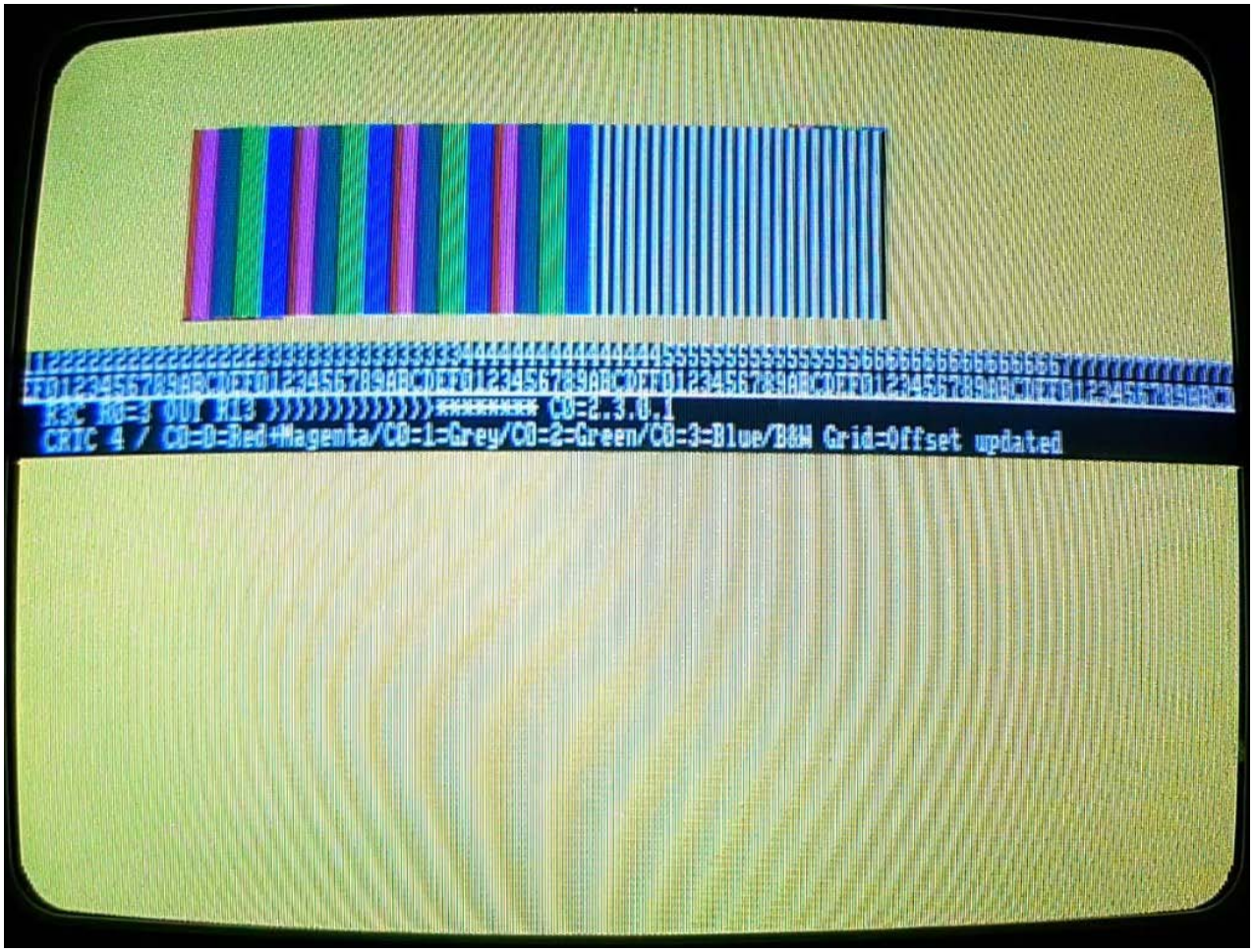
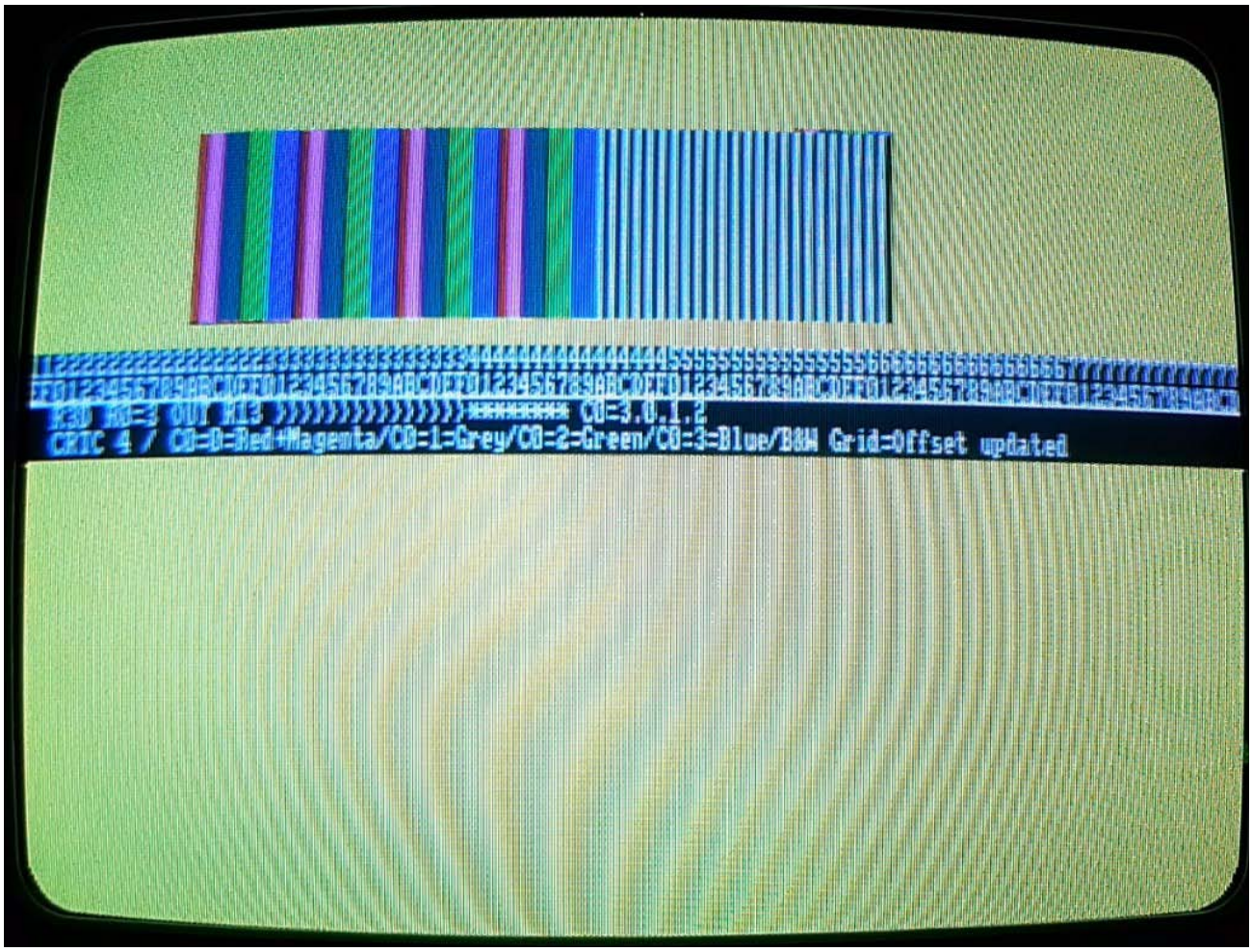
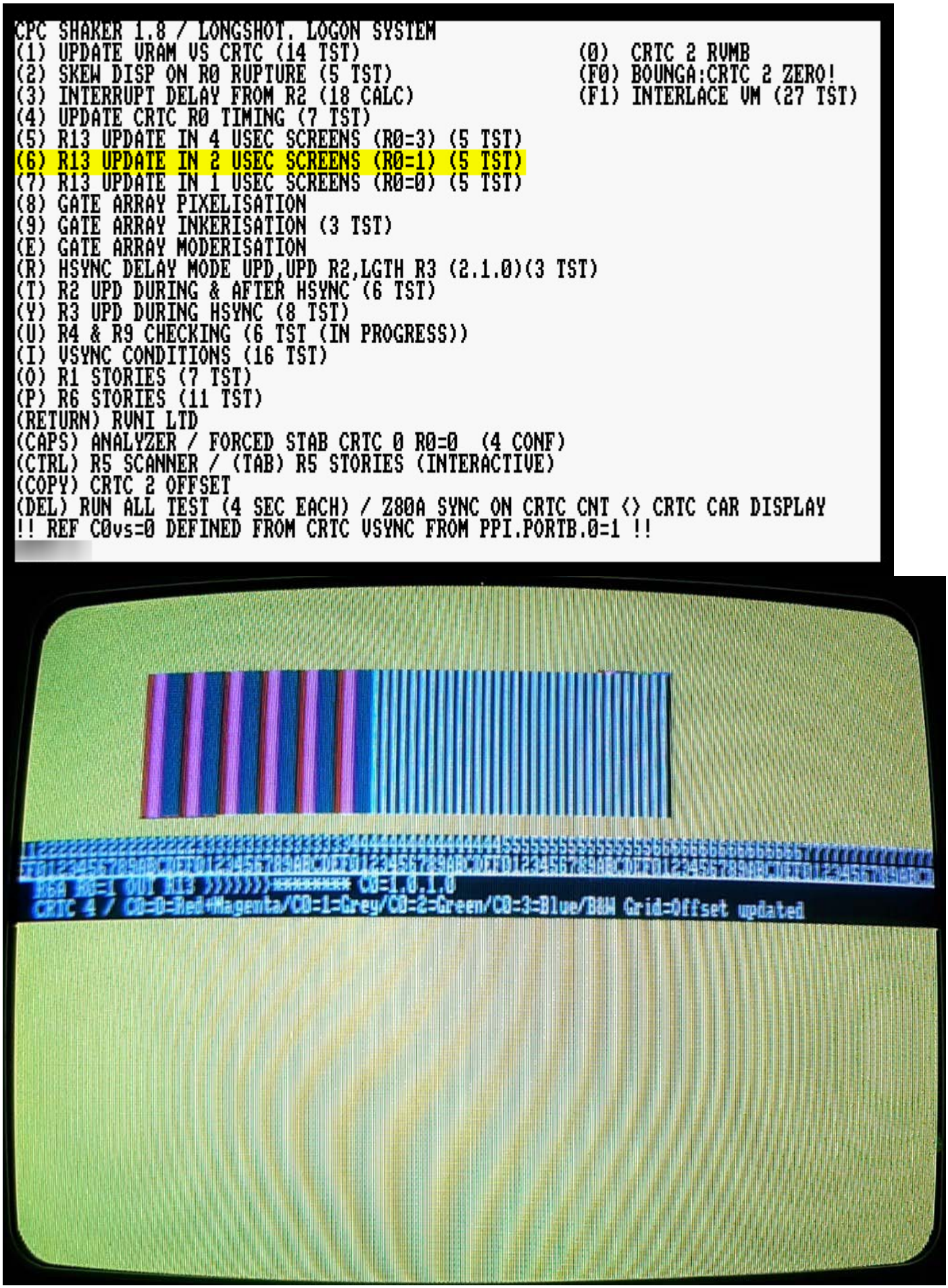

CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated

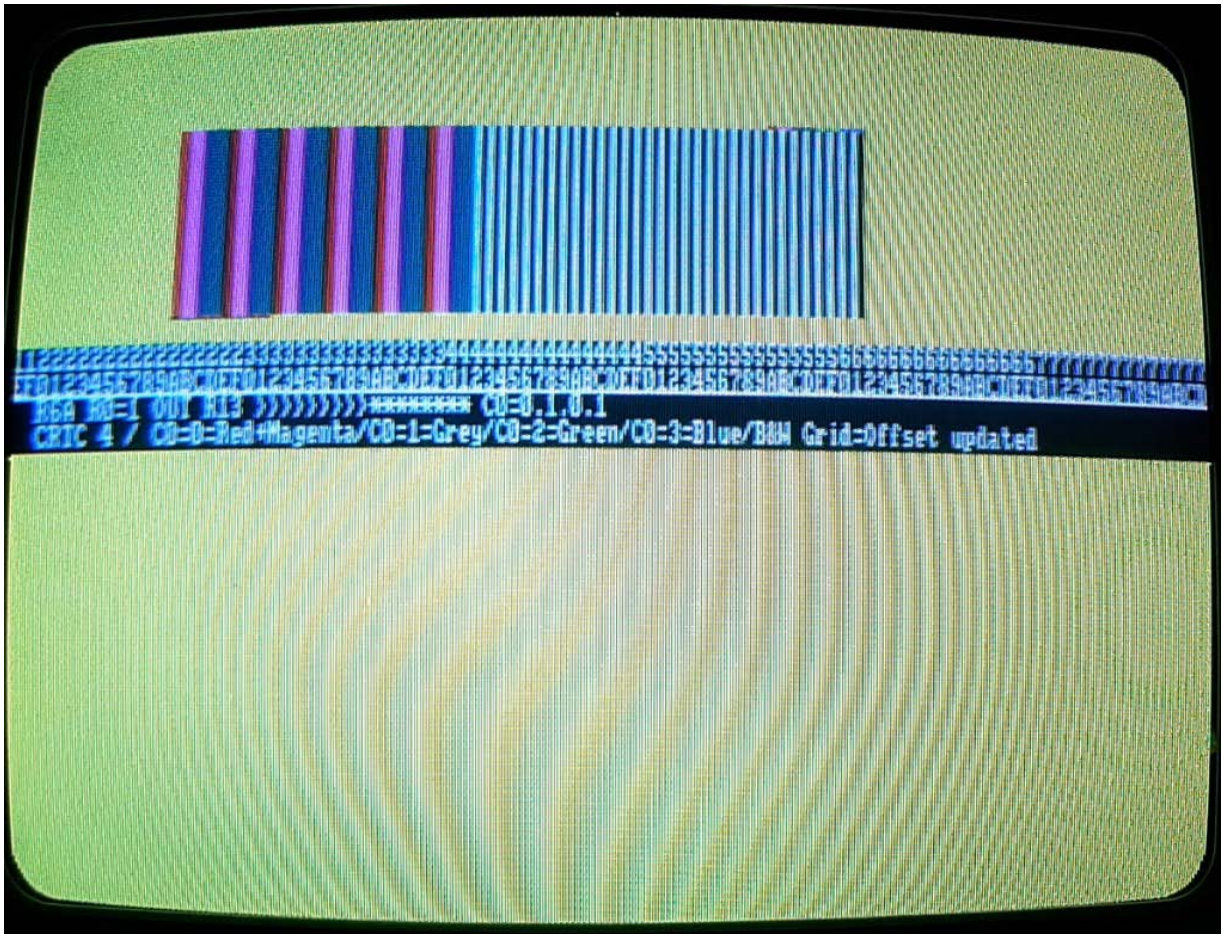

CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated


CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated

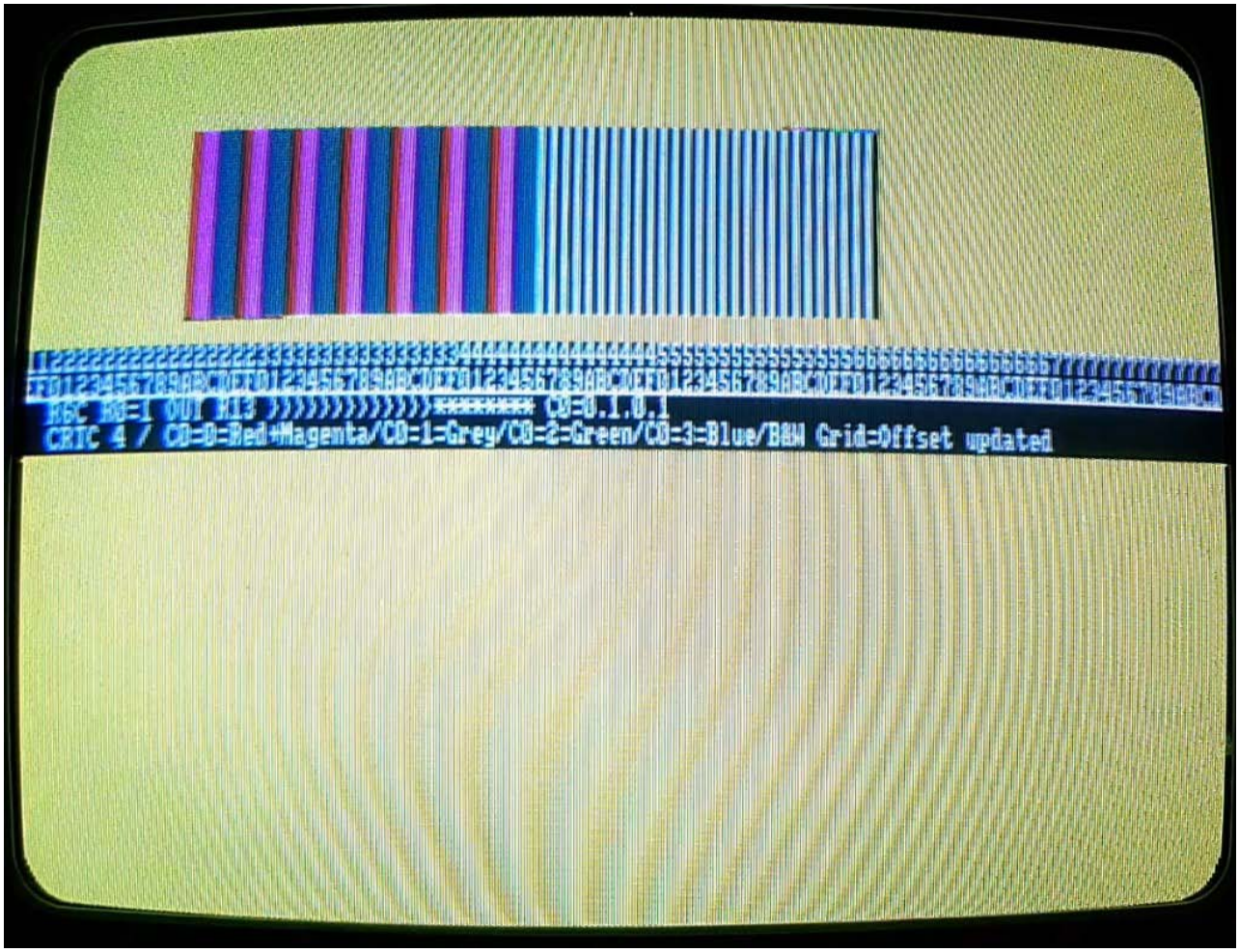

CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated

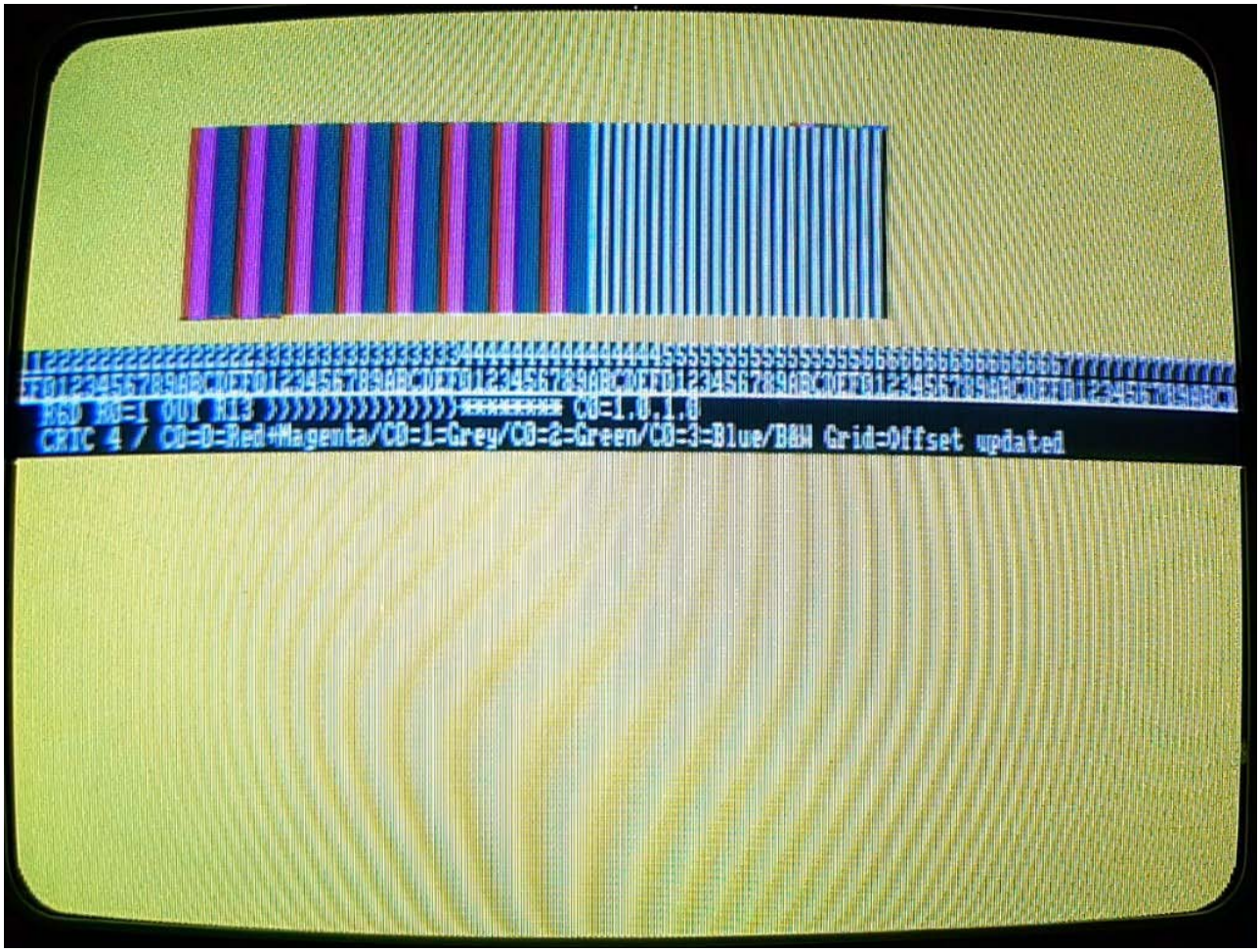
R13 UPDATE IN 2 USEC SCREENS (R0=1)




C0=0,1,0,1
CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated


C0=1,0,1,0
CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated


CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated


CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated

R13 UPDATE IN 1 USEC SCREENS (R0=0)

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
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(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(P) R6 STORIES (11 TST)
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(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
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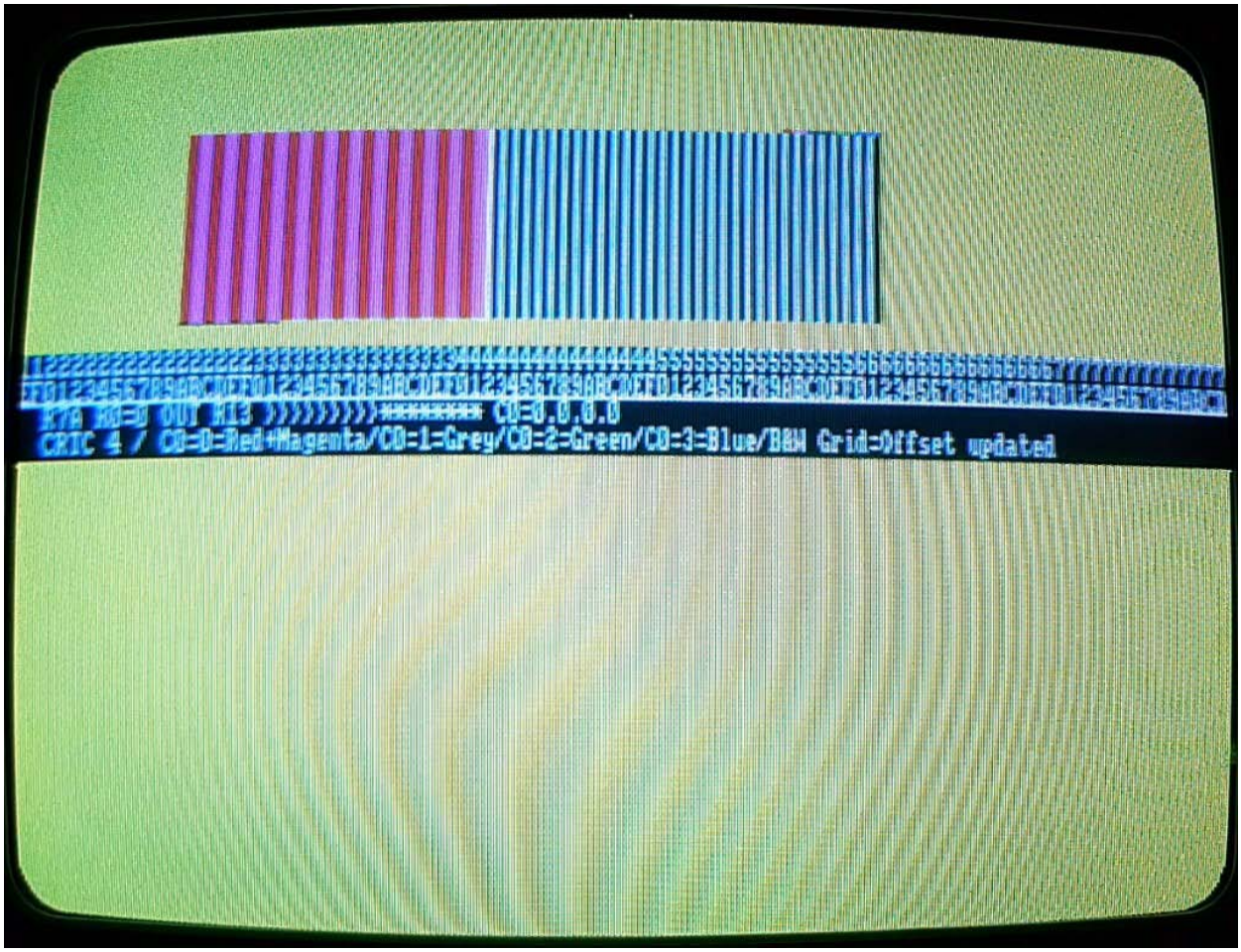
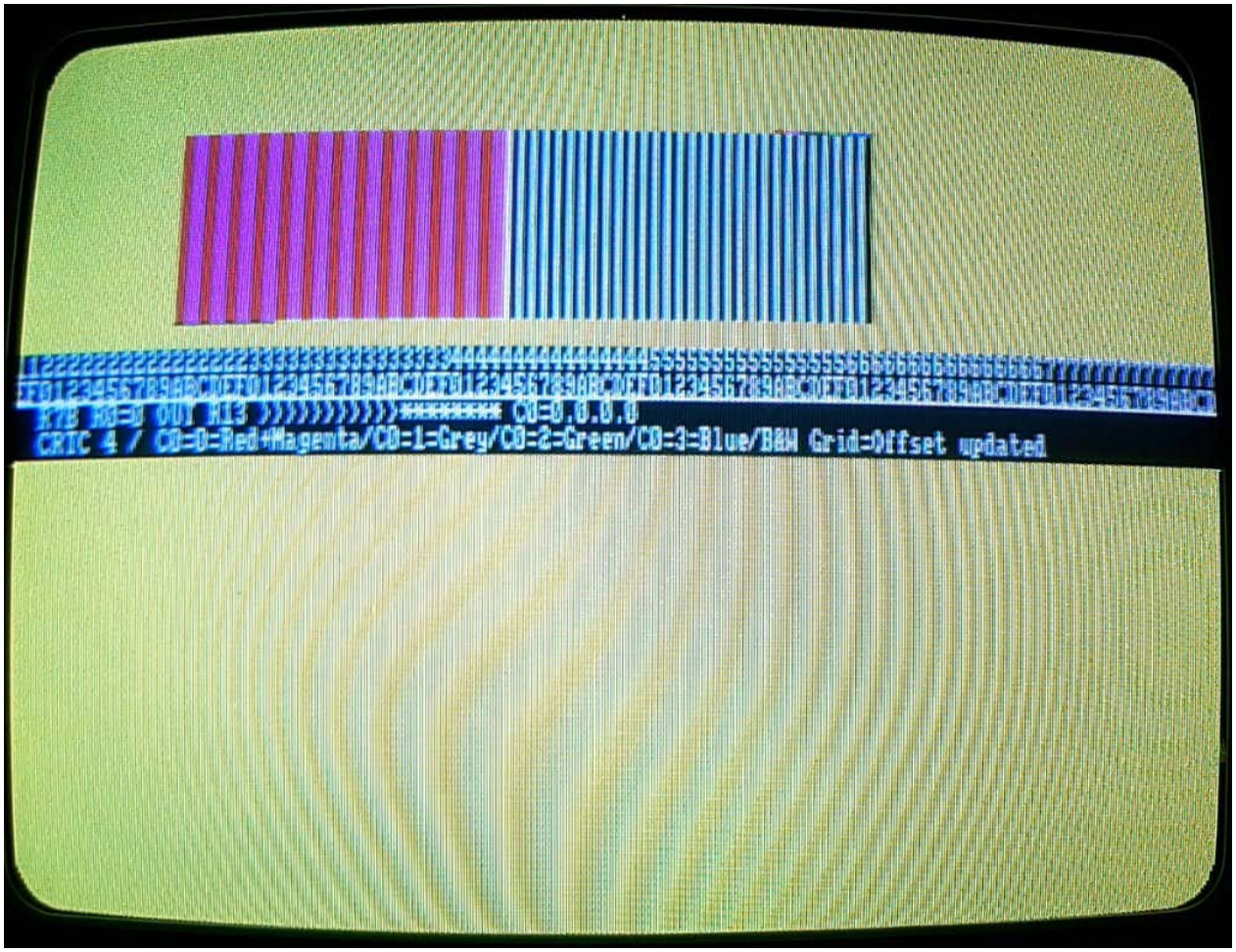
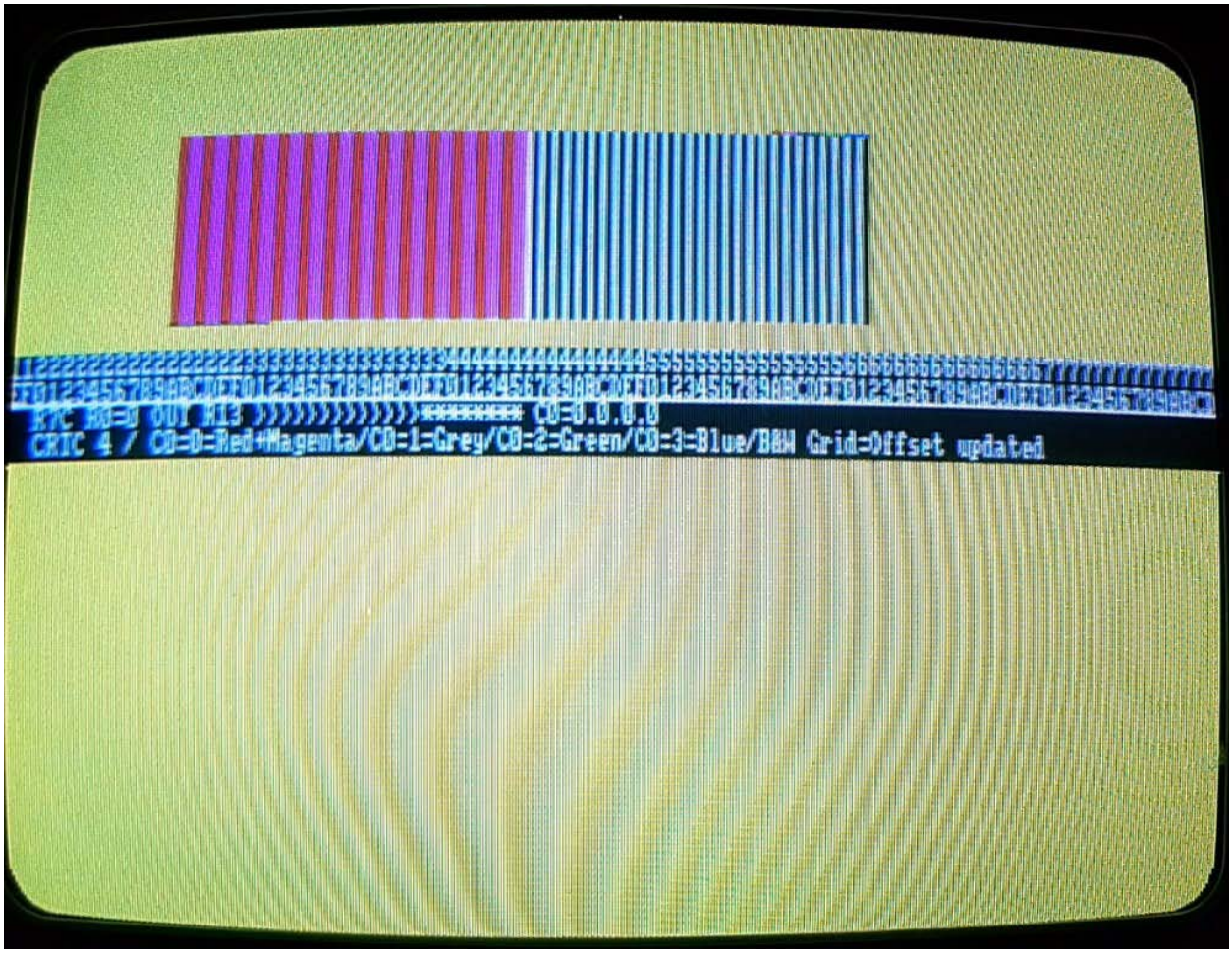

CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated


CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated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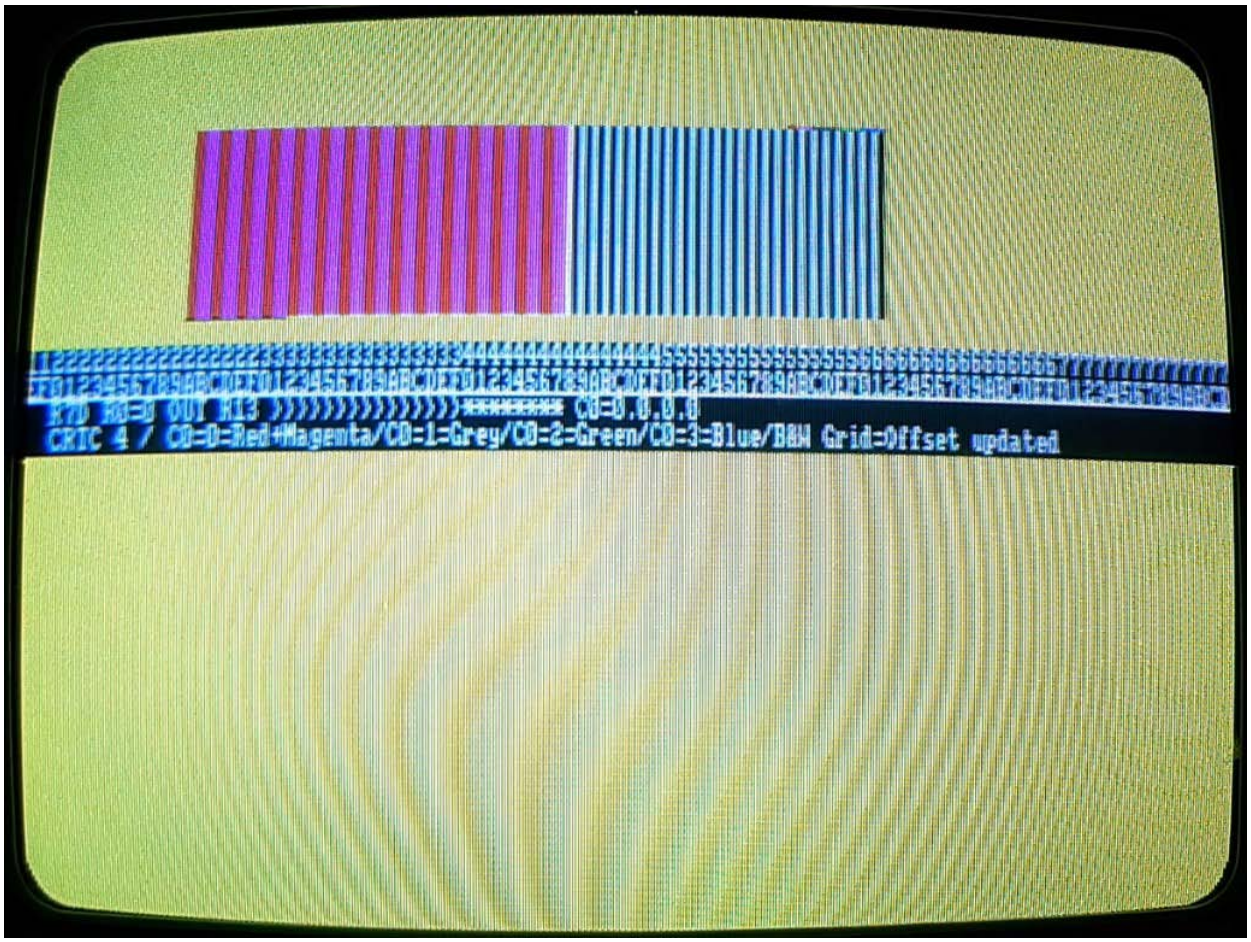
CRTC 4 / C0=0=Red+Magenta/C0=1=Grey/C0=2=Green/C0=3=Blue/B&W Grid=Offset updated

GATE ARRAY PIXELISATION

```
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(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
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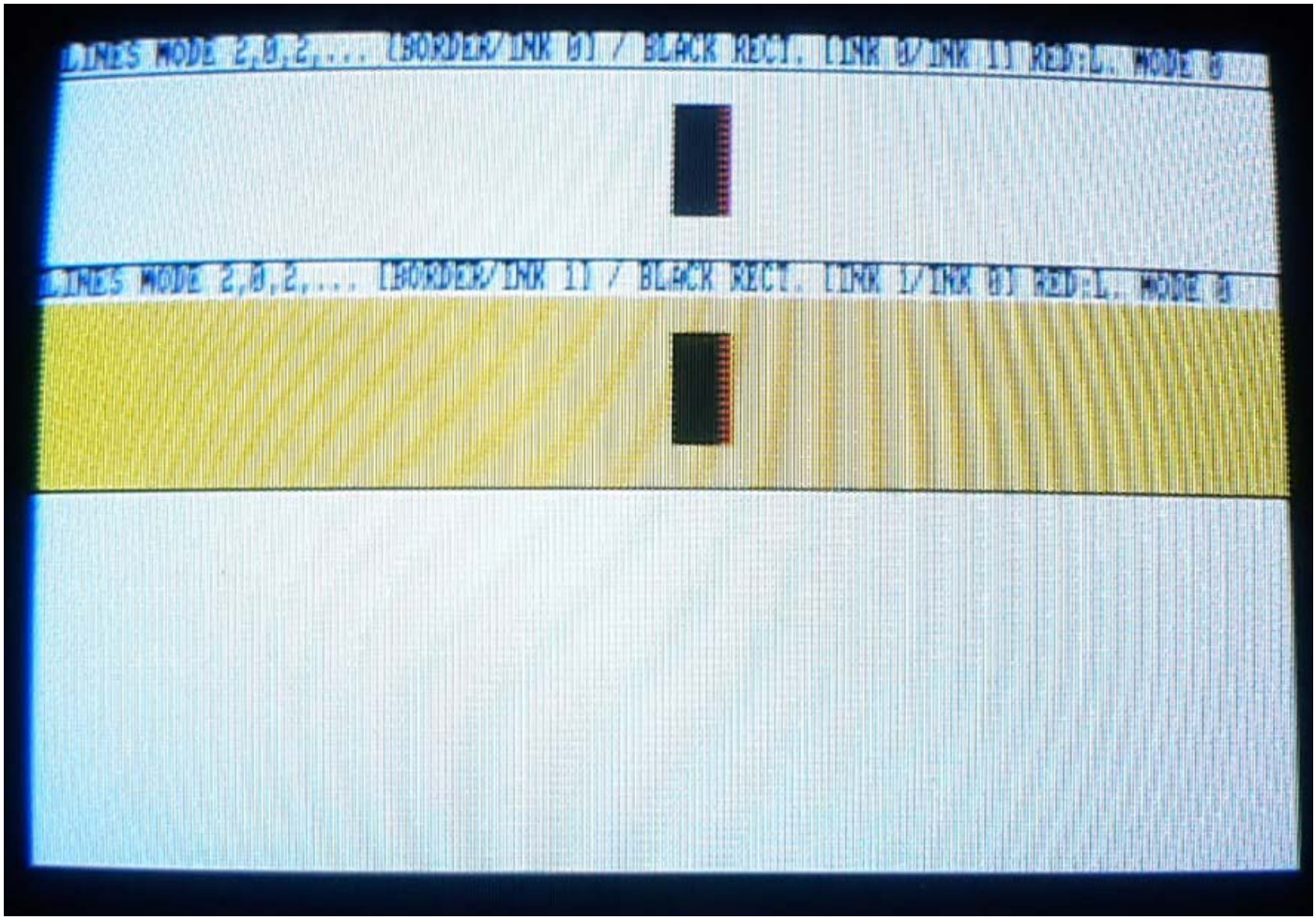
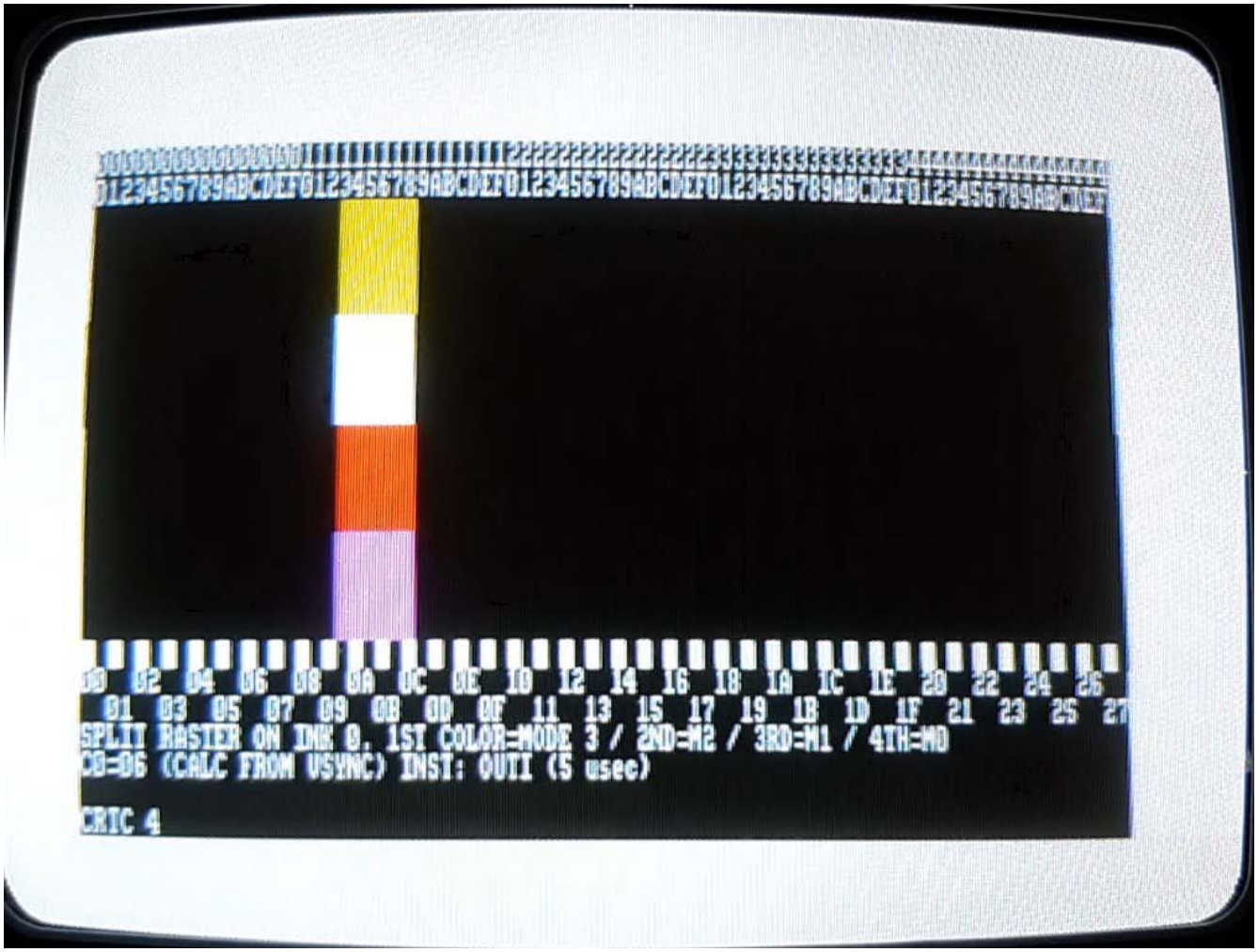
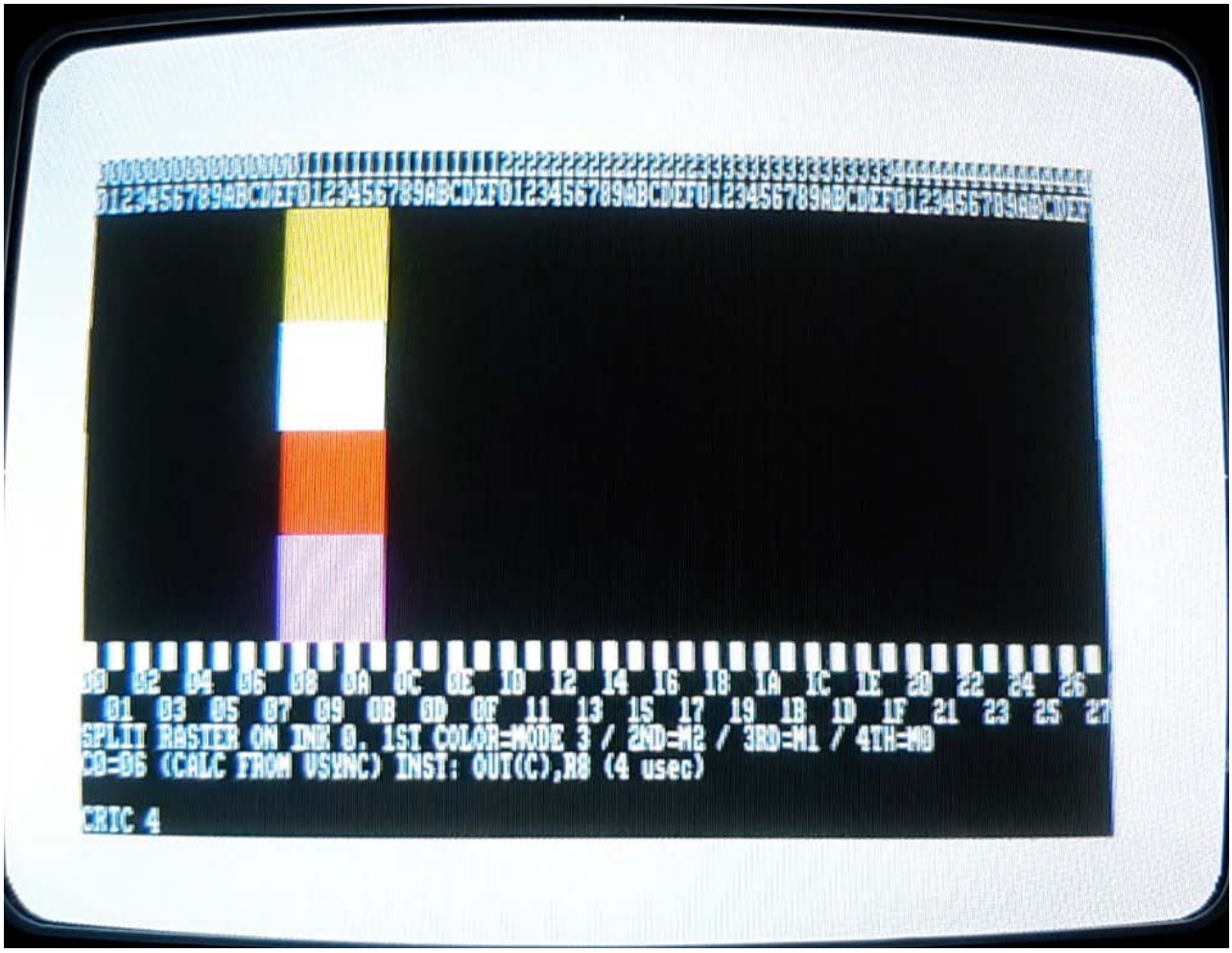
```

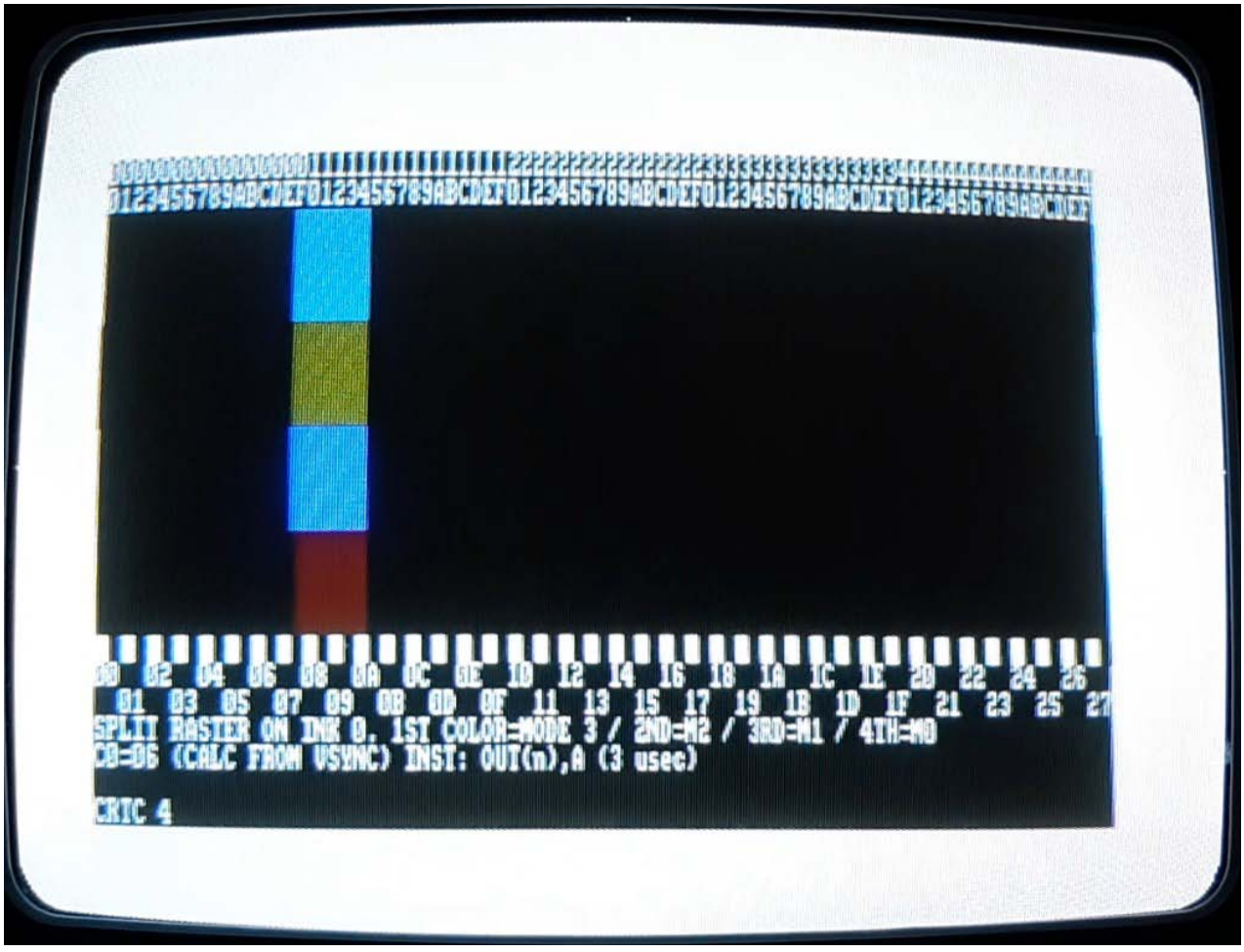


GATE ARRAY INKERISATION

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```




SPLIT RASTER ON INK 0, 1ST COLOR=MODE 3 / 2ND=M2 / 3RD=M1 / 4TH=M0
C0=06 (CALC FROM VSYNC) INST: OUT(C),R8 (4 usec)
CRTC 4

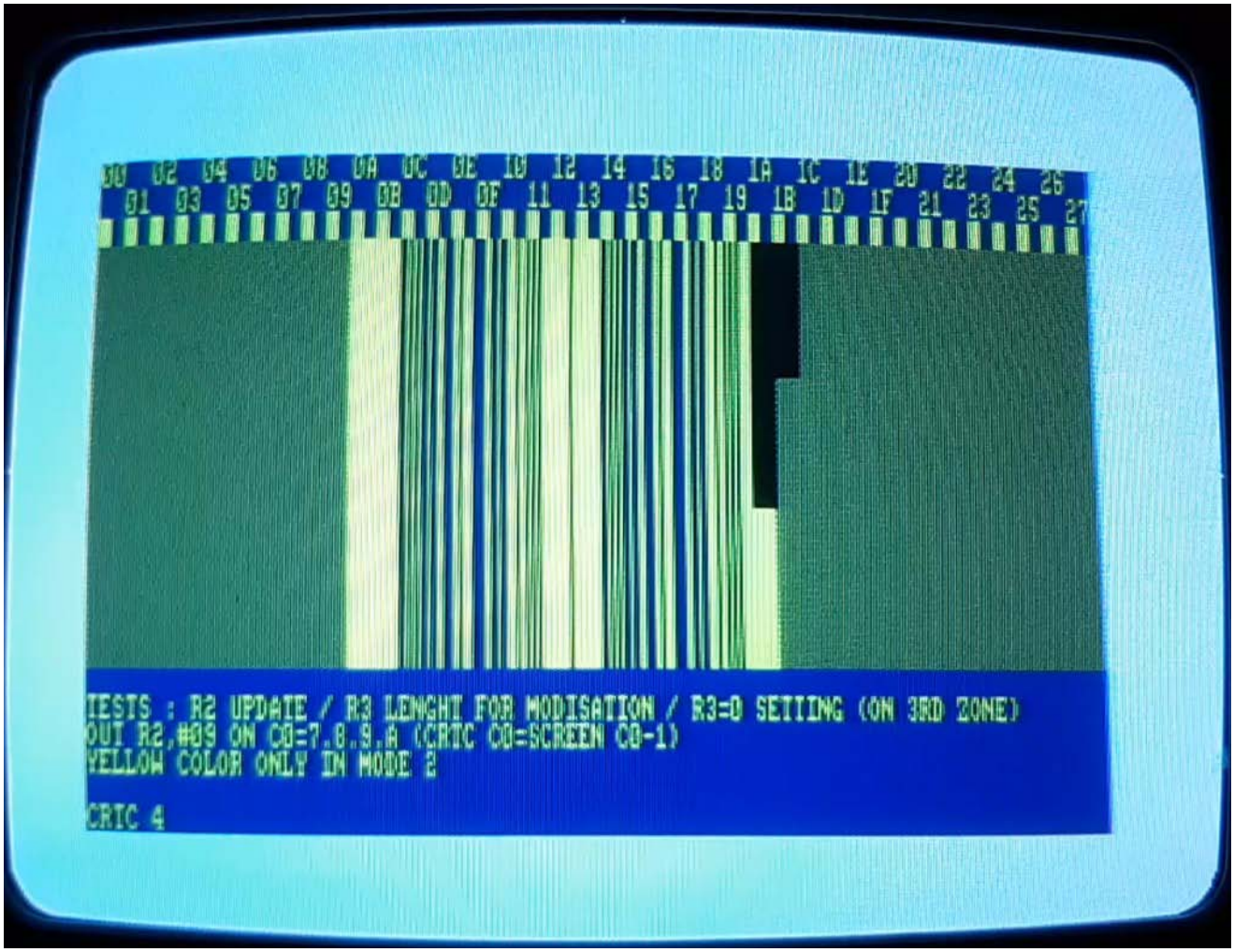

SPLIT RASTER ON INK 0, 1ST COLOR=MODE 3 / 2ND=M2 / 3RD=M1 / 4TH=M0
C0=06 (CALC FROM VSYNC) INST: OUT(n),A (3 usec)
CRTC 4

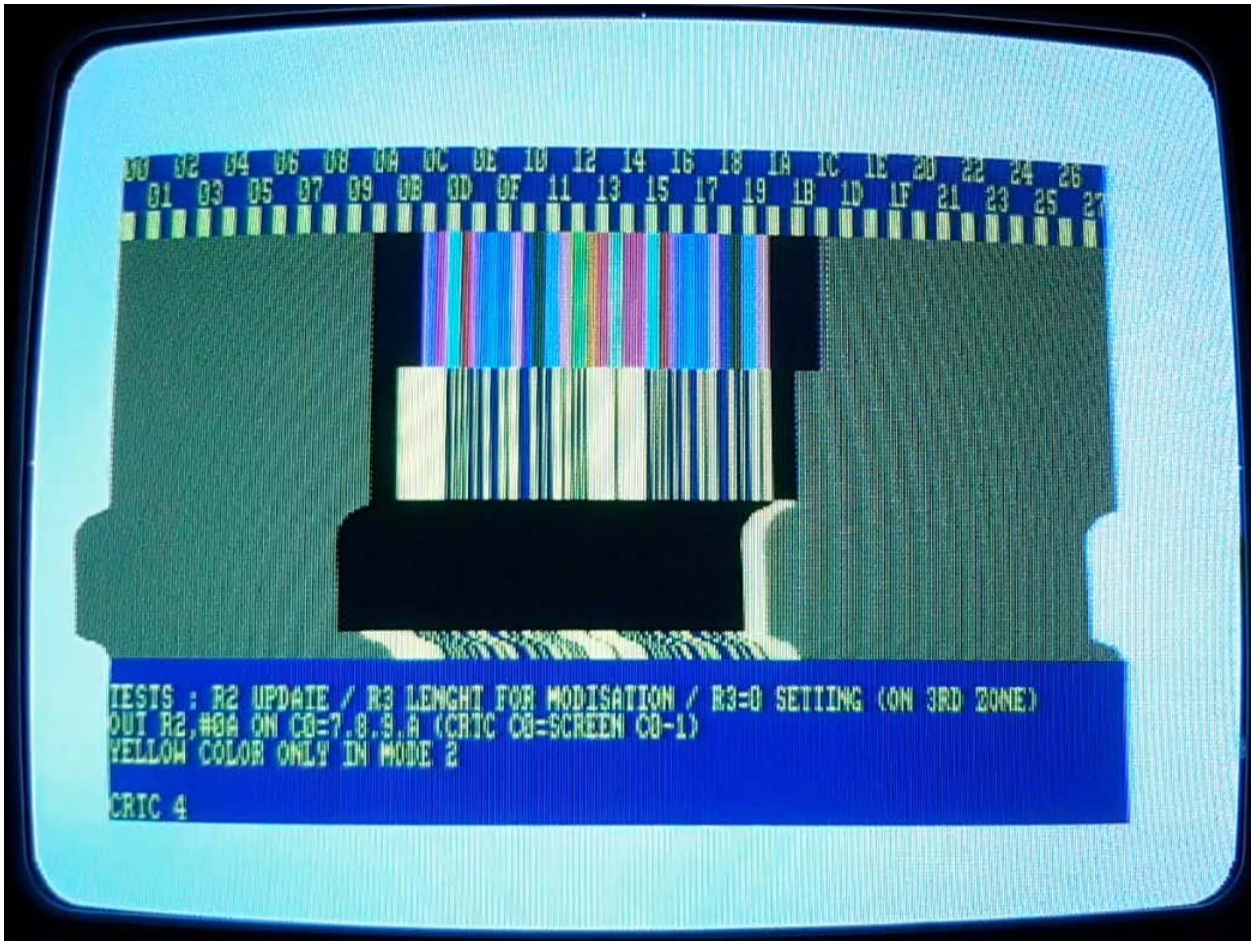
GATE ARRAY MODERISATION

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

HSYNC DELAY ON MODE UPDATE, R2 UPDATE/R3 LENGTH 2 to 0

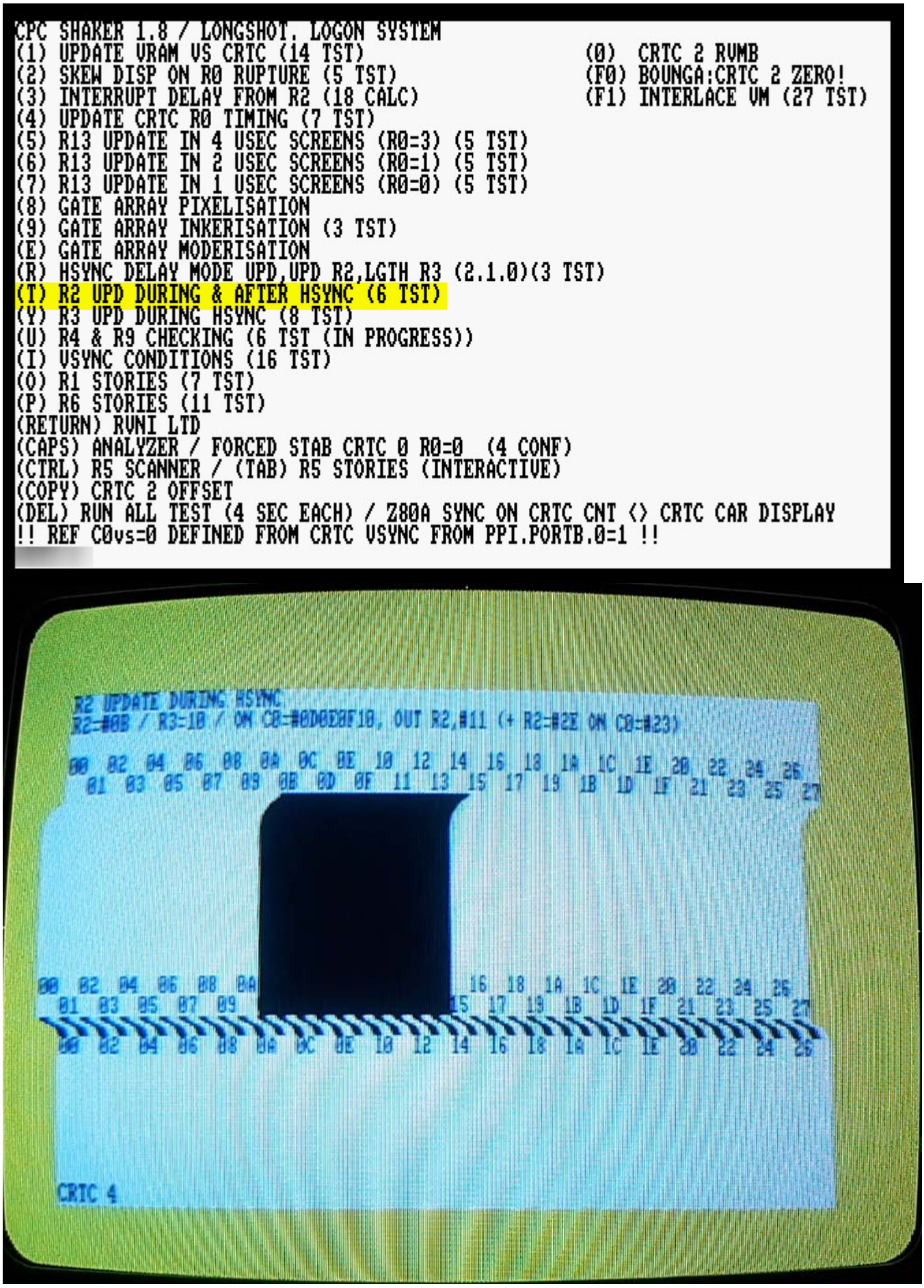
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



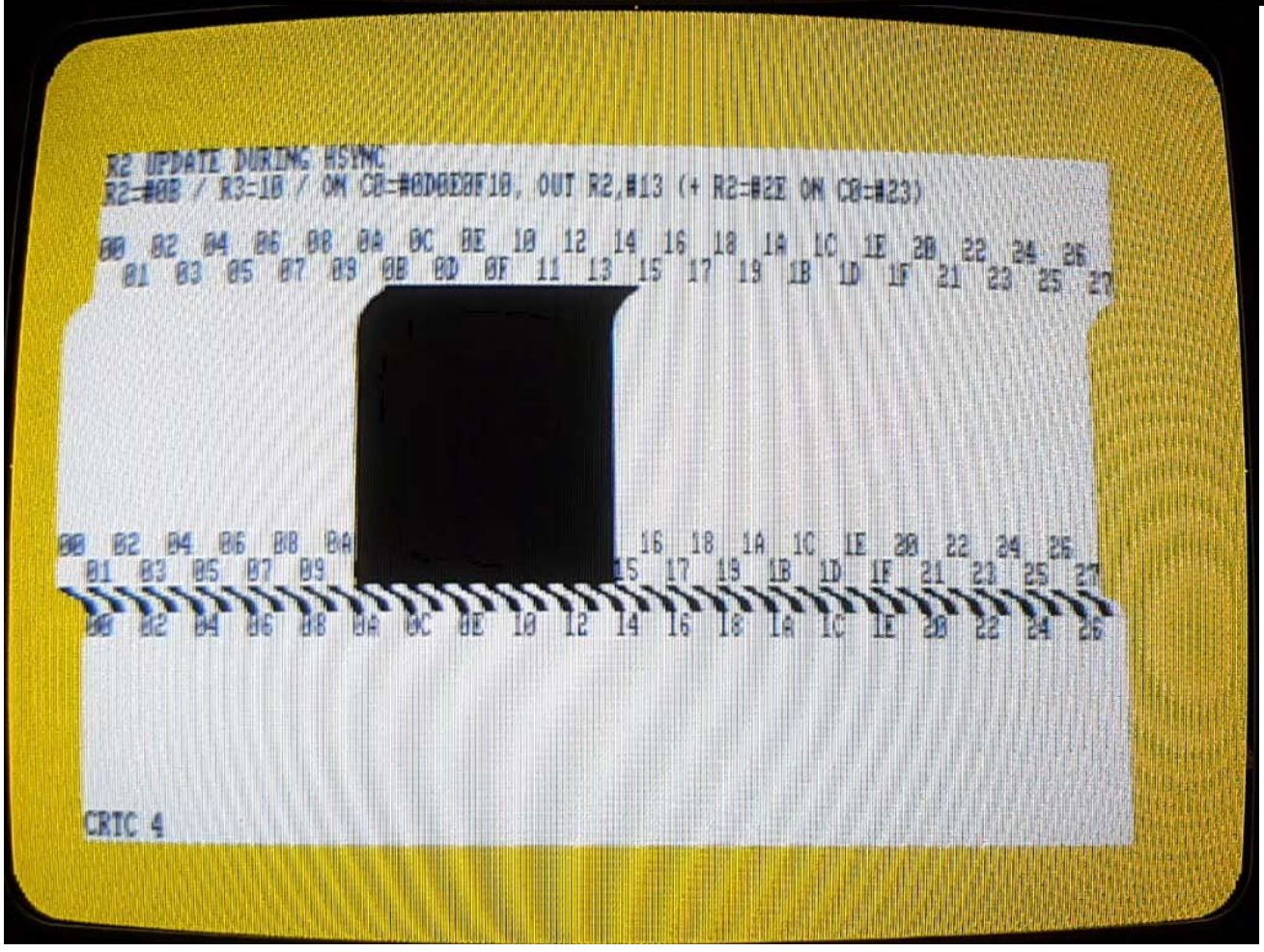

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
TESTS : R2 UPDATE / R3 LENGHT FOR MODISATION / R3=0 SETTING (ON 3RD DONE)
OUT R2,#0A ON C0=7.8.9.A (CRTC C0=SCREEN C0-1)
YELLOW COLOR ONLY IN MODE 2
CRTC 4

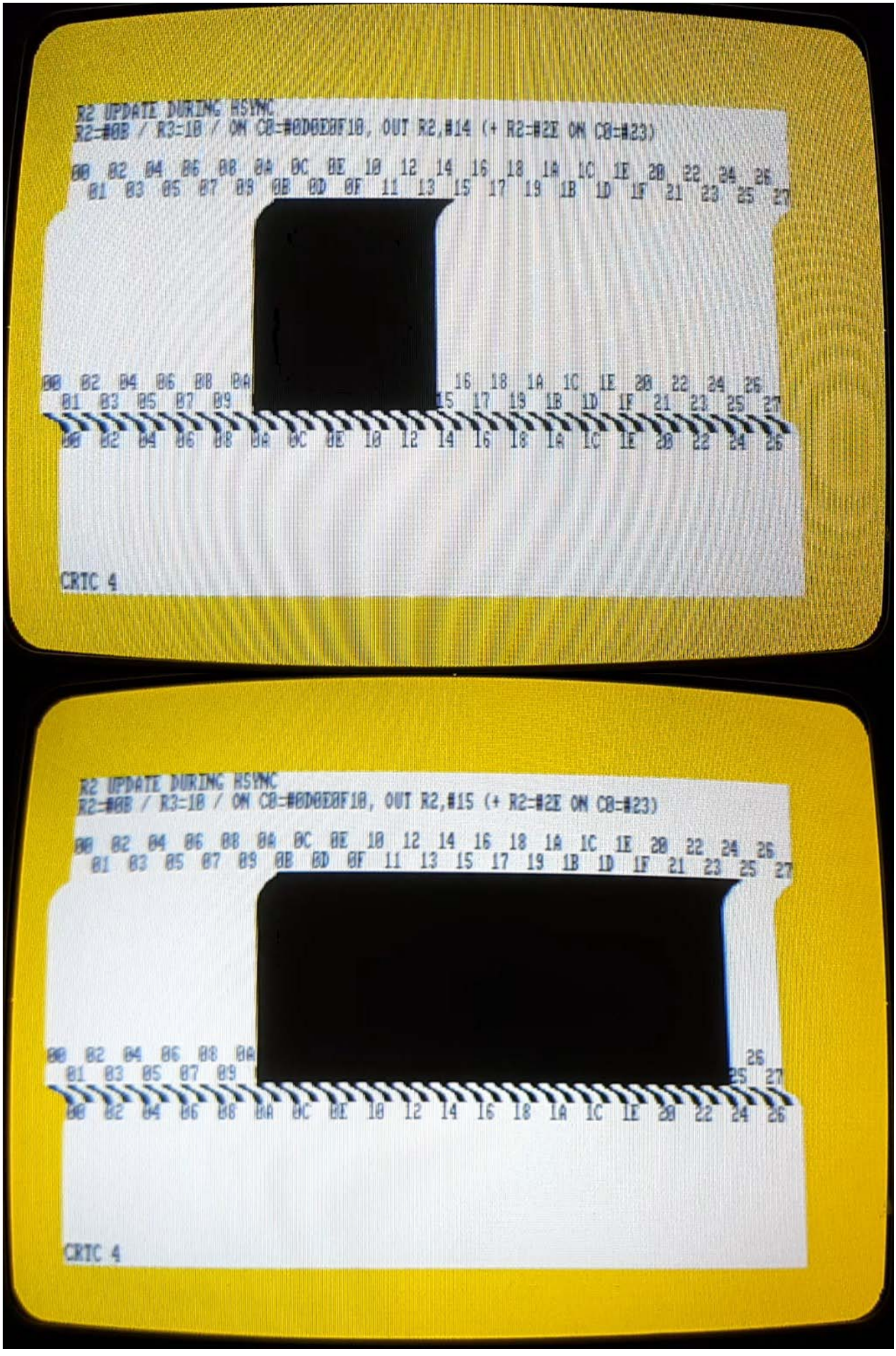

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
TESTS : R2 UPDATE / R3 LENGHT FOR MODISATION / R3=0 SETTING (ON 3RD DONE)
OUT R2,#0B ON C0=7.8.9.A (CRTC C0=SCREEN C0-1)
YELLOW COLOR ONLY IN MODE 2
CRTC 4

R2 UPDATE DURING & AFTER HSYNC




R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CB=#0D0E0F10, OUT R2,#12 (+ R2=#2E ON CB=#23)
CRTC 4

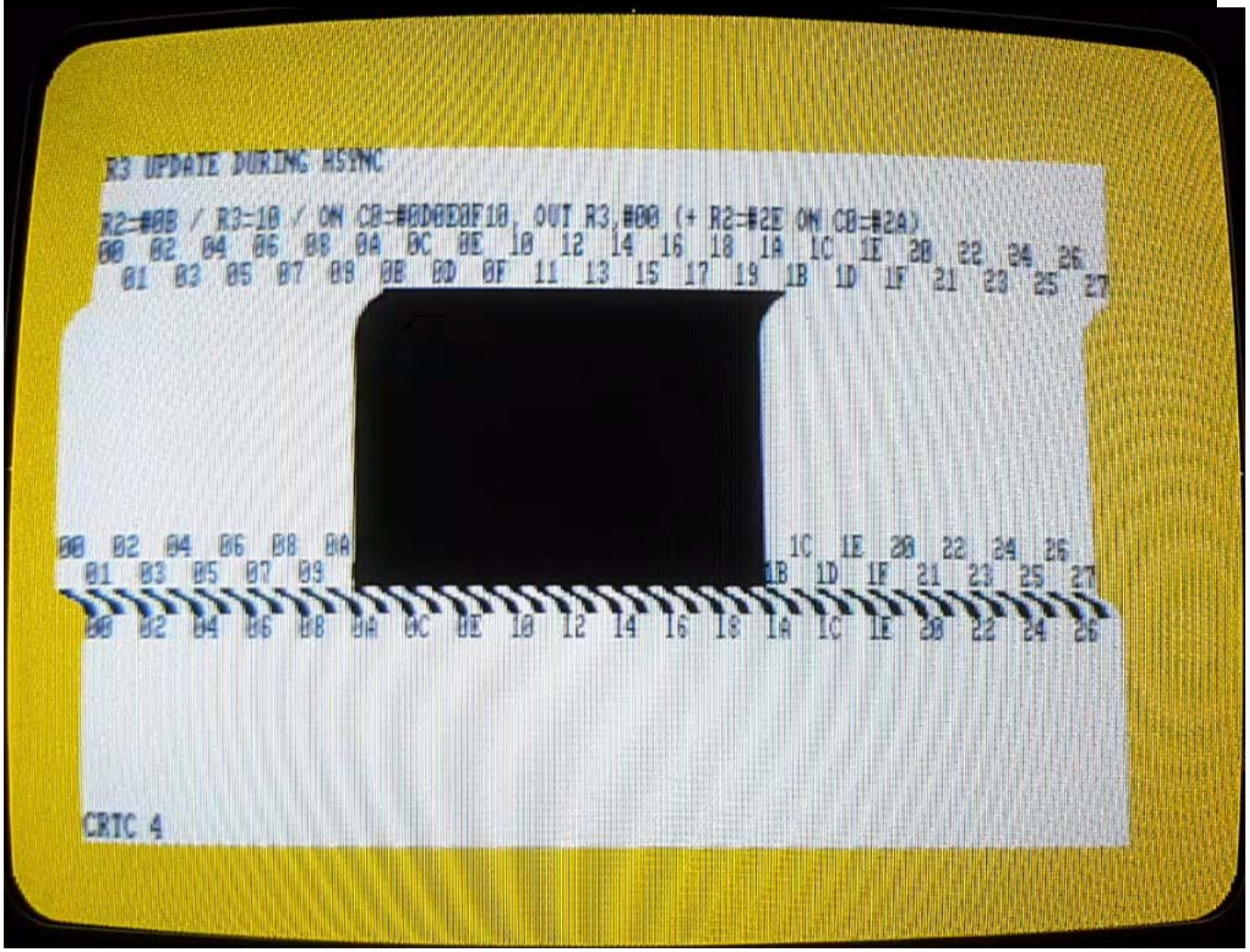

R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CB=#0D0E0F10, OUT R2,#13 (+ R2=#2E ON CB=#23)
CRTC 4

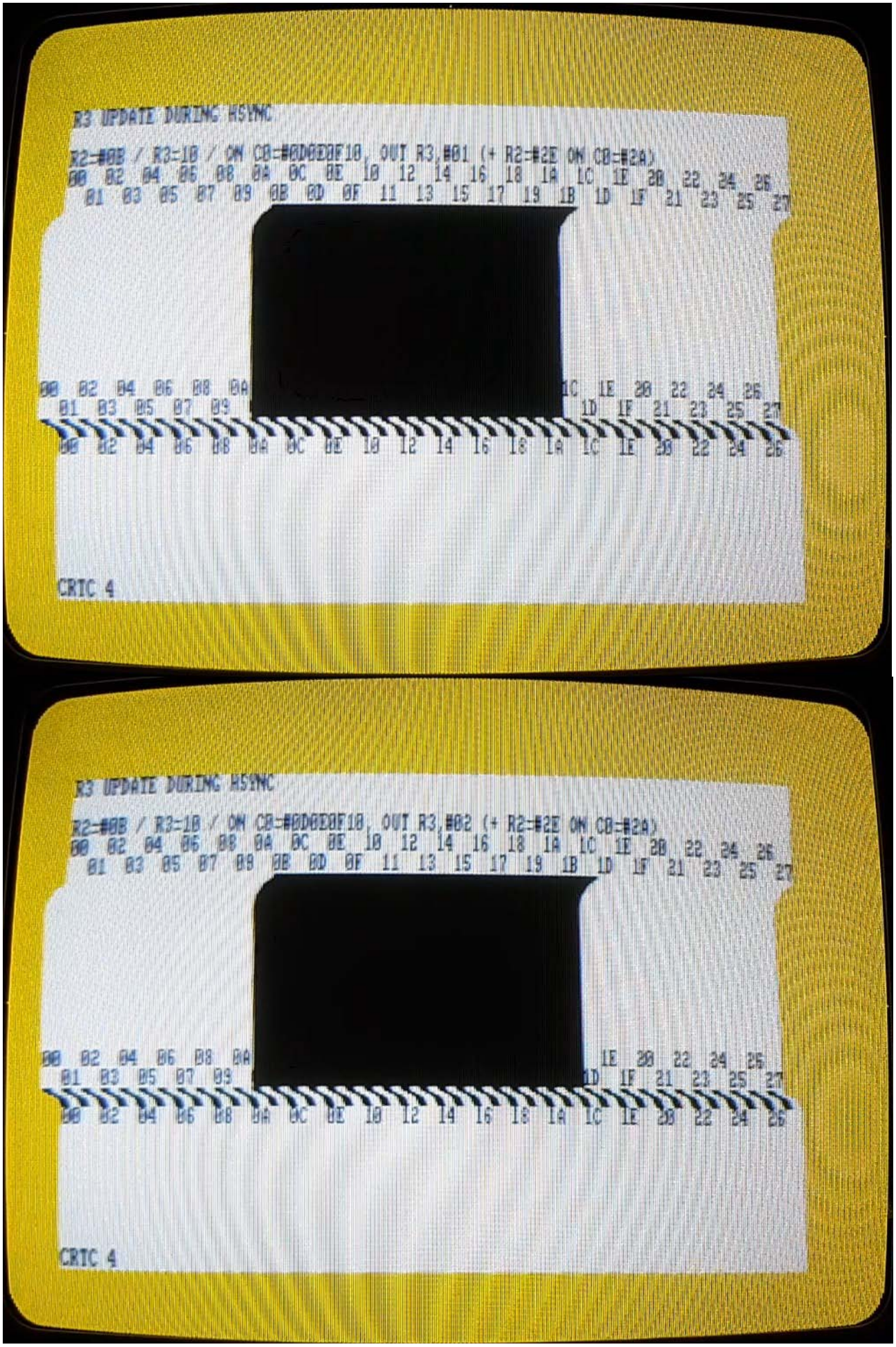

R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#14 (+ R2=#2E ON C0=#23)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 4
R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#15 (+ R2=#2E ON C0=#23)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 4

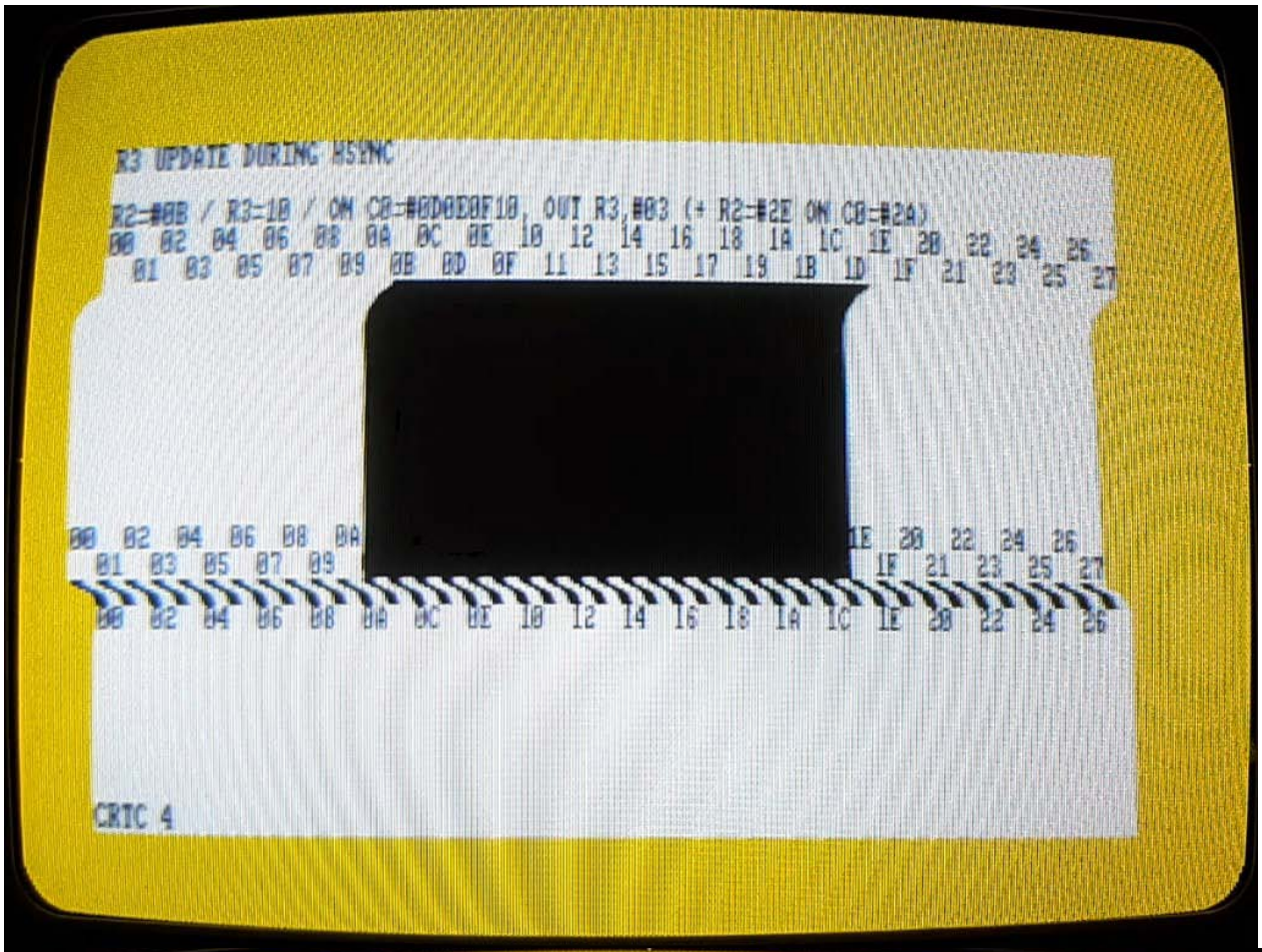

R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#16 (+ R2=#2E ON C0=#23)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

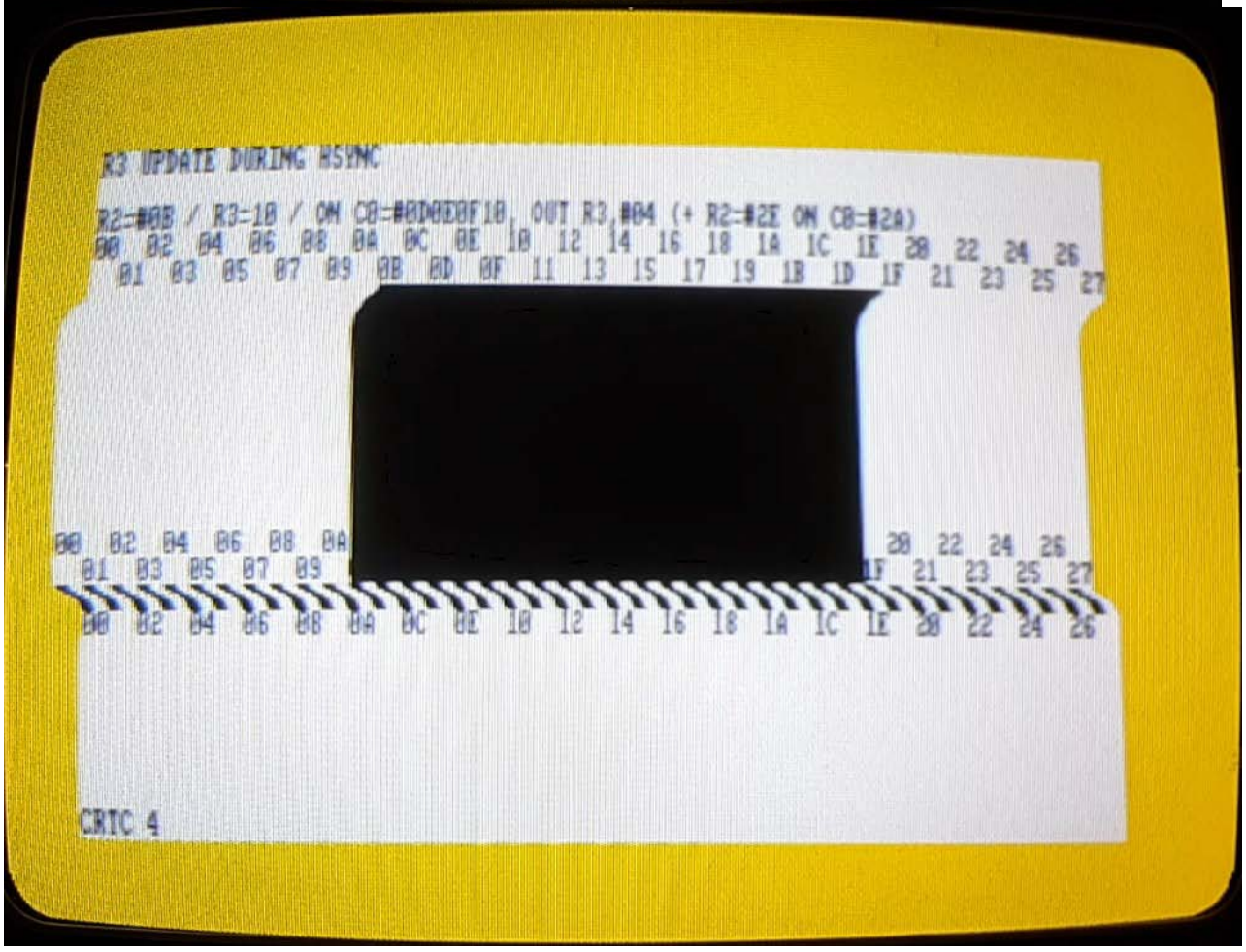
R3 UPDATE DURING HSYNC

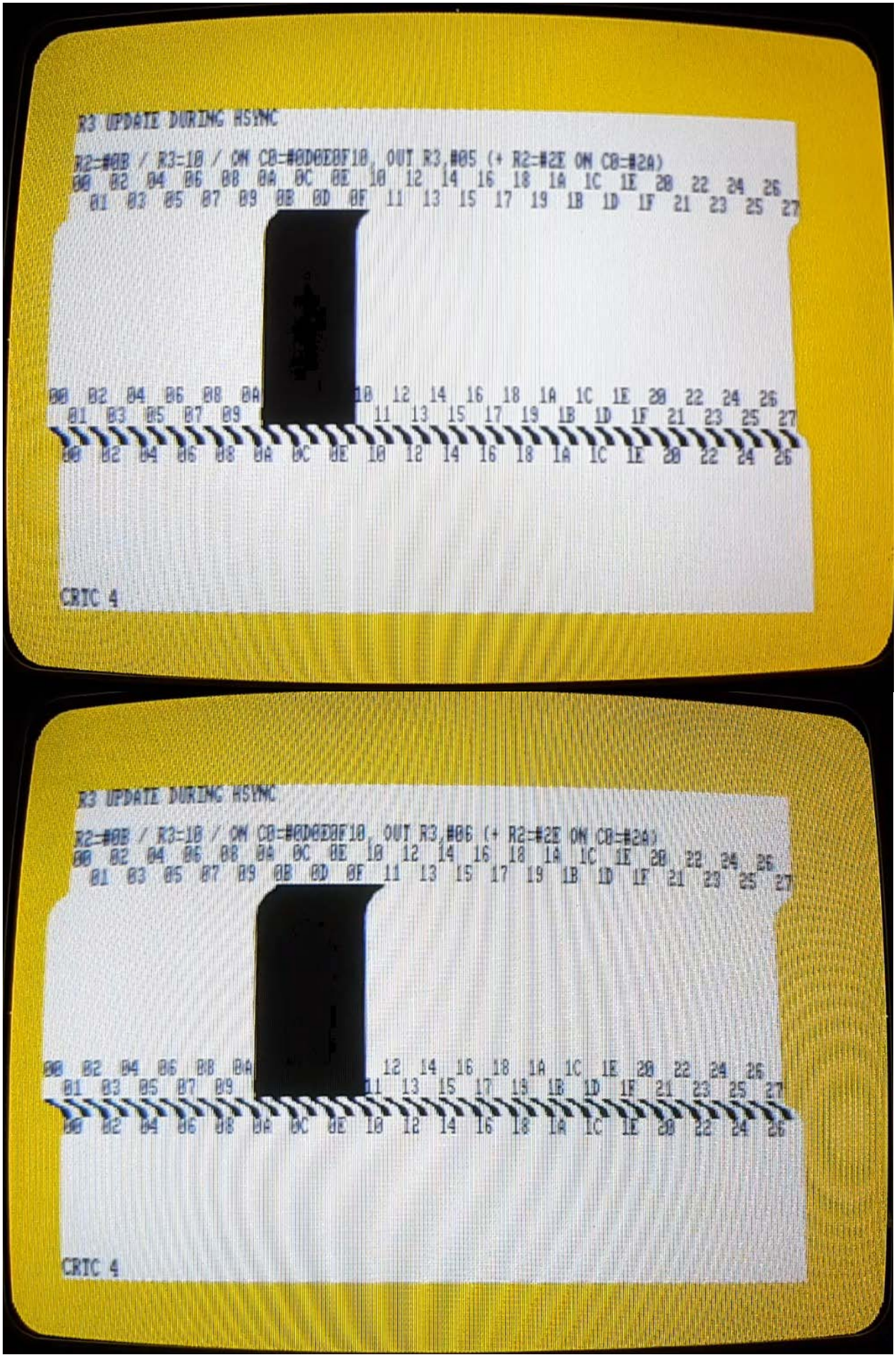
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

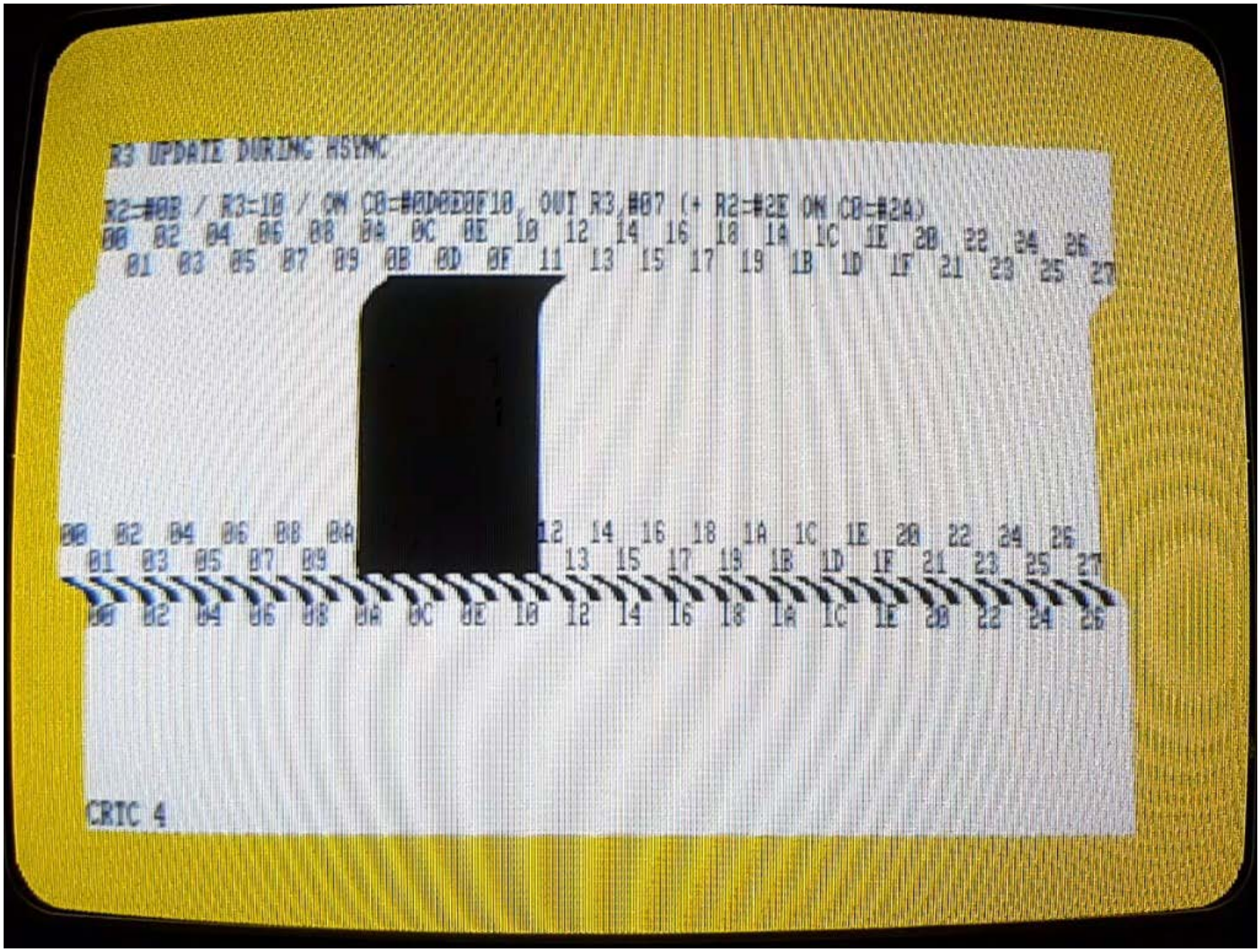



R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / CM CB=#0D0E0F10, OUT R3,#01 (+ R2=#2E ON CB=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 4
R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / CM CB=#0D0E0F10, OUT R3,#02 (+ R2=#2E ON CB=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 4


R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#03 (+ R2=#2E ON C0=#2A)
CRTC 4

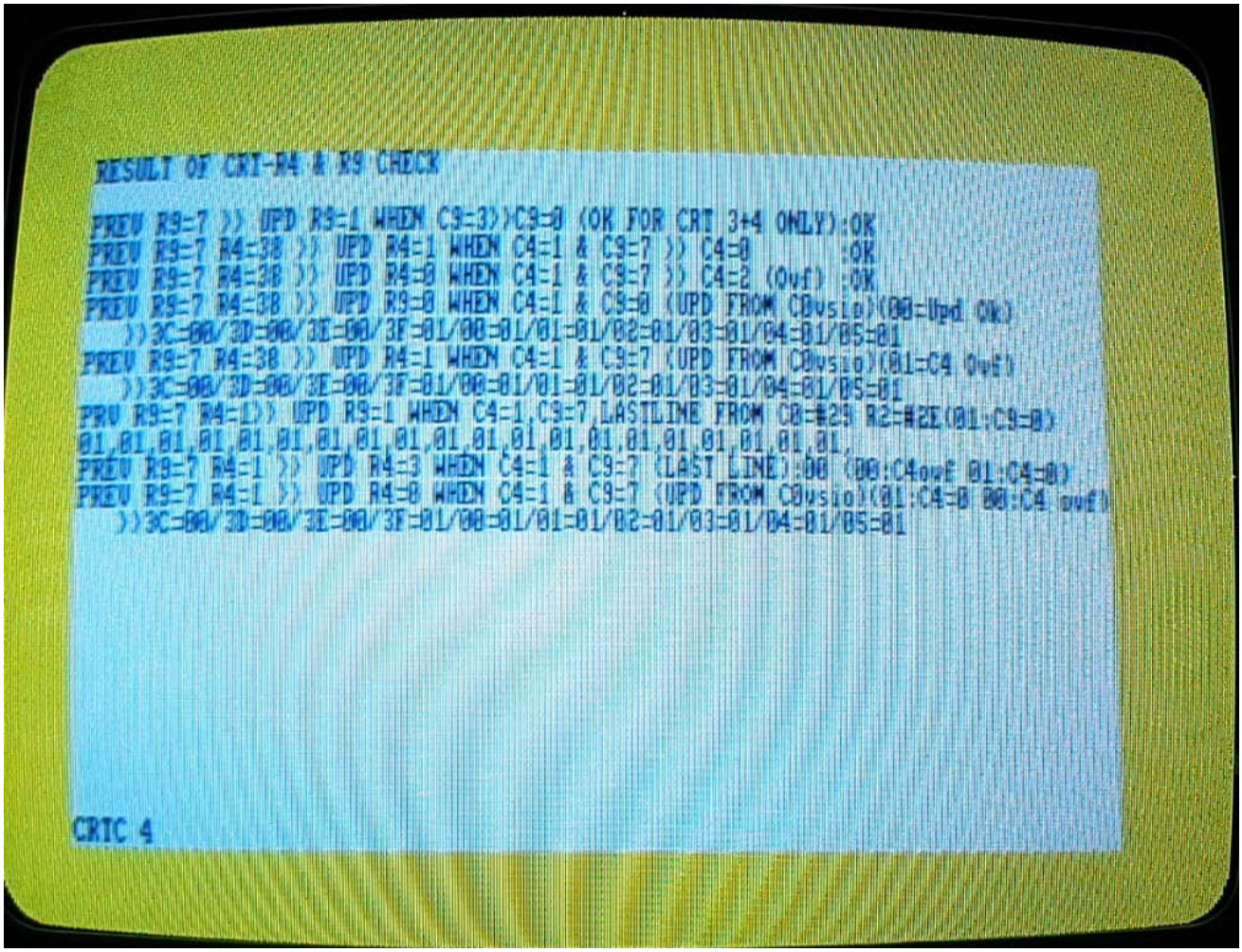

R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#04 (+ R2=#2E ON C0=#2A)
CRTC 4


R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / CM CB=#0D0E0F10, OUT R3,#05 (+ R2=#2E ON CB=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 4
R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / CM CB=#0D0E0F10, OUT R3,#06 (+ R2=#2E ON CB=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 4


R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#07 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
CRTC 4

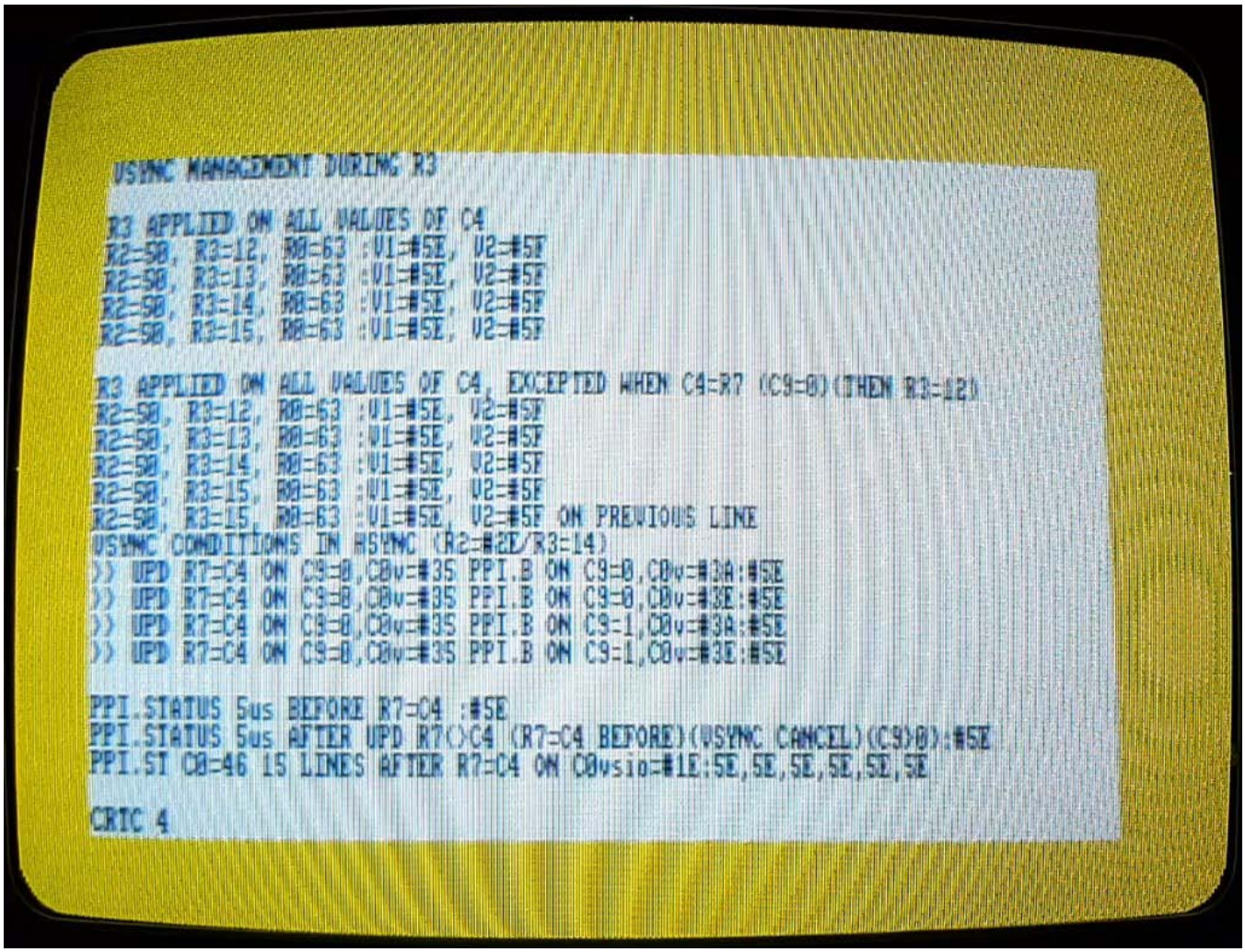
R4 & R9 CHECKING

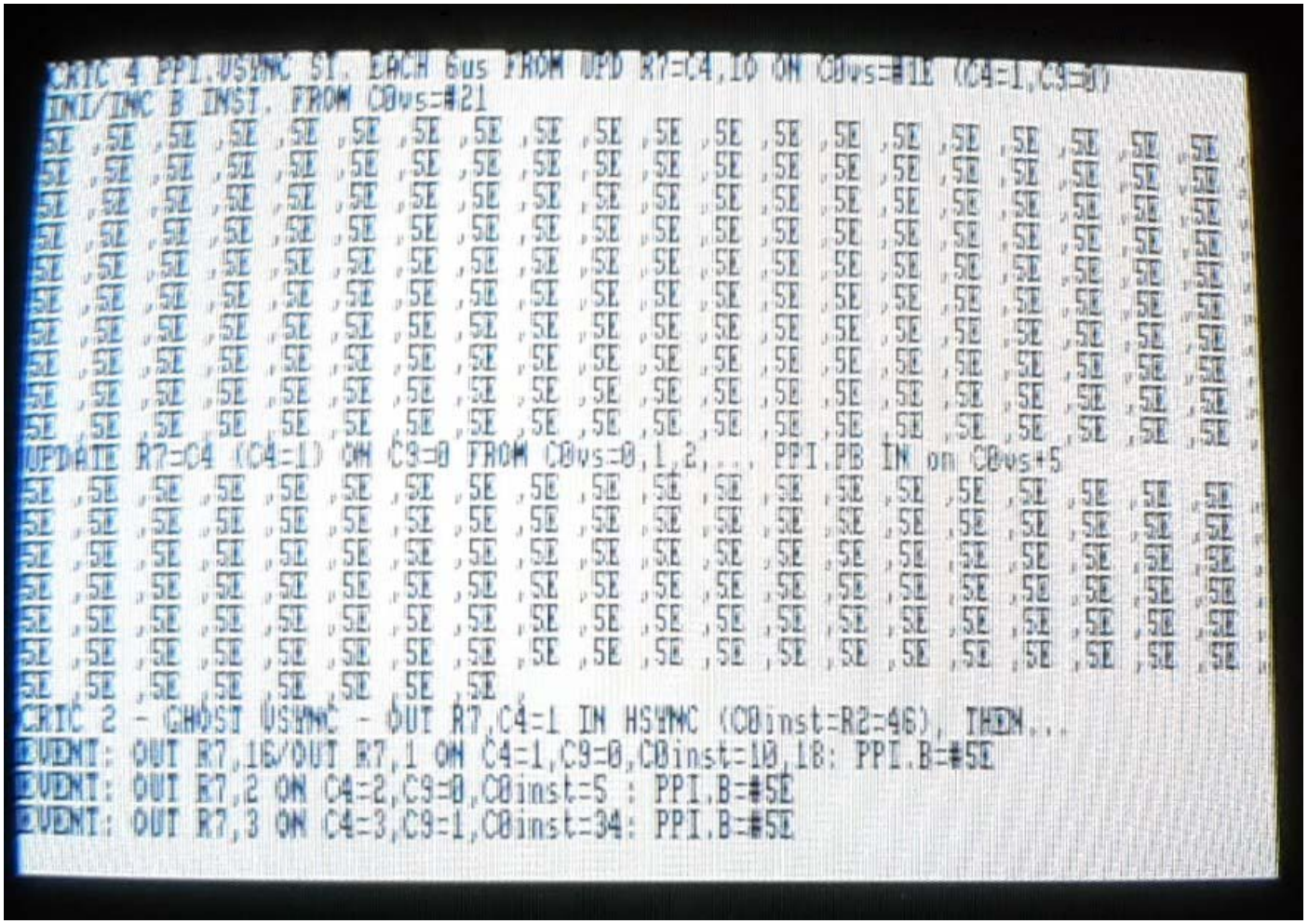
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



VSYNC CONDITIONS

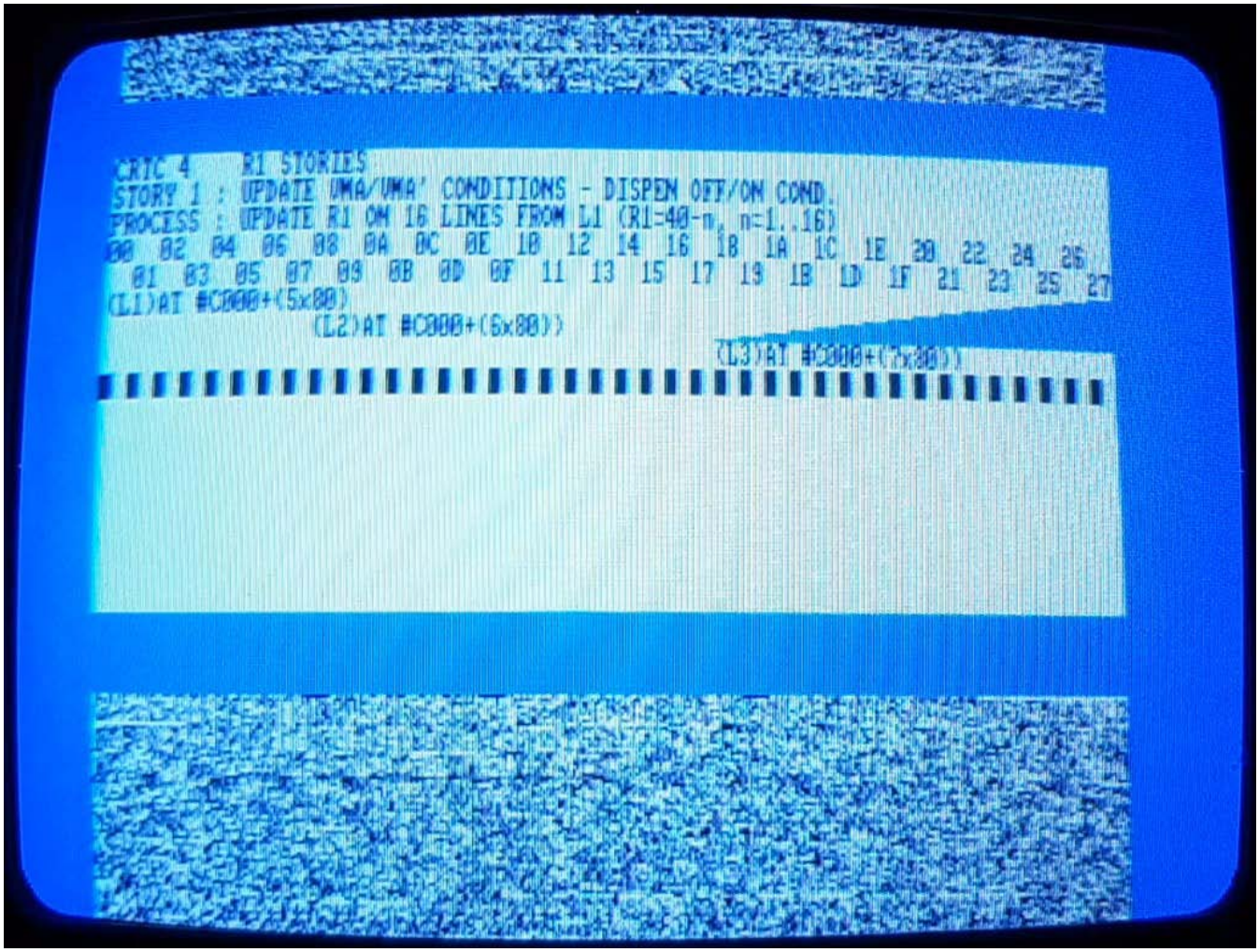
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

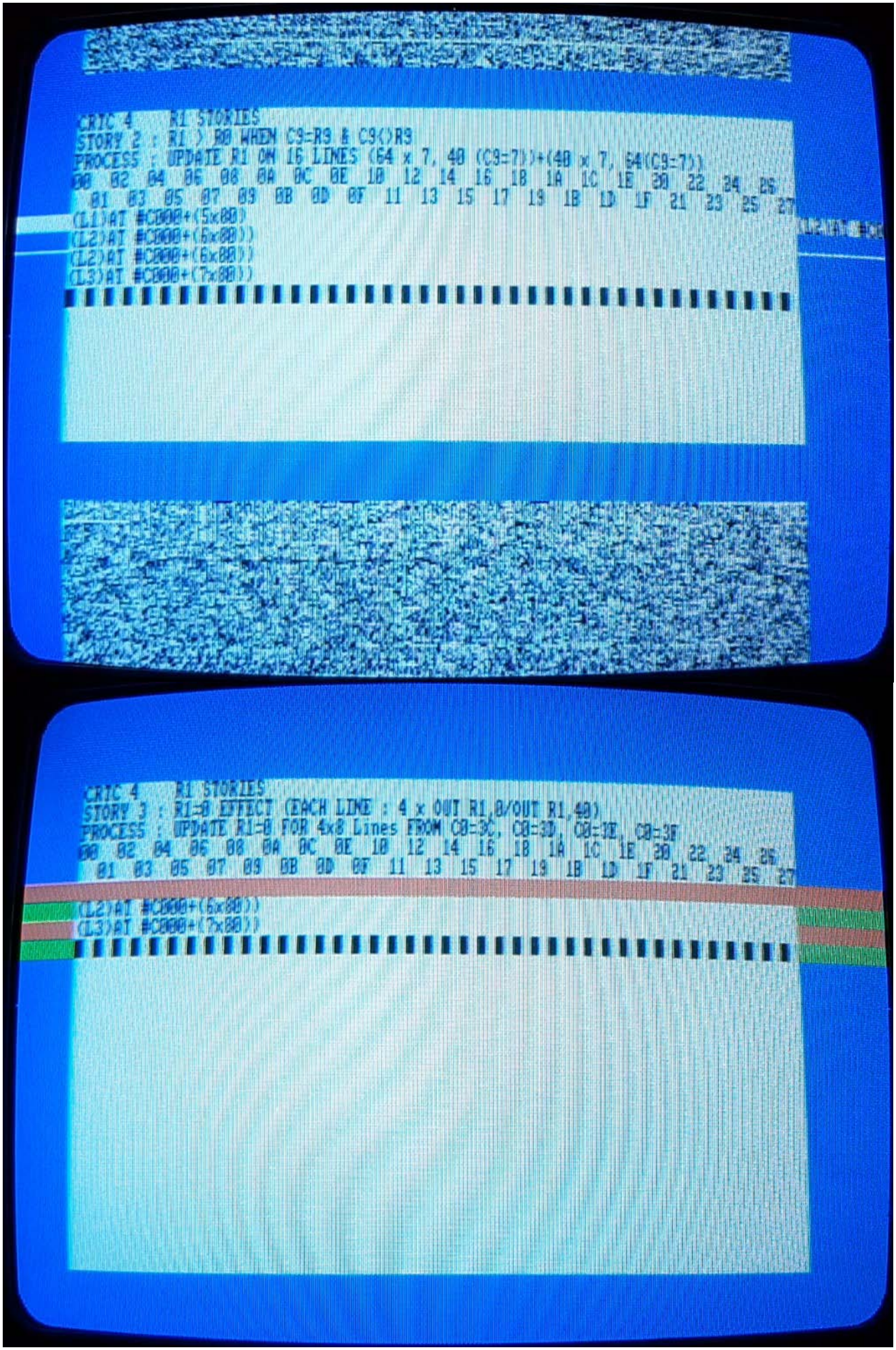


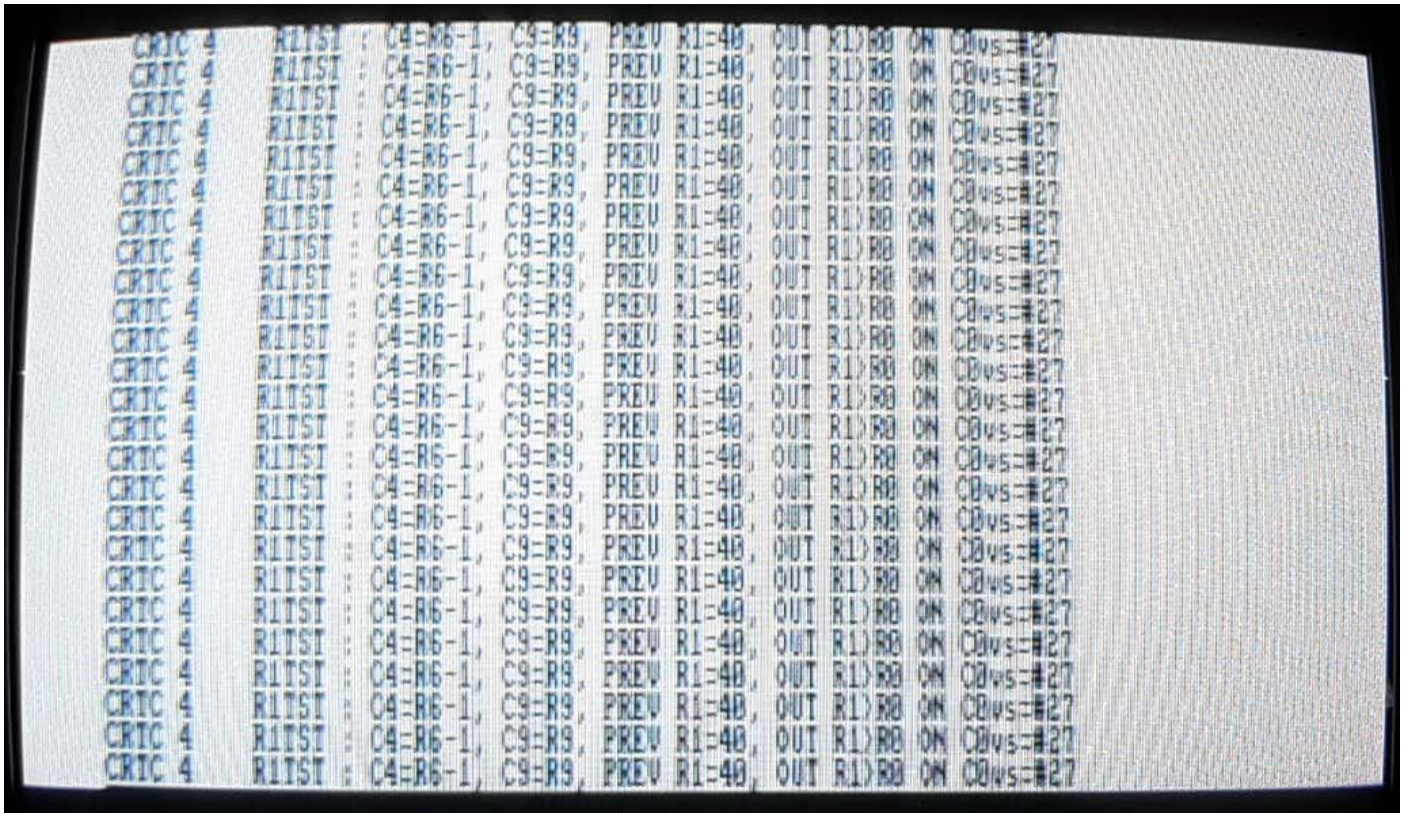

CRIC 4 PPI.USYNC SI. EACH 6us FROM UPD R7=C4,10 ON C0vs=#1E (C4=1,C9=0)
UNI/IMC B INST. FROM C0vs=#21
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
UPDATE R7=C4 (C4=1) ON C9=0 FROM C0vs=0,1,2,... PPI.PB IN on C0vs+5
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
5E ,5E ,5E ,5E ,5E ,5E ,5E ,5E
CRIC 2 - GHOST USYNC - OUT R7,C4=1 IN HSYNC (C0inst=R2=46), THEN...
EVENT: OUT R7,16/OUT R7,1 ON C4=1,C9=0,C0inst=10,18: PPI.B=#5E
EVENT: OUT R7,2 ON C4=2,C9=0,C0inst=5 : PPI.B=#5E
EVENT: OUT R7,3 ON C4=3,C9=1,C0inst=34: PPI.B=#5E

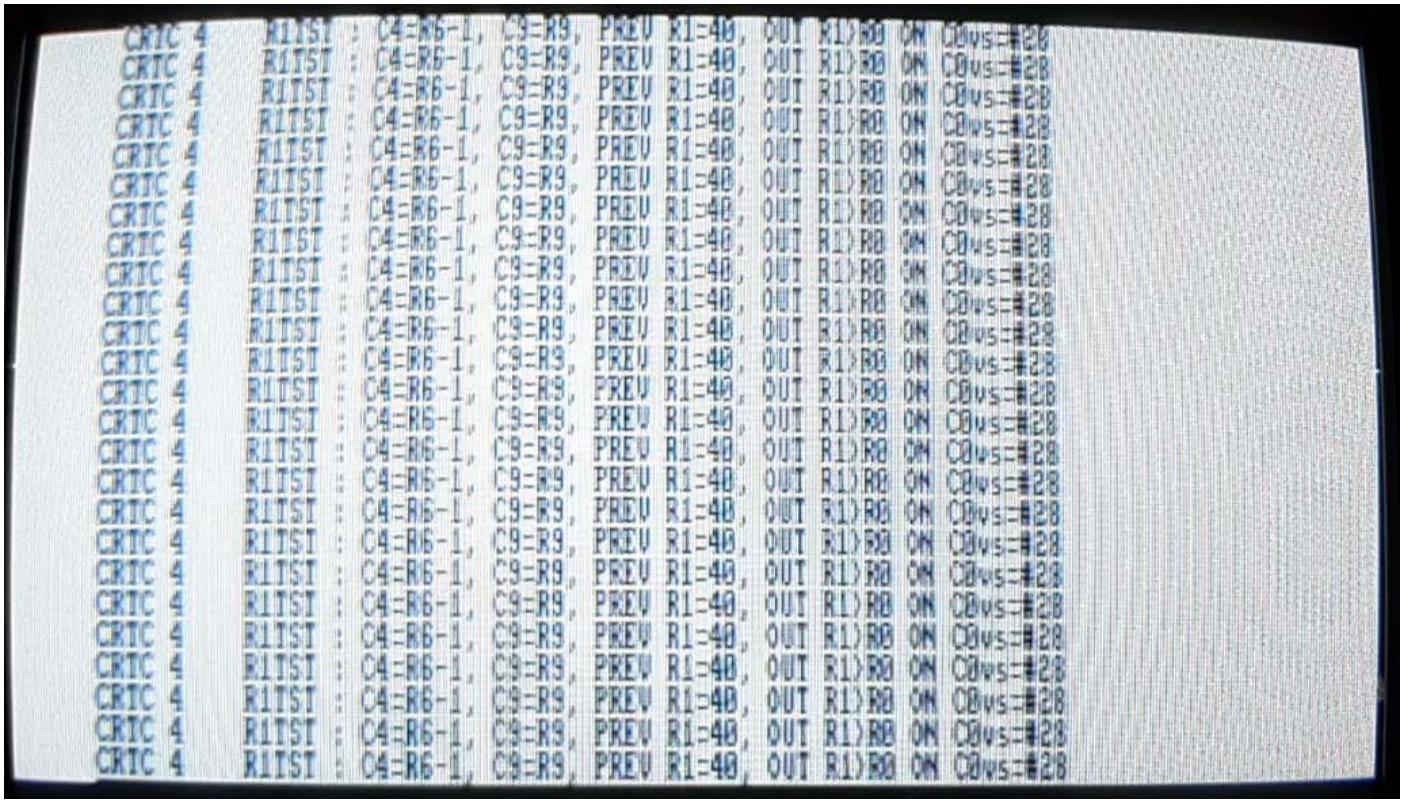
R1 STORIES

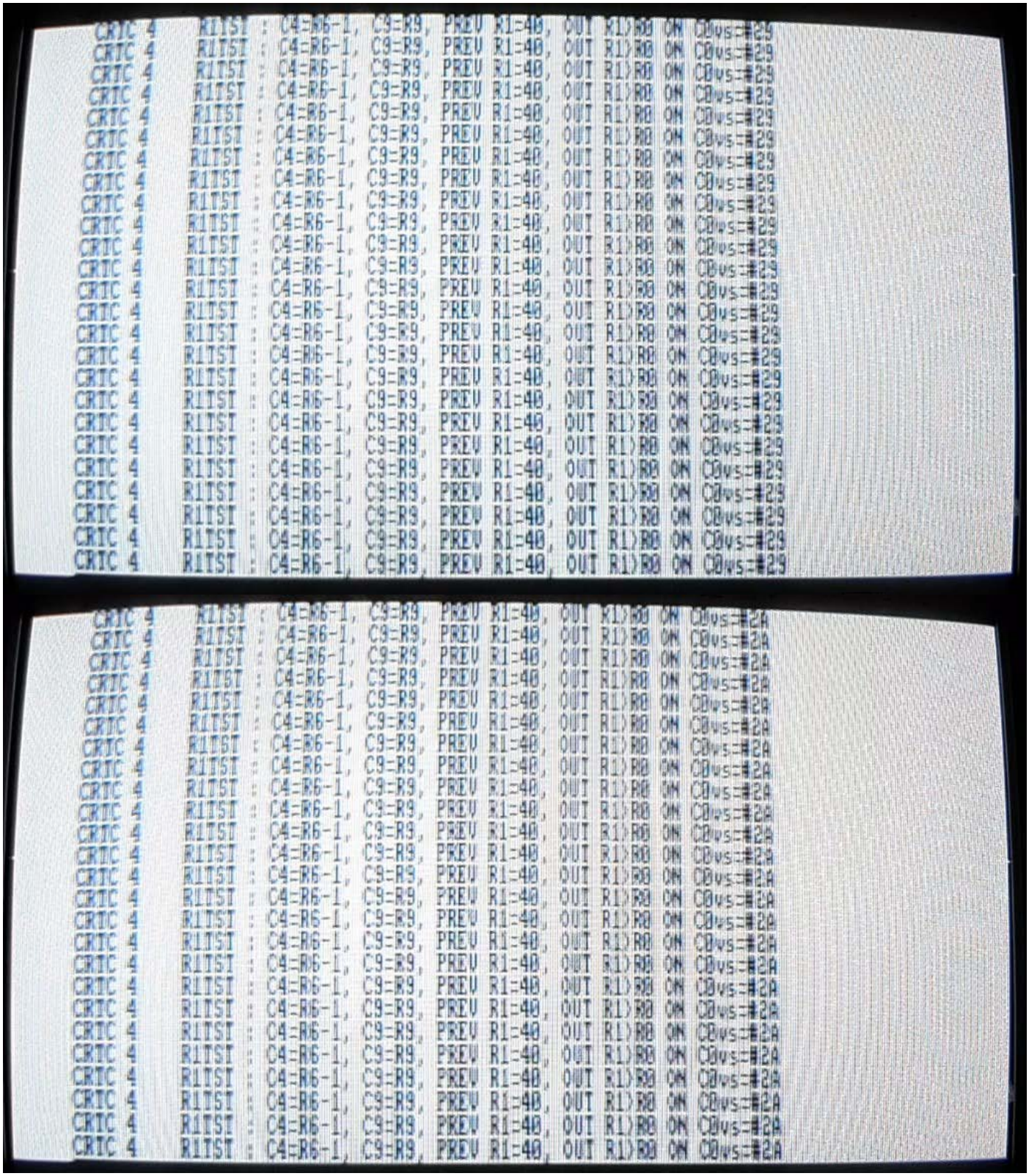
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



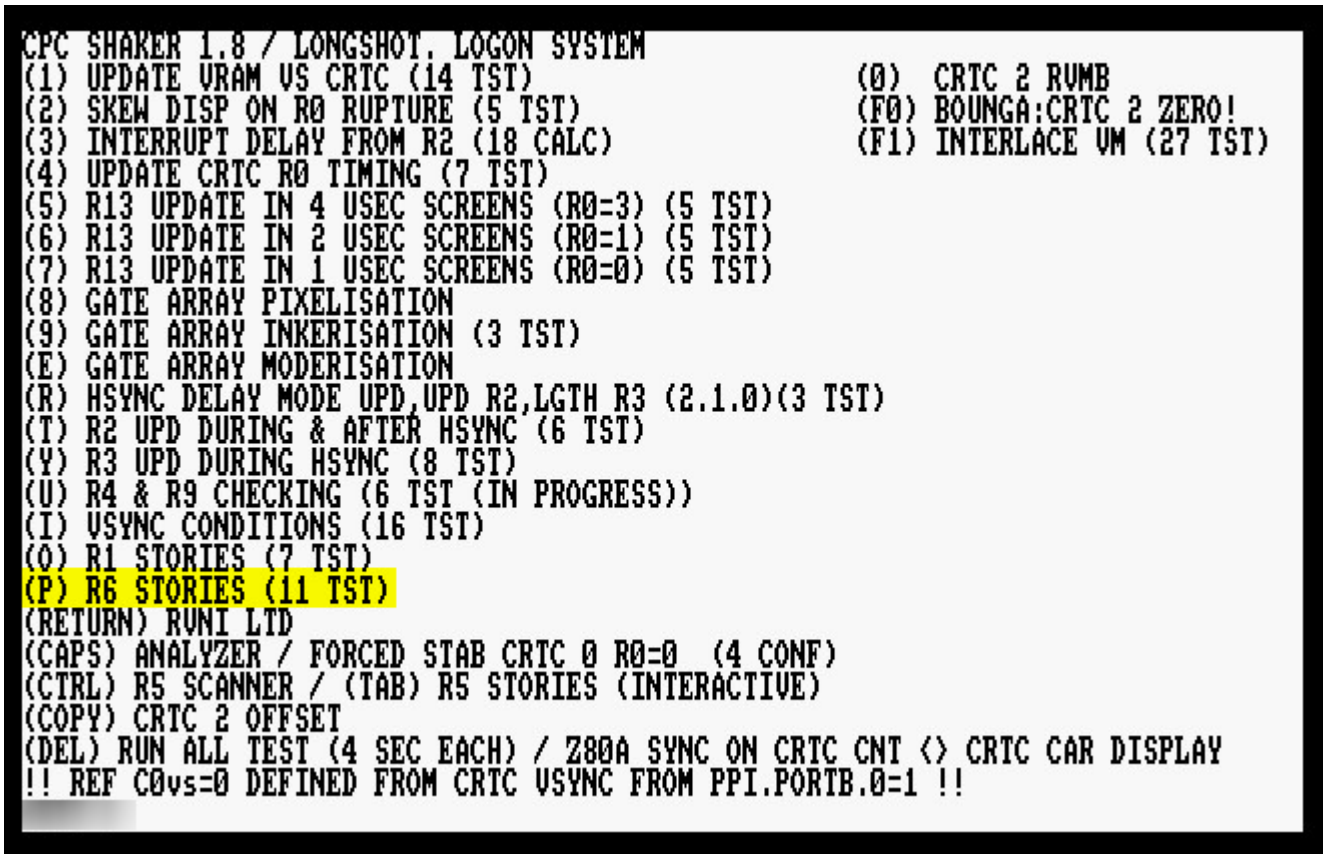

CRTC 4 R1 STORIES
STORY 2 : R1) R0 WHEN C9=R9 & C9()R9
PROCESS : UPDATE R1 ON 16 LINES (64 x 7, 40 (C9=7))+(40 x 7, 64(C9=7))
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
(L1)AT #C000+(5x80)
(L2)AT #C000+(6x80))
(L2)AT #C000+(6x80))
(L3)AT #C000+(7x80))
CRTC 4 R1 STORIES
STORY 3 : R1=0 EFFECT (EACH LINE : 4 x OUT R1,0/OUT R1,40)
PROCESS : UPDATE R1=0 FOR 4x8 Lines FROM C0=0C, C0=3D, C0=3E, C0=3F
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
(L2)AT #C000+(6x80))
(L3)AT #C000+(7x80))

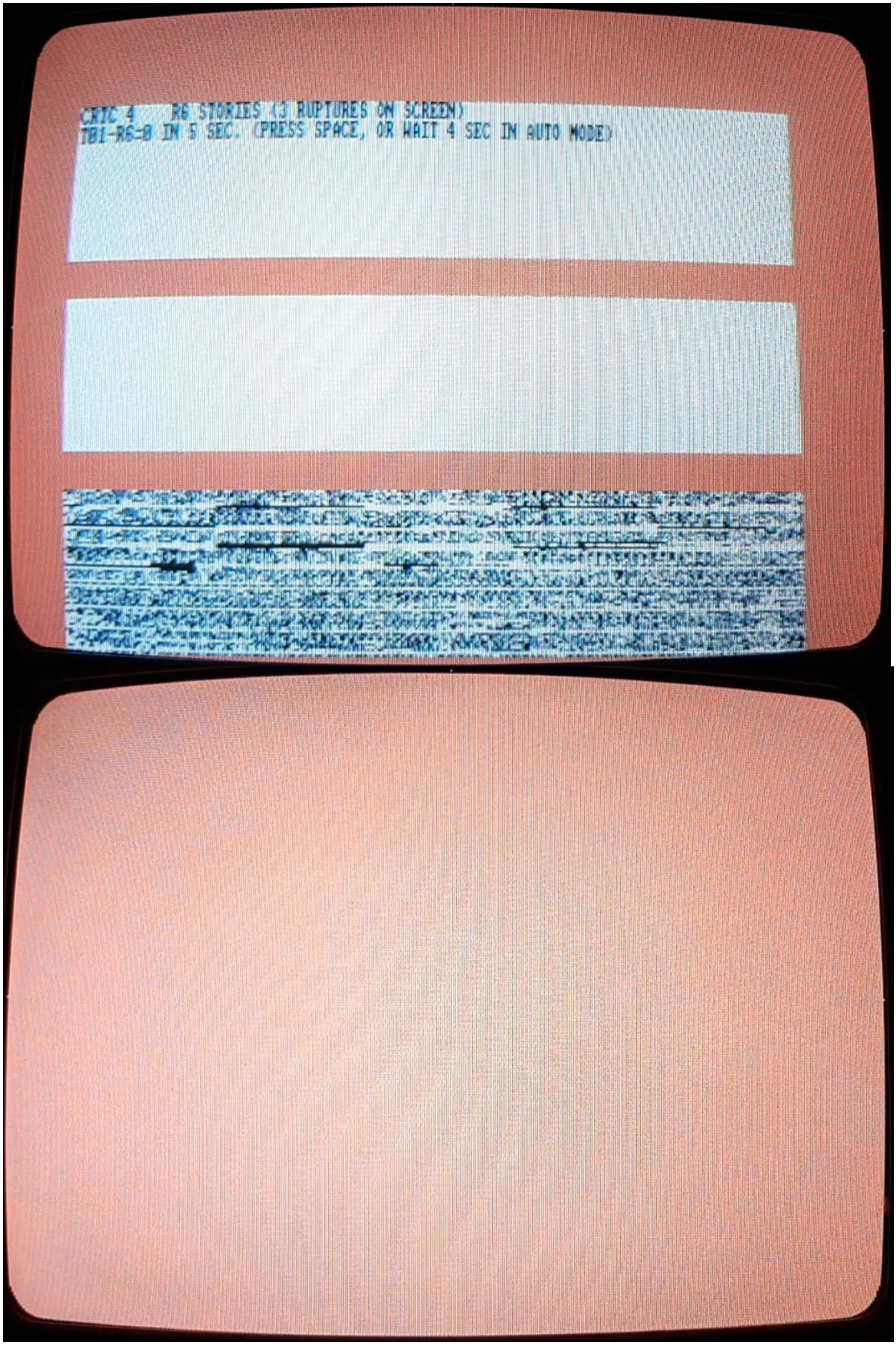

CRTC 4 R1TST : C4=R6-1, C9=R9, PREV R1=40, OUT R1)R0 ON C0vs=#27

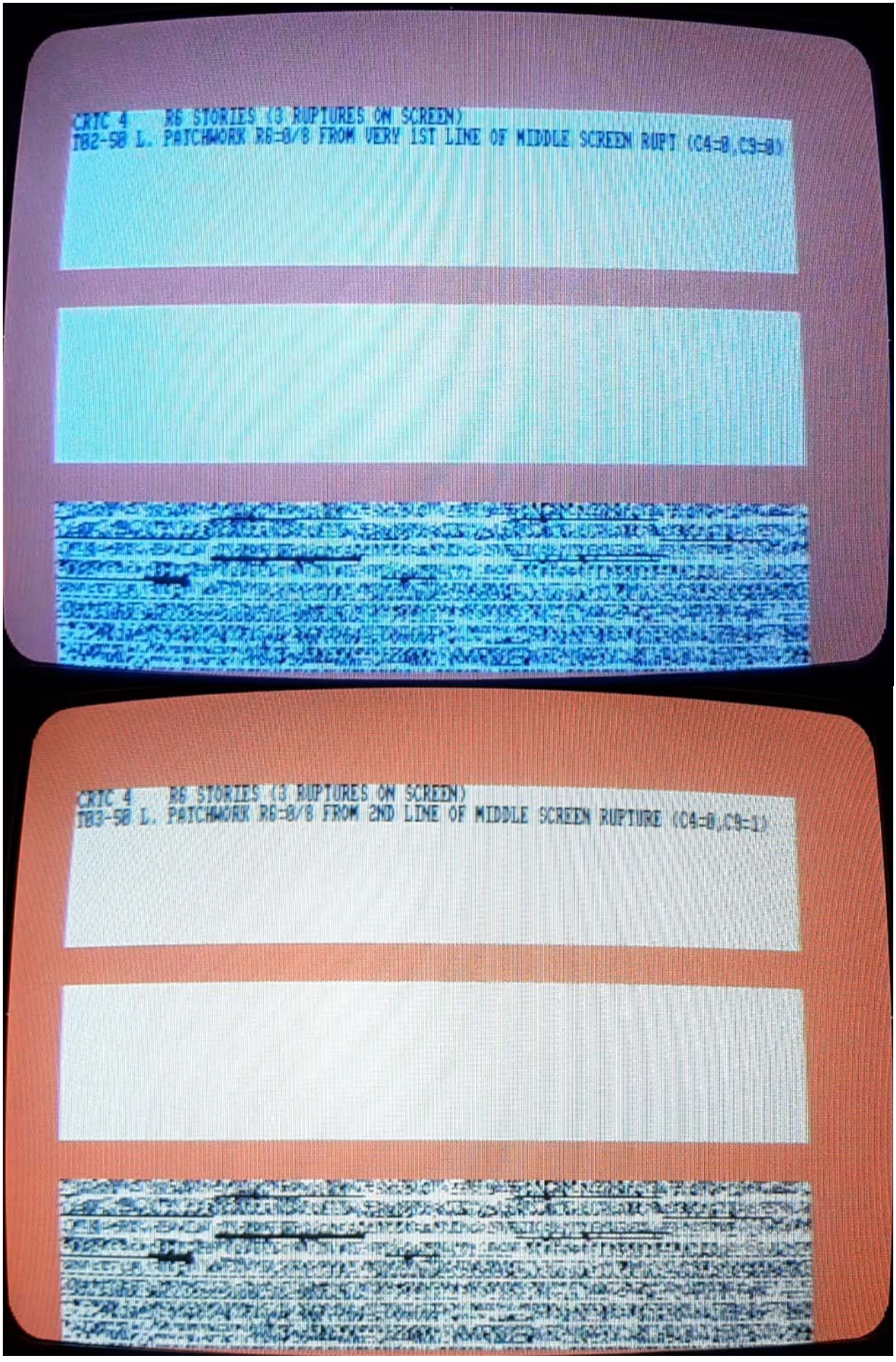

CRTC 4 R1TST : C4=R6-1, C9=R9, PREV R1=40, OUT R1)R0 ON C0vs=#28

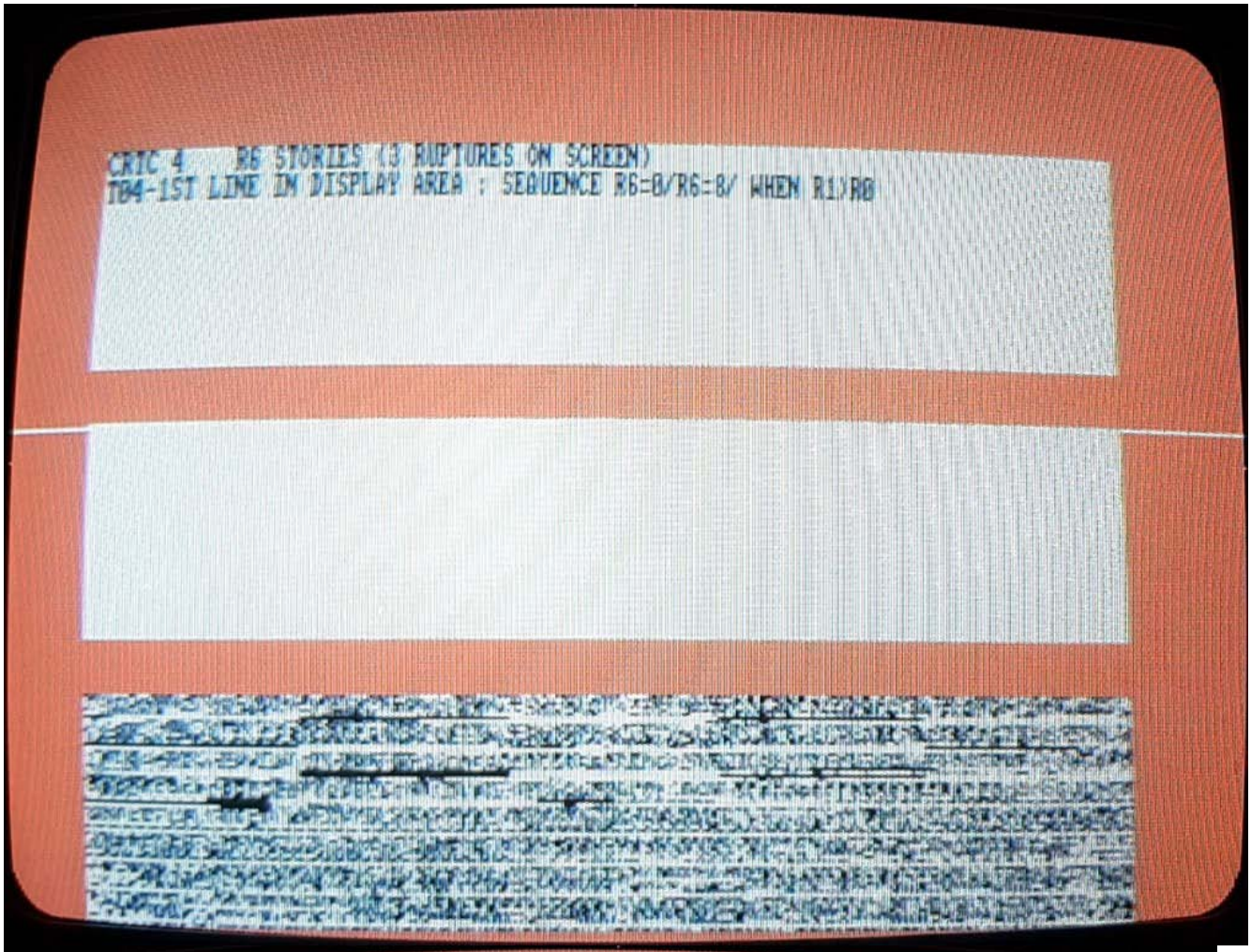

CRTC 4 R1TST : C4=R6-1, C9=R9, PREV R1=40, OUT R1)R0 ON C0vs=#29
CRTC 4 R1TST : C4=R6-1, C9=R9, PREV R1=40, OUT R1)R0 ON C0vs=#2A

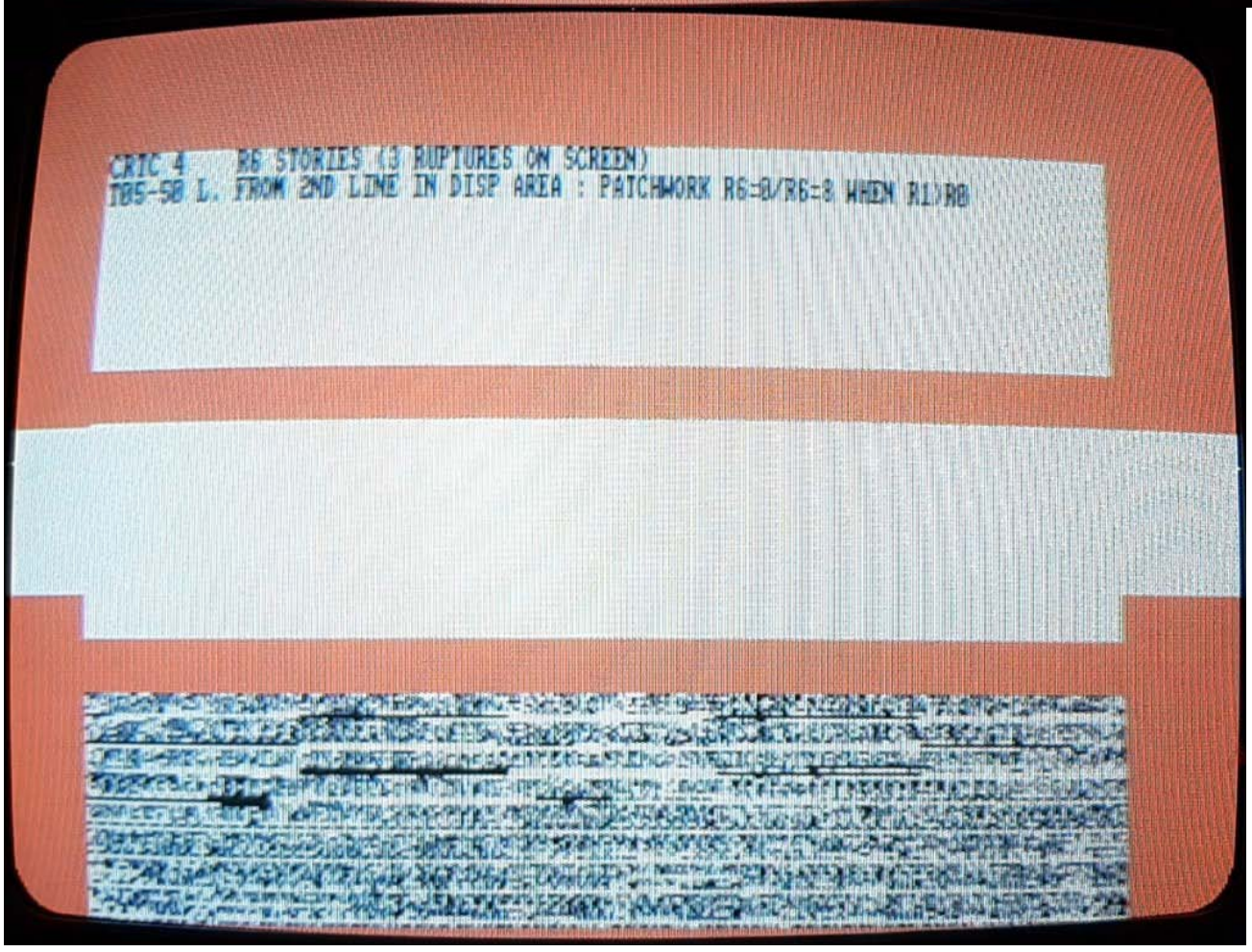
R6 STORIES

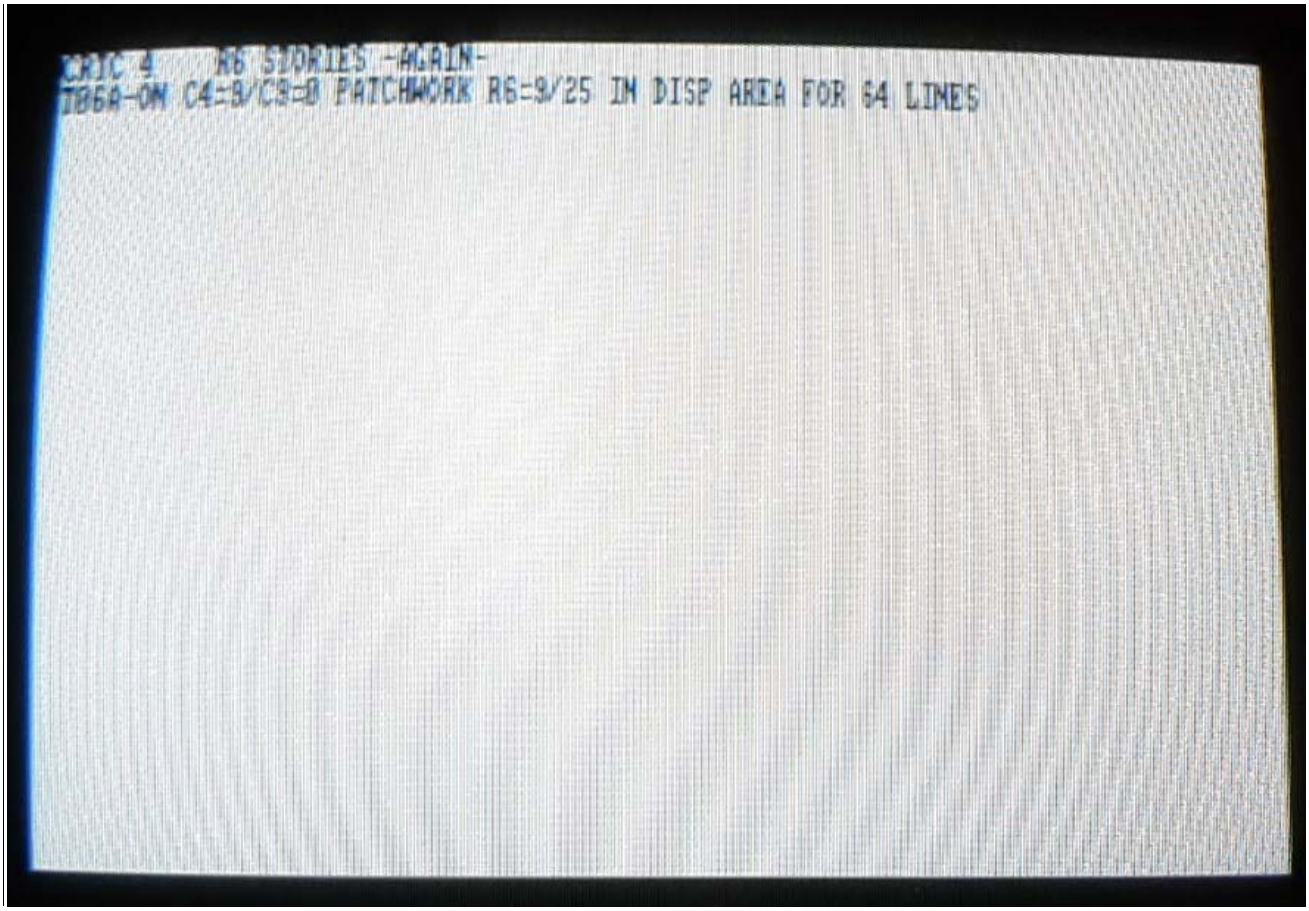

CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
(0) CRTC 2 RVMB
(F0) BOUNGA:CRTC 2 ZERO!
(F1) INTERLACE VM (27 TST)

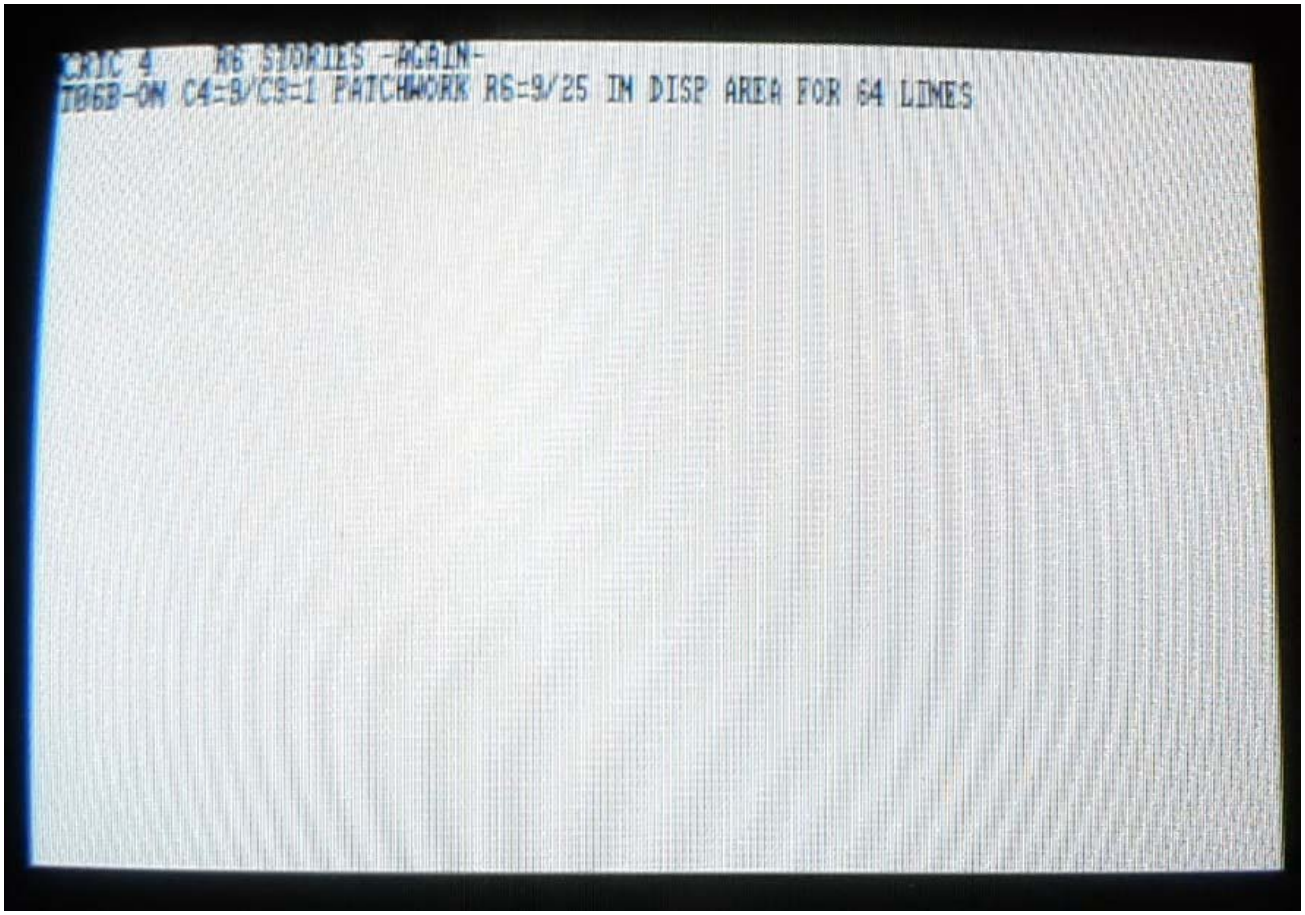

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
TBI-R6=8 IN 5 SEC. (PRESS SPACE, OR WAIT 4 SEC IN AUTO MODE)

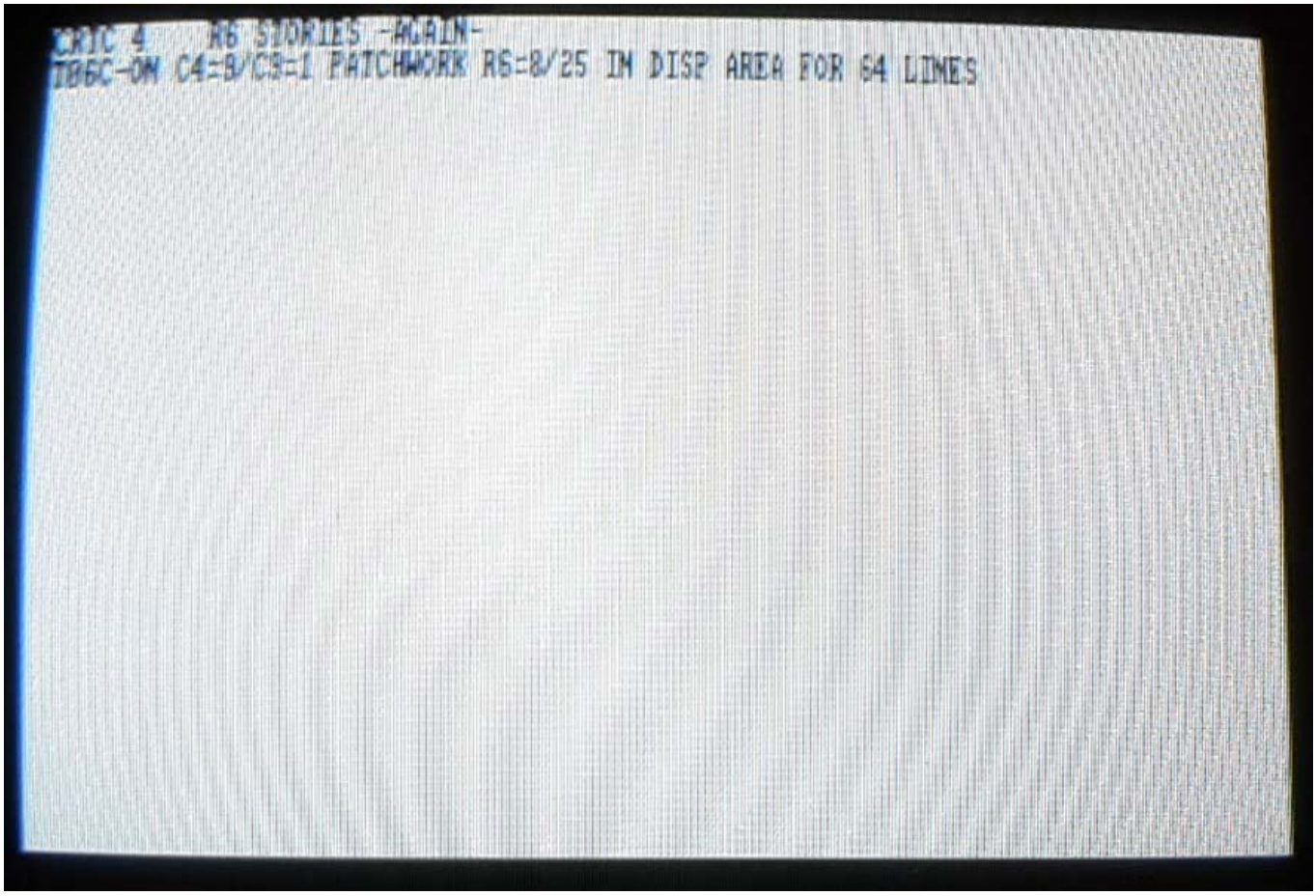

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
T82-58 L. PATCHWORK R6=0/8 FROM VERY 1ST LINE OF MIDDLE SCREEN RUPT (C4=0,C9=0)
CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
T83-58 L. PATCHWORK R6=0/8 FROM 2ND LINE OF MIDDLE SCREEN RUPTURE (C4=0,C9=1)

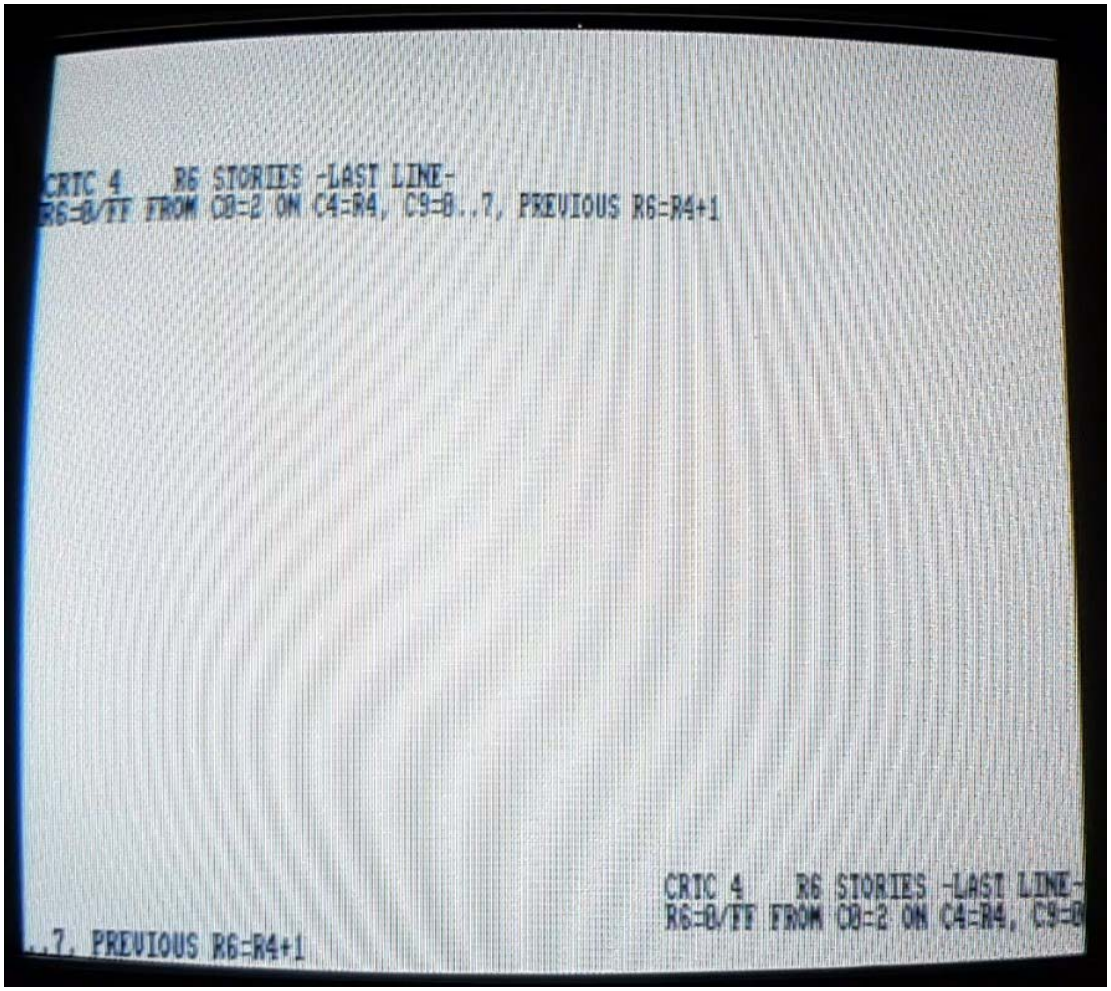

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
TB4-1ST LINE IN DISPLAY AREA : SEQUENCE R6=0/R6=8/ WHEN R1>R0

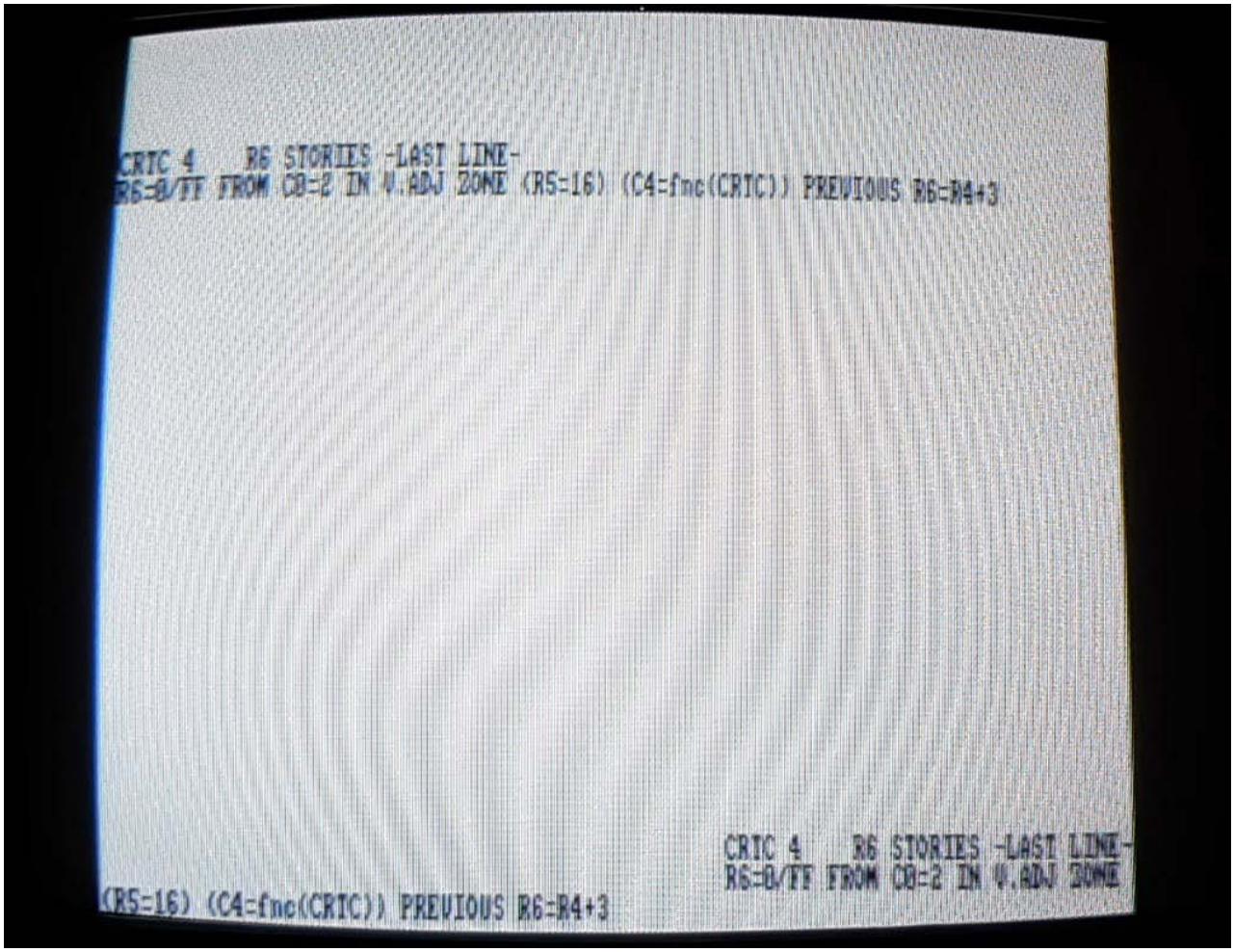

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
TB5-50 L. FROM 2ND LINE IN DISP AREA : PATCHWORK R6=0/R6=8 WHEN R1>R0

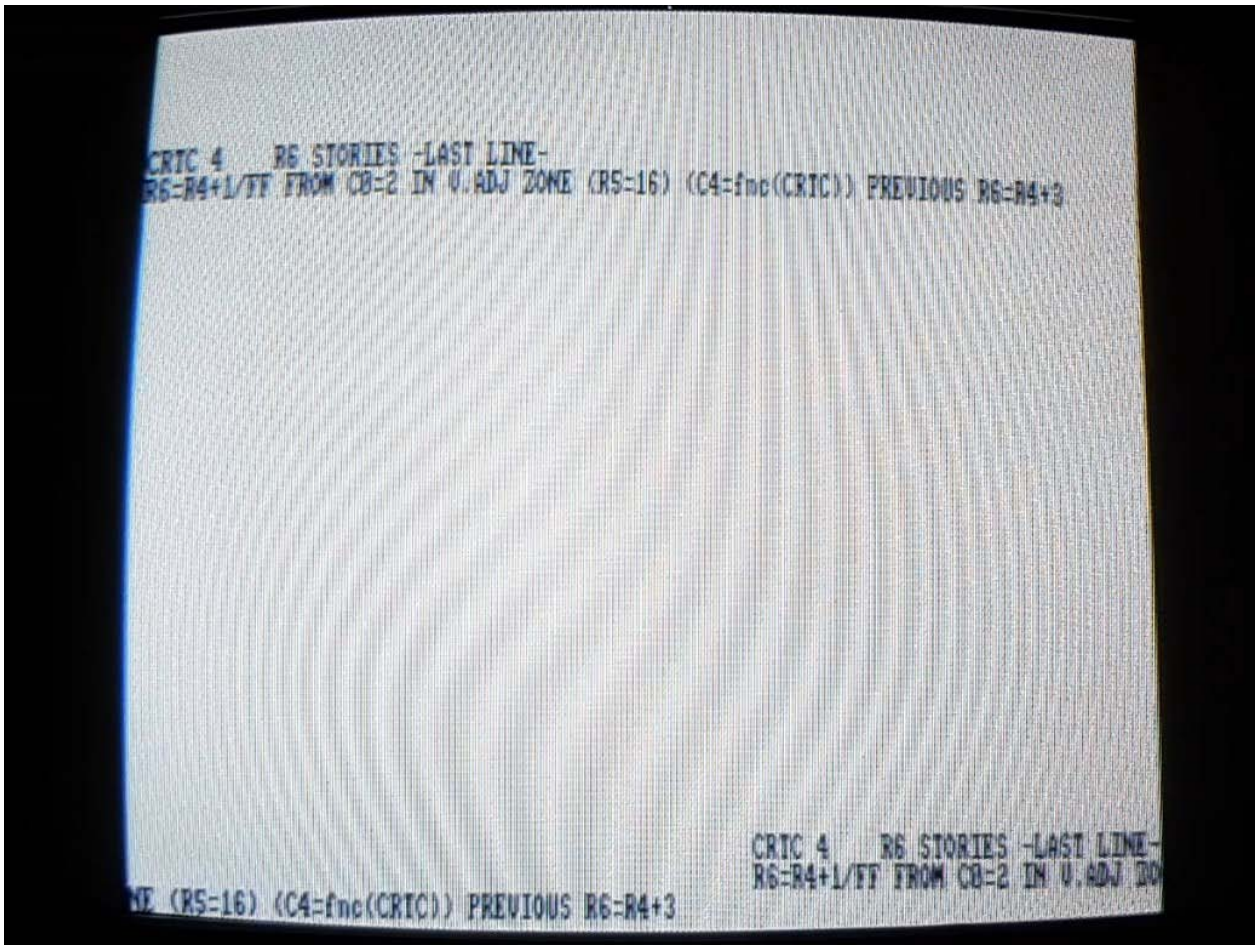

CRTC 4 R6 STORIES -AGAIN-
TB6A-ON C4=9/C9=0 PATCHWORK R6=9/25 IN DISP AREA FOR 64 LINES


CRTC 4 R6 STORIES -AGAIN-
TB6B-ON C4=9/C9=1 PATCHWORK R6=9/25 IN DISP AREA FOR 64 LINES


CRTC 4 R6 STORIES -AGAIN-
T06C-ON C4=9/C9=1 PATCHWORK R6=8/25 IN DISP AREA FOR 64 LINES

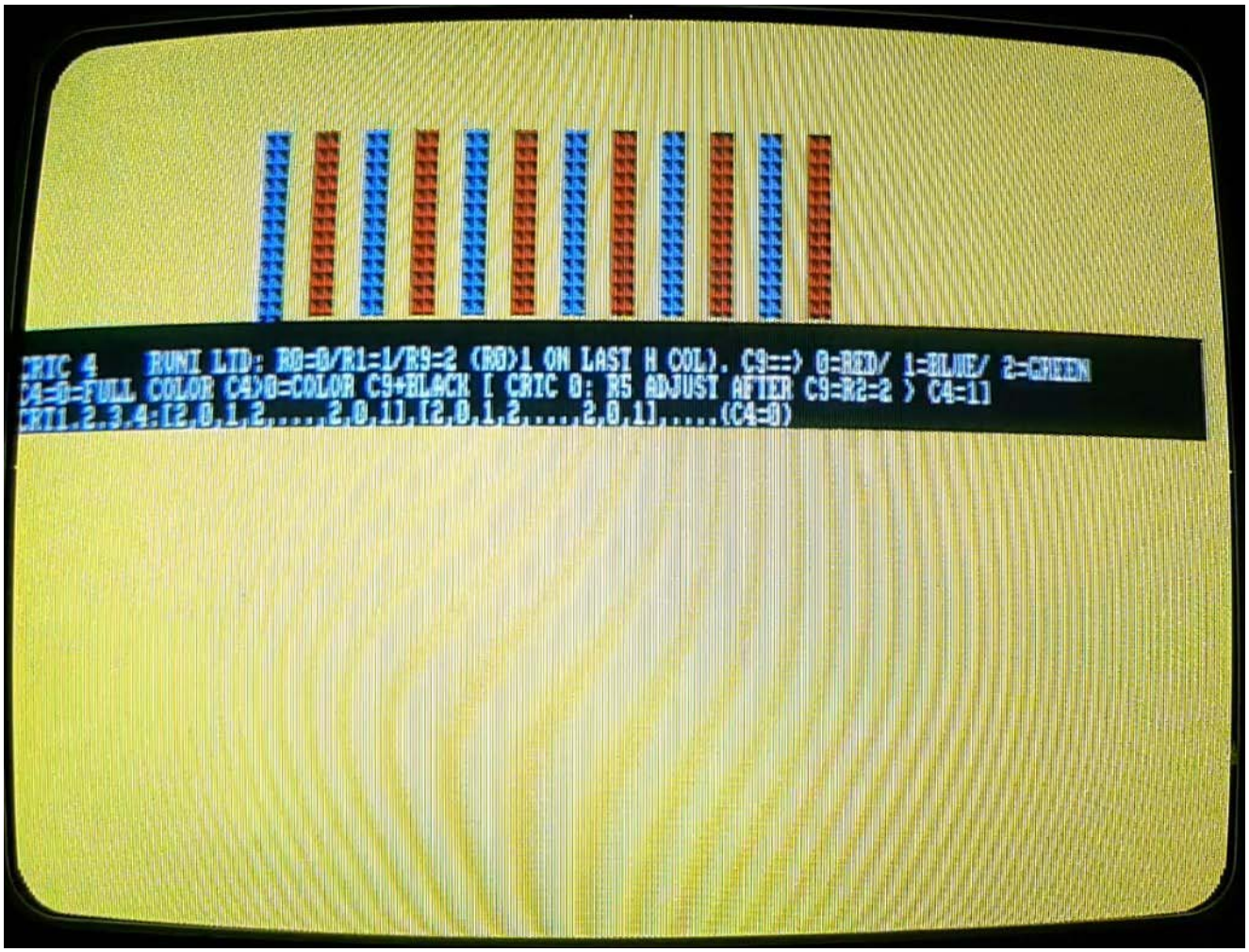

CRTC 4 R6 STORIES -LAST LINE-
R6=8/FF FROM C0=2 ON C4=R4, C9=0..7, PREVIOUS R6=R4+1
CRTC 4 R6 STORIES -LAST LINE-
..7, PREVIOUS R6=R4+1


CRTC 4 R6 STORIES -LAST LINE-
R6=0/FF FROM C0=2 IN V.ADJ ZONE (R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3
CRTC 4 R6 STORIES -LAST LINE-
R6=0/FF FROM C0=2 IN V.ADJ ZONE
(R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3


CRTC 4 R6 STORIES -LAST LINE-
R6=R4+1/FF FROM C0=2 IN V.ADJ ZONE (R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3
CRTC 4 R6 STORIES -LAST LINE-
R6=R4+1/FF FROM C0=2 IN V.ADJ ZO
(R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

RVNI (NON INVISIBLE VERTICAL RUPTURE)

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



ANALYZER / FORCED STABILISATION ON R0=0

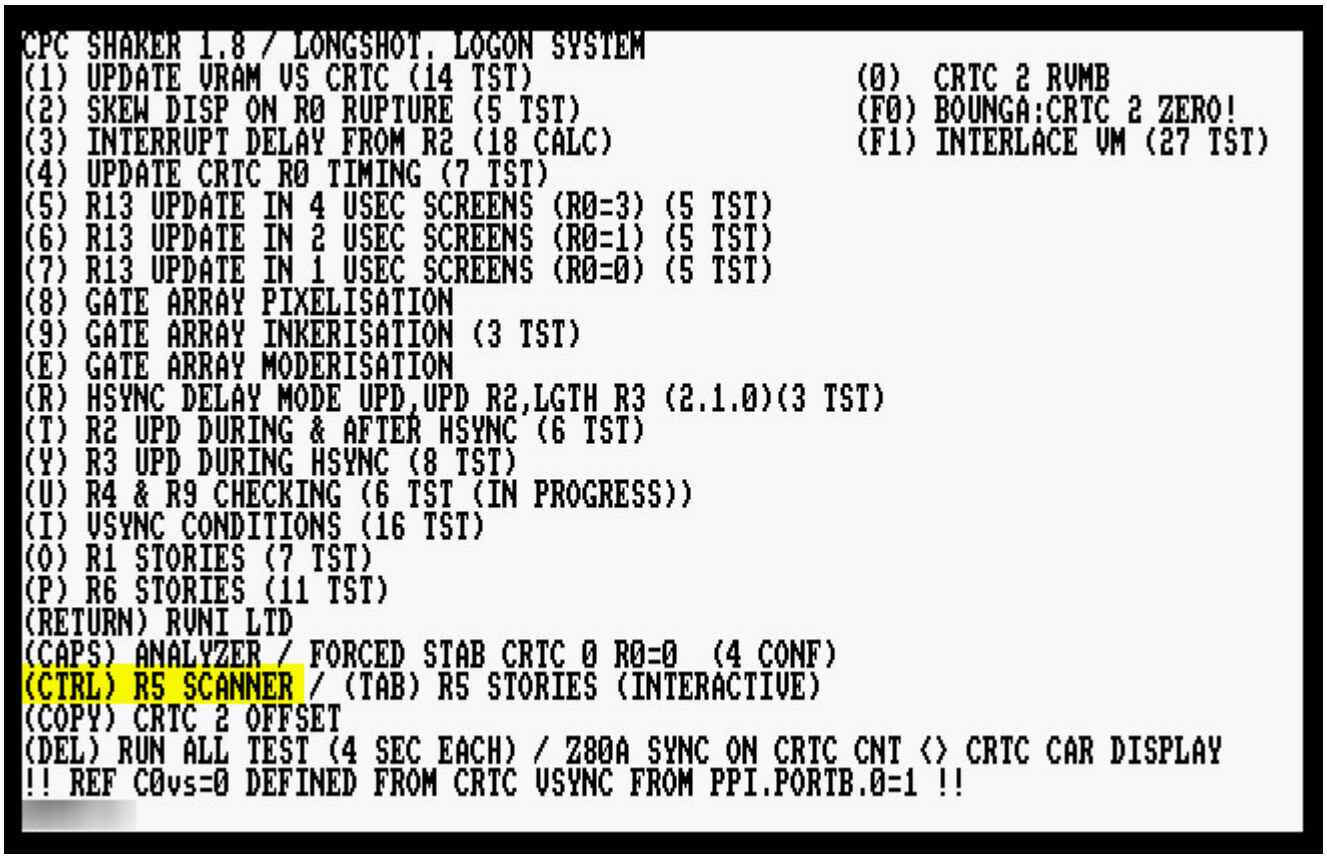
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```


CRTC ANALYZER
PRESS KEY 1 TO 8: IDENTIFY THE 1ST FLASHING COLOR UNDER 1ST PATCHWORK LINE AT >>>x<<< X POS
TEST R02 : R0=0 WHEN R4<>0, R9=0
R4 SYNC FOUND:#7A
NOTE : EXCEPT INK 0 + RED/WHITE RASTER, ONLY ONE EXTRA INK EACH 2KB BLOCK
CRTC 4


CRTC ANALYZER
PRESS KEY 1 TO 8: IDENTIFY THE 1ST FLASHING COLOR UNDER 1ST PATCHWORK LINE AT >>>x<<< X POS
TEST R03 : R0=0 WHEN R4=0, R9<>0
R4 SYNC FOUND:#48
NOTE : EXCEPT INK 0 + RED/WHITE RASTER, ONLY ONE EXTRA INK EACH 2KB BLOCK
CRTC 4

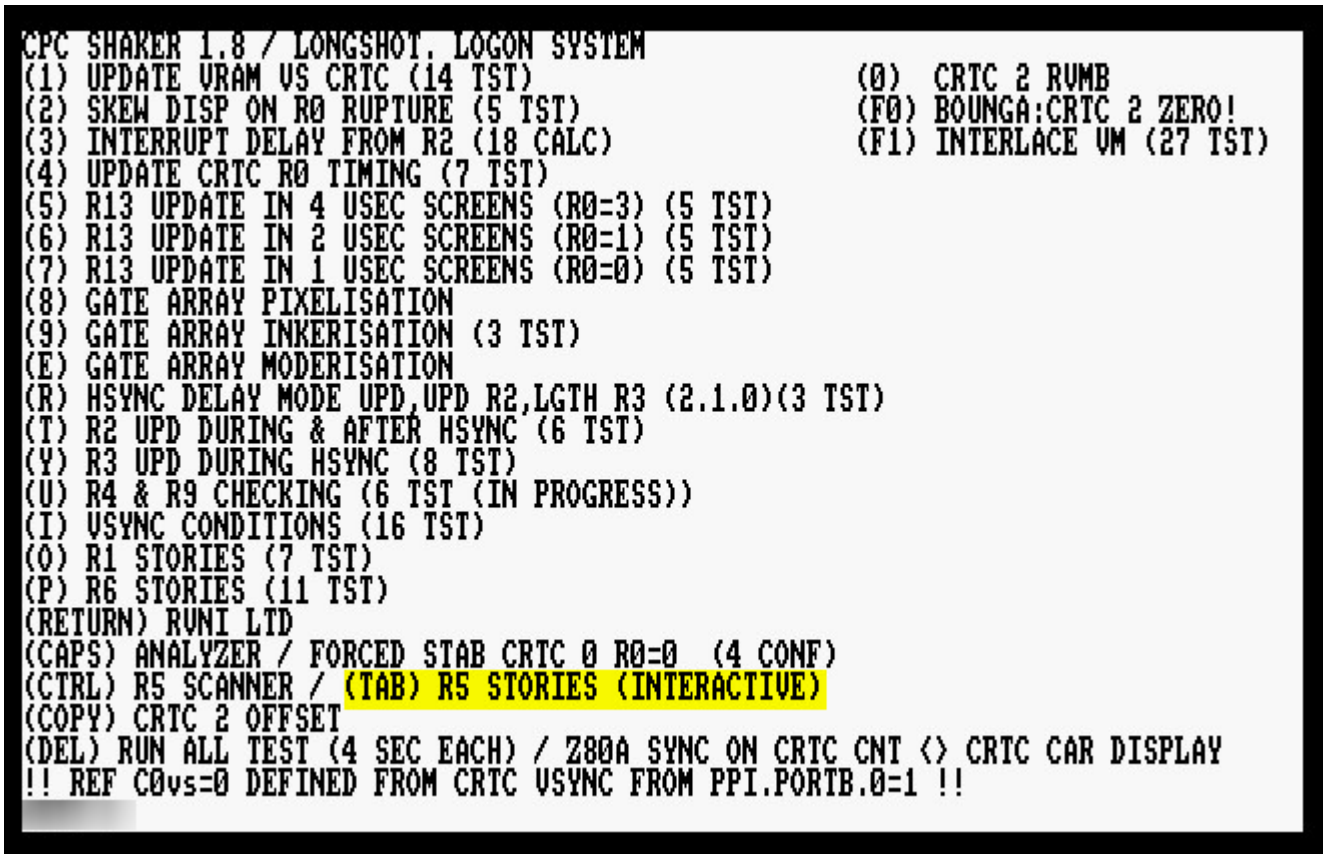

CRTC ANALYZER
PRESS KEY 1 TO 8: IDENTIFY THE 1ST FLASHING COLOR UNDER 1ST PATCHWORK LINE AT)))nxxxx(H POS
TEST R04 : R0=0 WHEN R4=0, R9=0
R4 SYNC FOUND:#48
NOTE : EXCEPT INK 0 + RED/WHITE RASTER, ONLY ONE EXTRA INK EACH 2KB BLOCK
CRTC 4

R5 SCANNER (for CRTC 1)



Only for CRTC 1

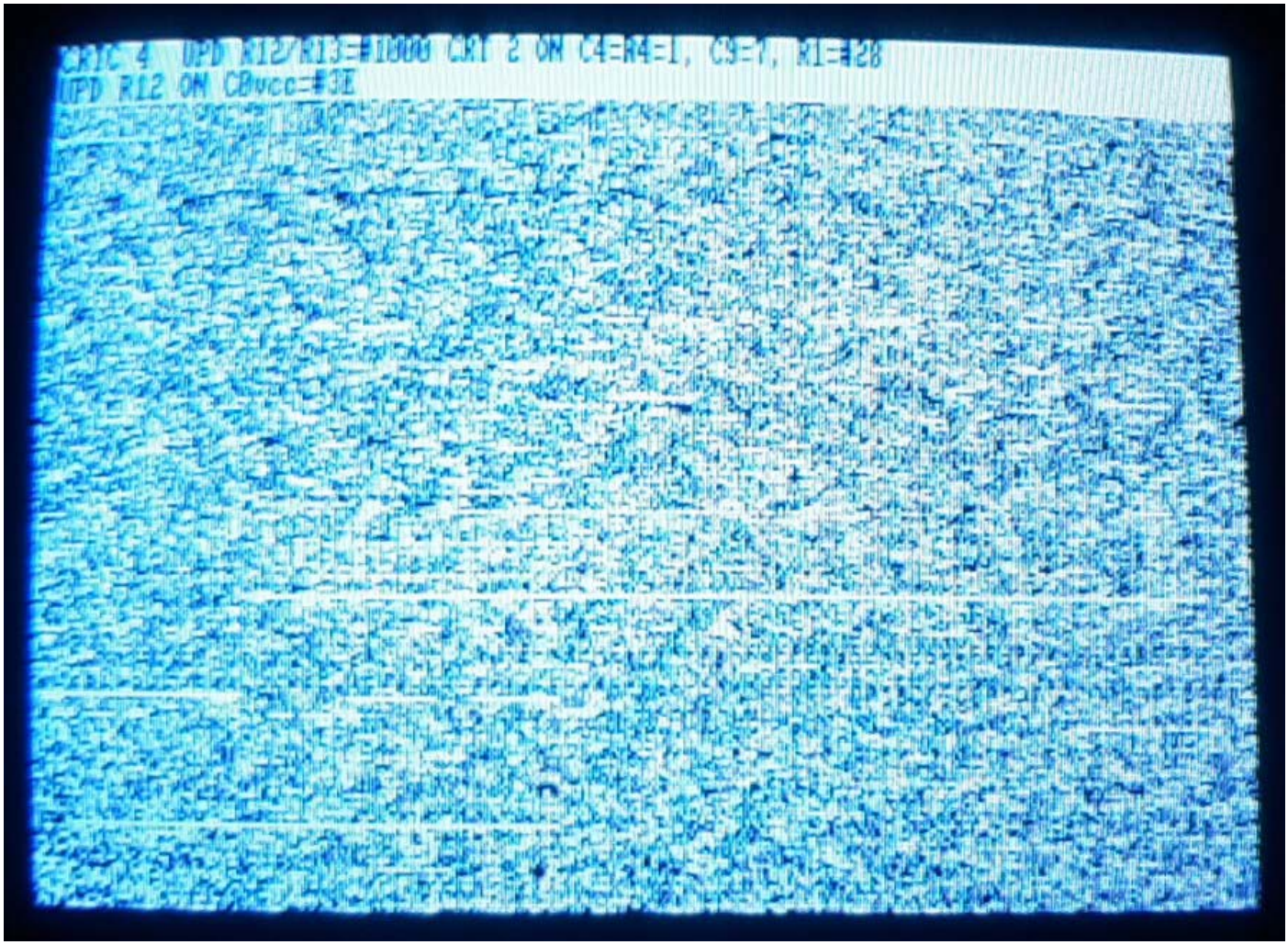
R5 STORIES / INTERACTIVE TEST



Only for CRTC 1

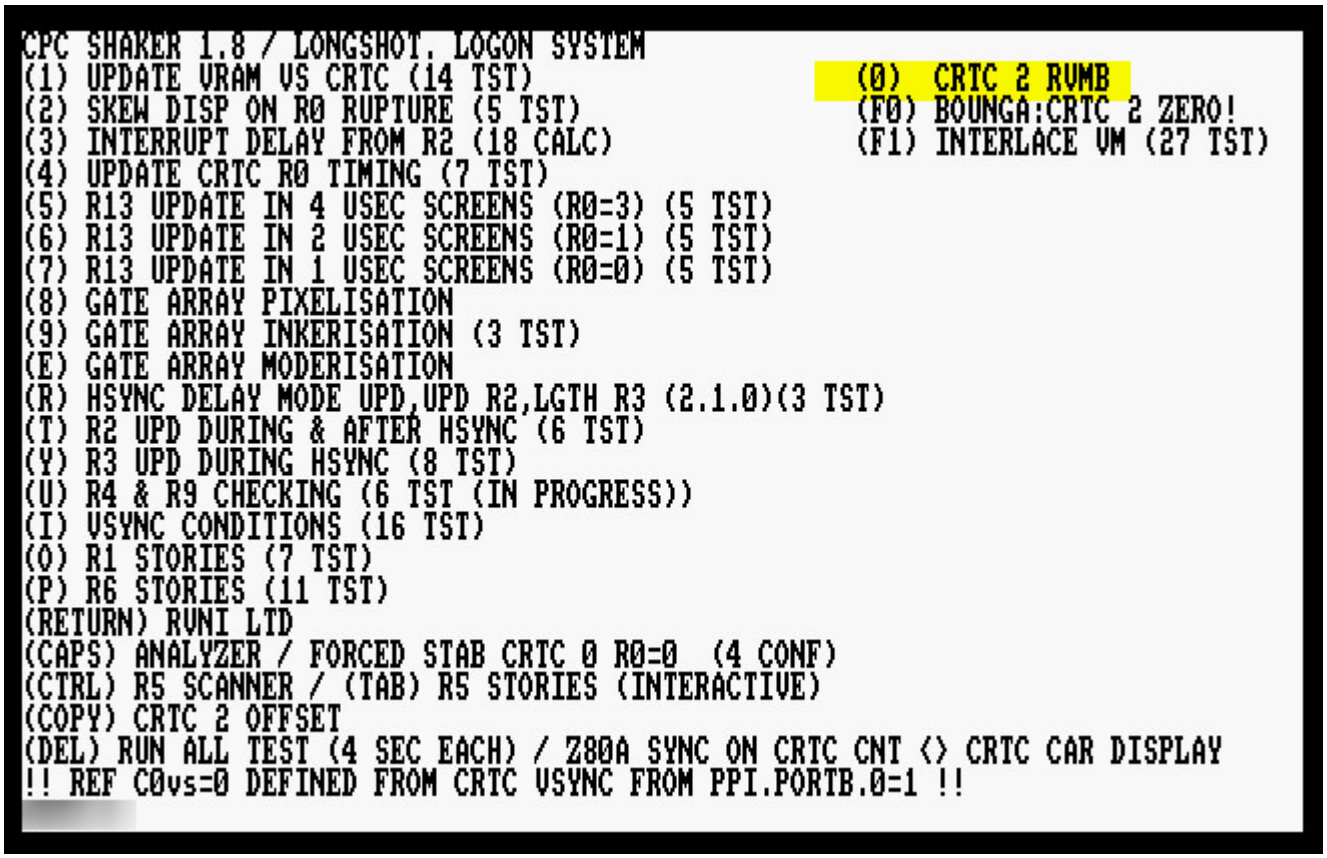
OFFSET UPDATE

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```




CRTC 4 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON CDvcc=#3F
CRTC 4 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON CDvcc=#3F

« RVMB »


CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
(0) CRTC 2 RVMB
(F0) BOUNGA:CRTC 2 ZERO!
(F1) INTERLACE VM (27 TST)


R0=3 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 16 RUPT / LINE
TEST WITH R1=3, R9=7, R4=120
CRTC 4


R0=3 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 16 RUPT / LINE
TEST WITH R1=3, R9=7, R4=120
CRTC 4


R0=3 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR >> C9=0 - 16 RUPT / LINE
TEST WITH R1=4, R9=7, R4=120
CRTC 4


R0=3 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR >> C9=0 - 16 RUPT / LINE
TEST WITH R1=4, R9=7, R4=120
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=0
CRTC 4

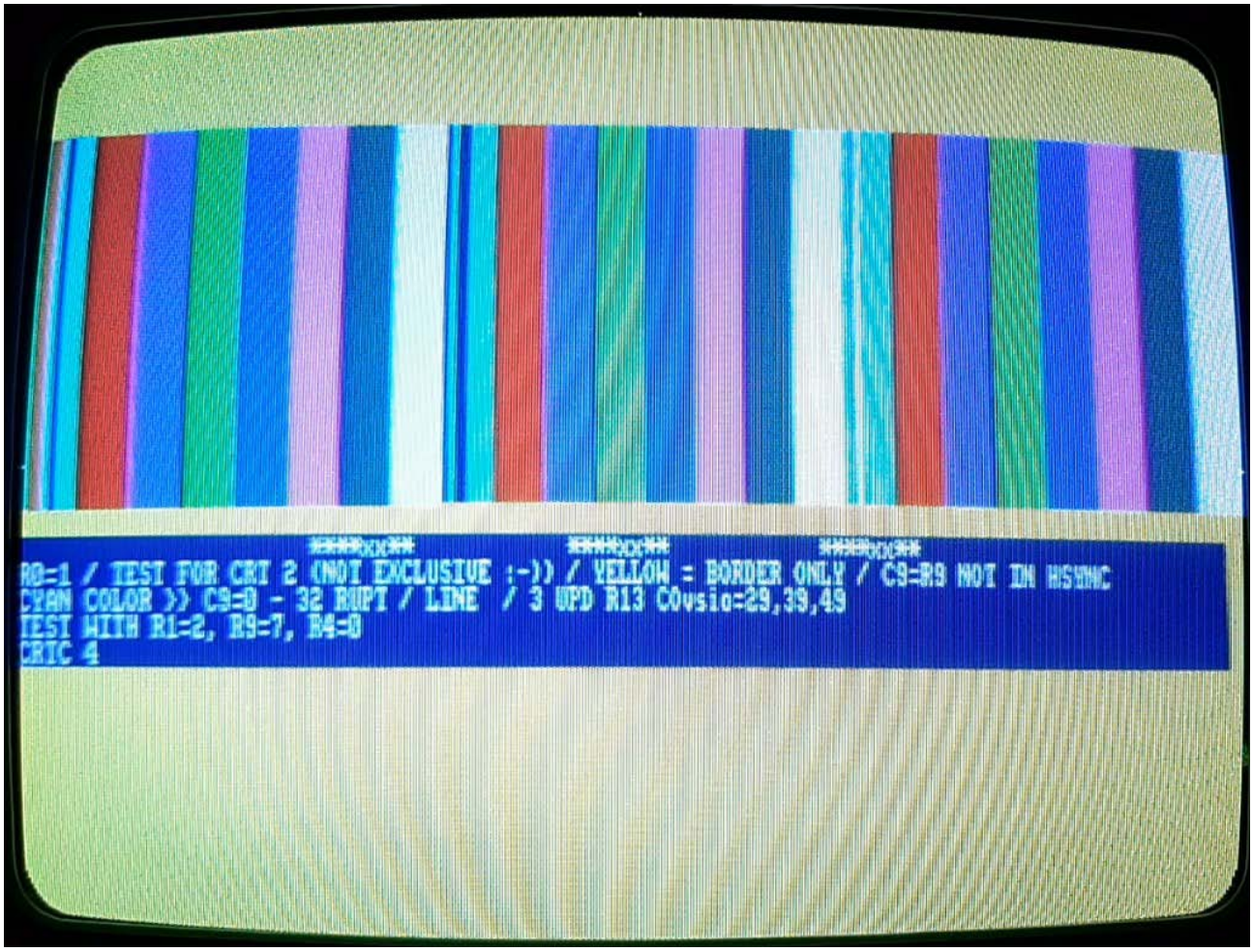

R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=0
CRTC 4


R0=1 / TEST FOR CRI 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=1, R9=7, R4=0
CRTC 4


R0=1 / TEST FOR CRI 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=1, R9=7, R4=0
CRTC 4

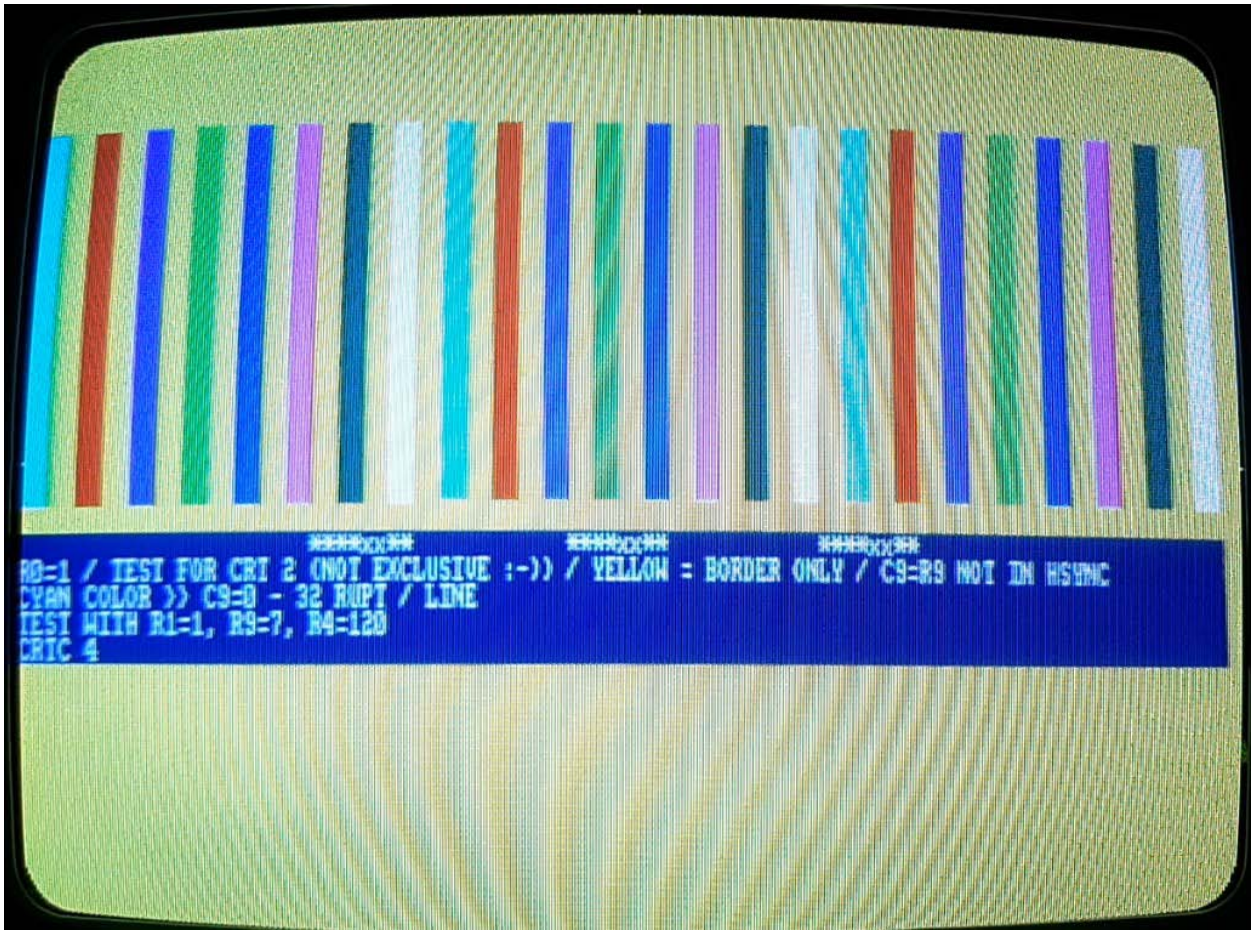

R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=0
CRTC 4

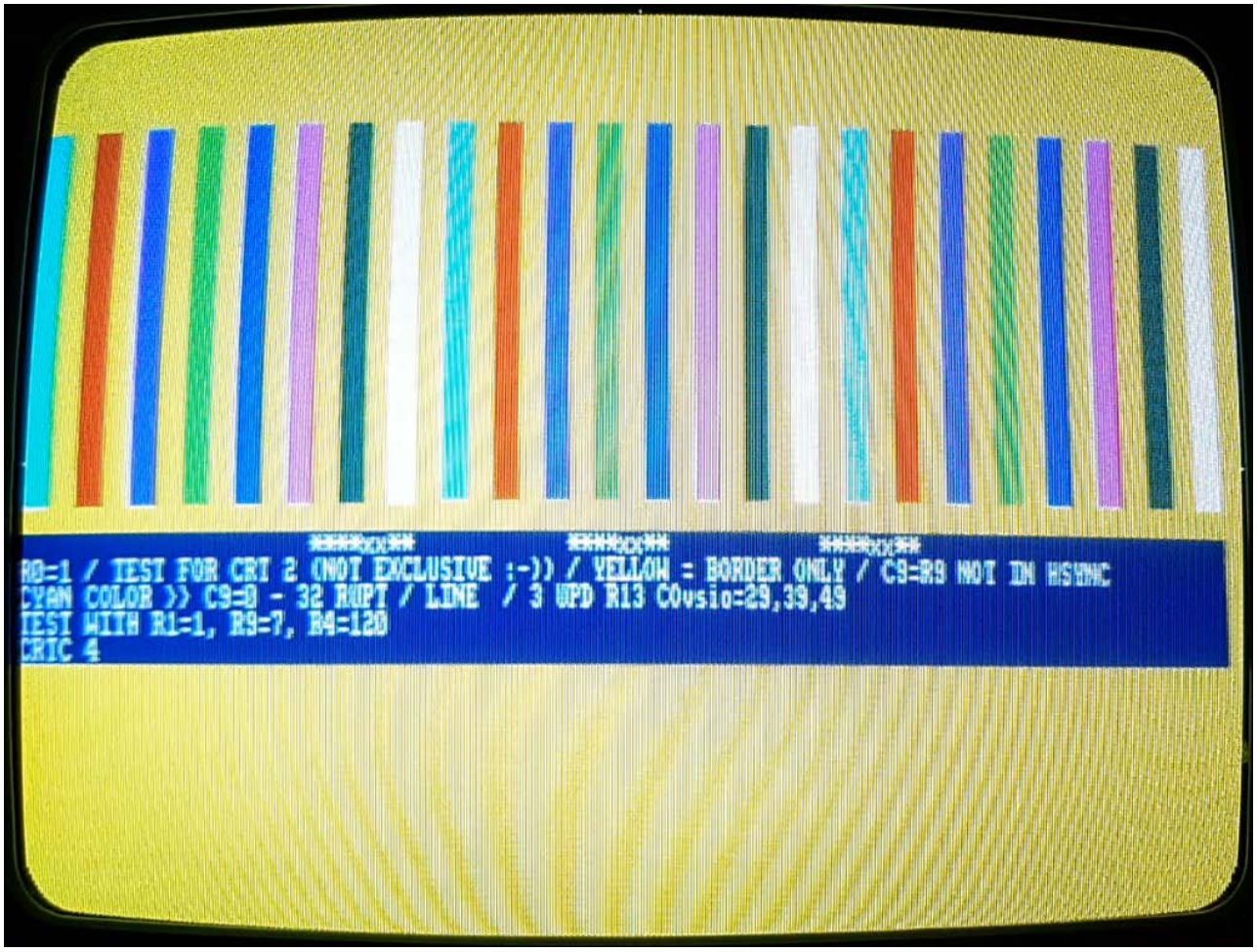

R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=0
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR >> C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=2, R9=7, R4=0
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR >> C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=2, R9=7, R4=0
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=89 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=128
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=89 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=128
CRTC 4


R0=1 / TEST FOR CRI 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=1, R9=7, R4=120
CRIC 4


R0=1 / TEST FOR CRI 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=1, R9=7, R4=120
CRIC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=128
CRTC 4

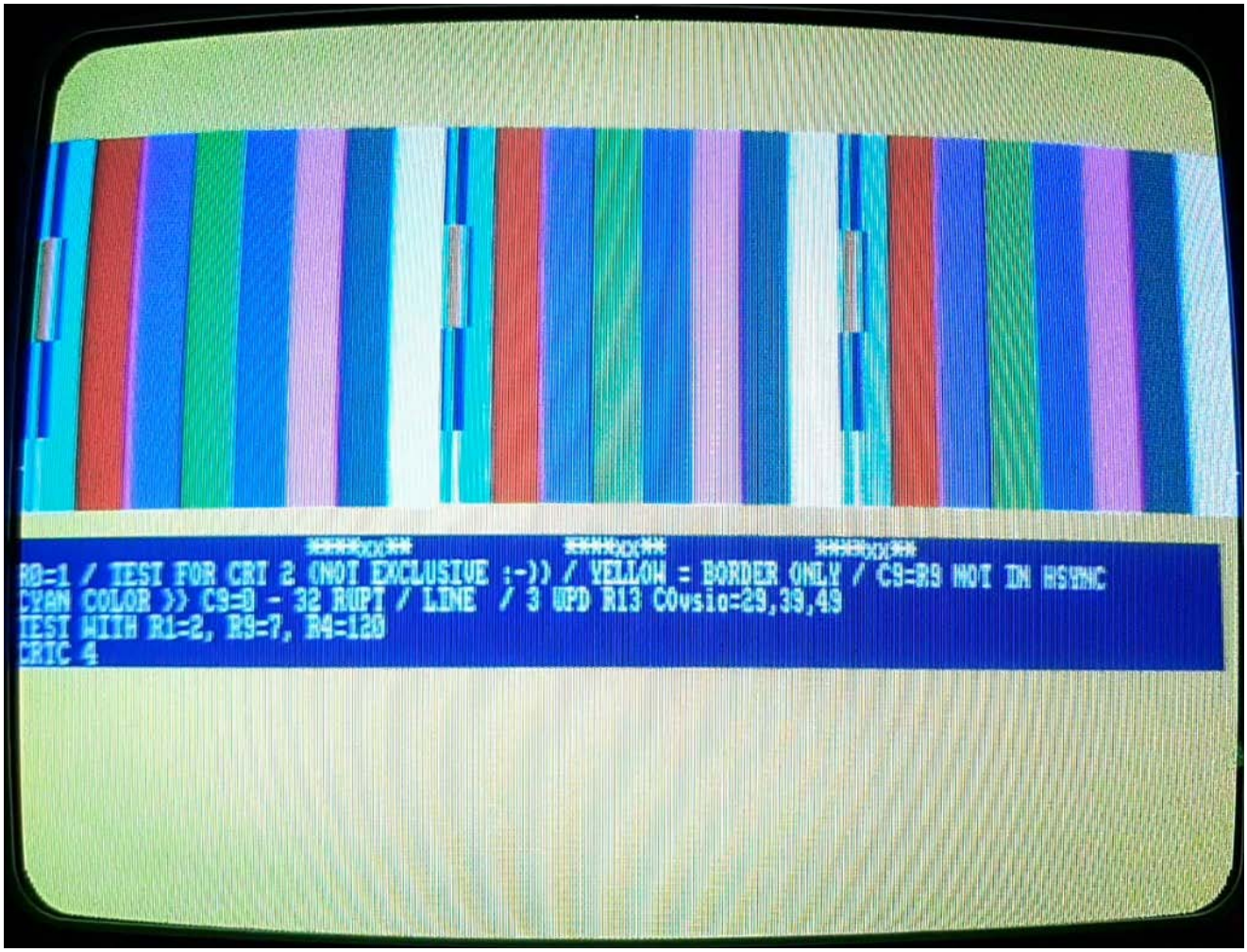

R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=128
CRTC 4

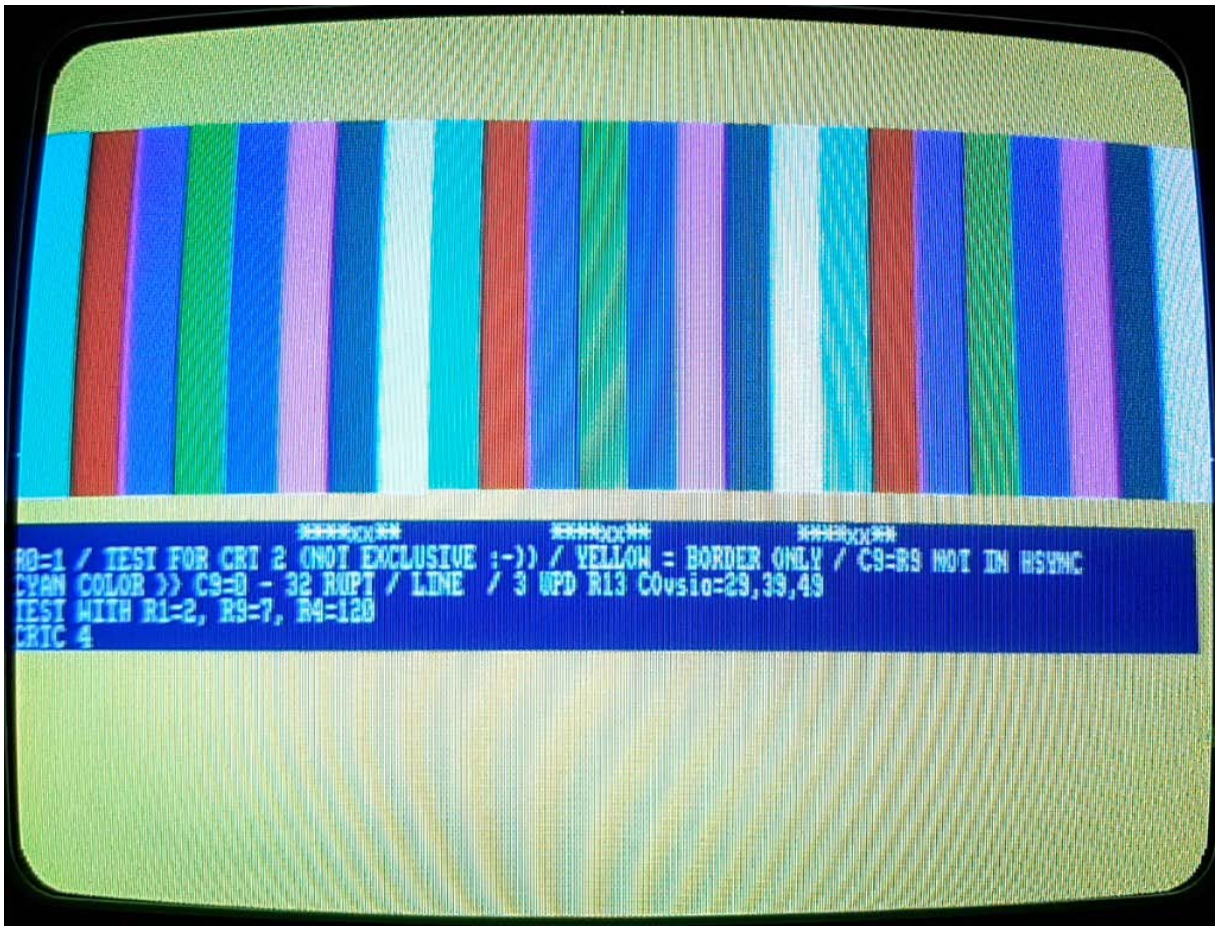

R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IM HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=1, R9=7, R4=120
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IM HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=1, R9=7, R4=120
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=120
CRTC 4

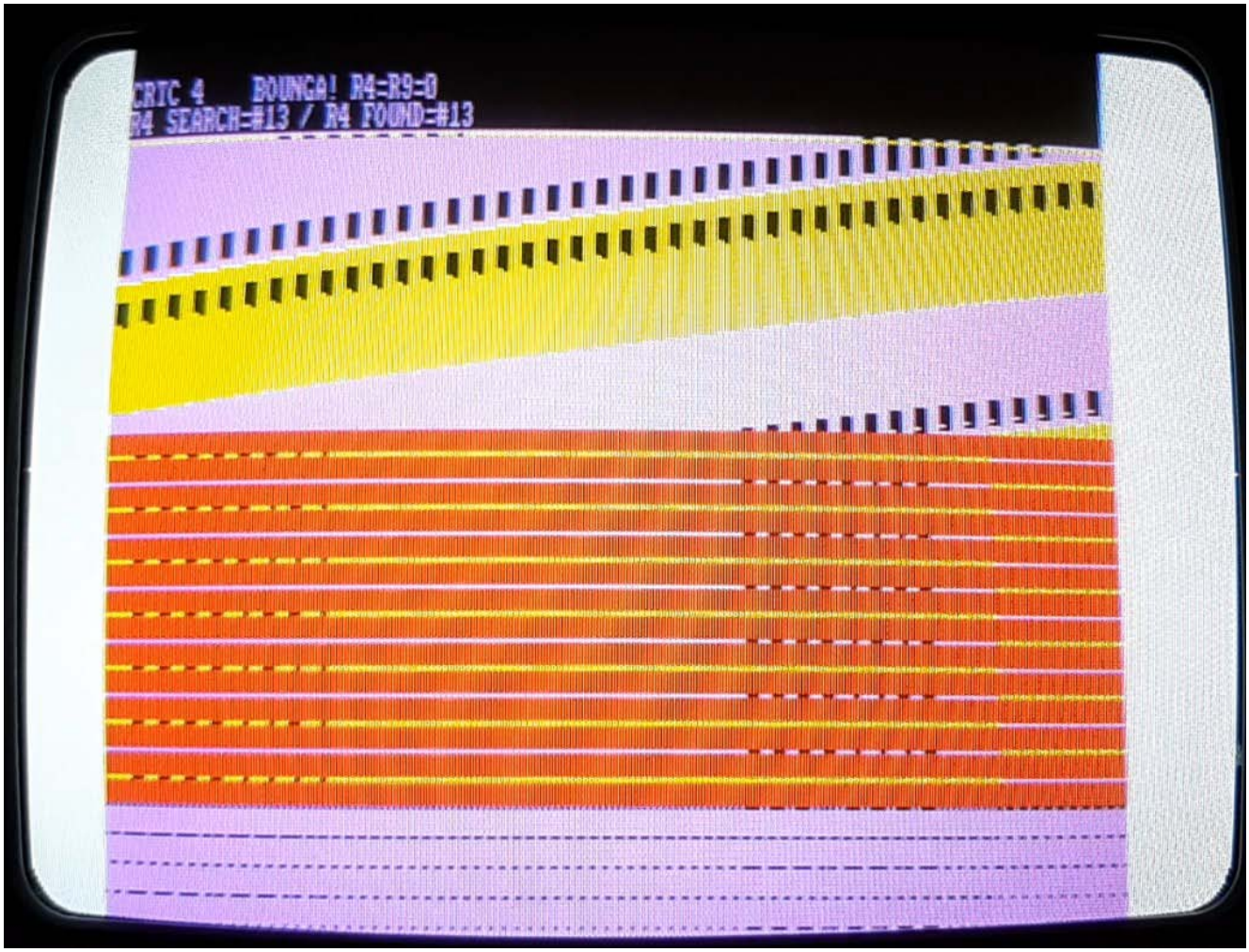

R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=120
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=2, R9=7, R4=120
CRTC 4


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE / 3 UPD R13 COvsio=29,39,49
TEST WITH R1=2, R9=7, R4=120
CRTC 4

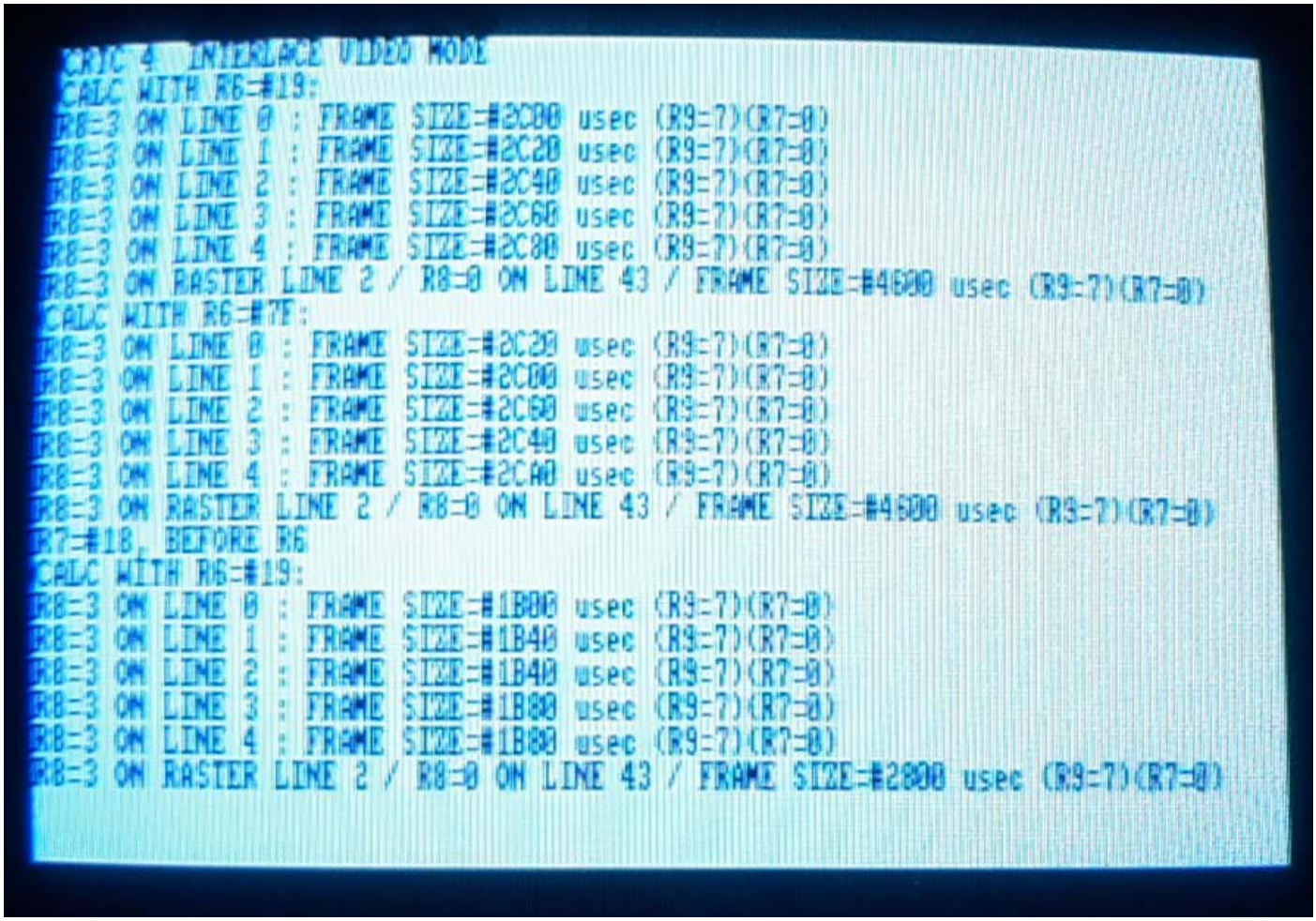
BOUNGA : CRTC 2 R4=R9=0 FORCED

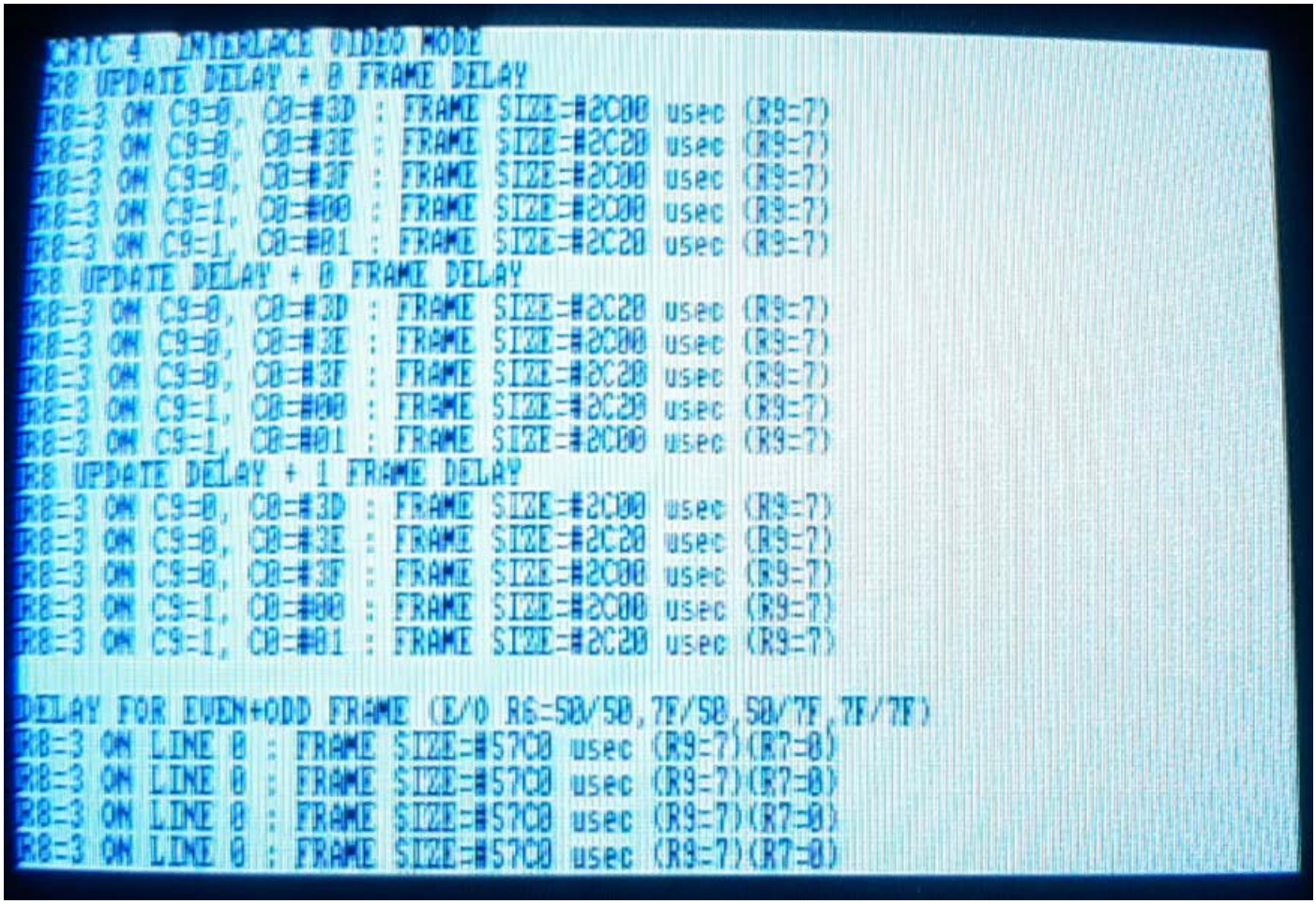
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



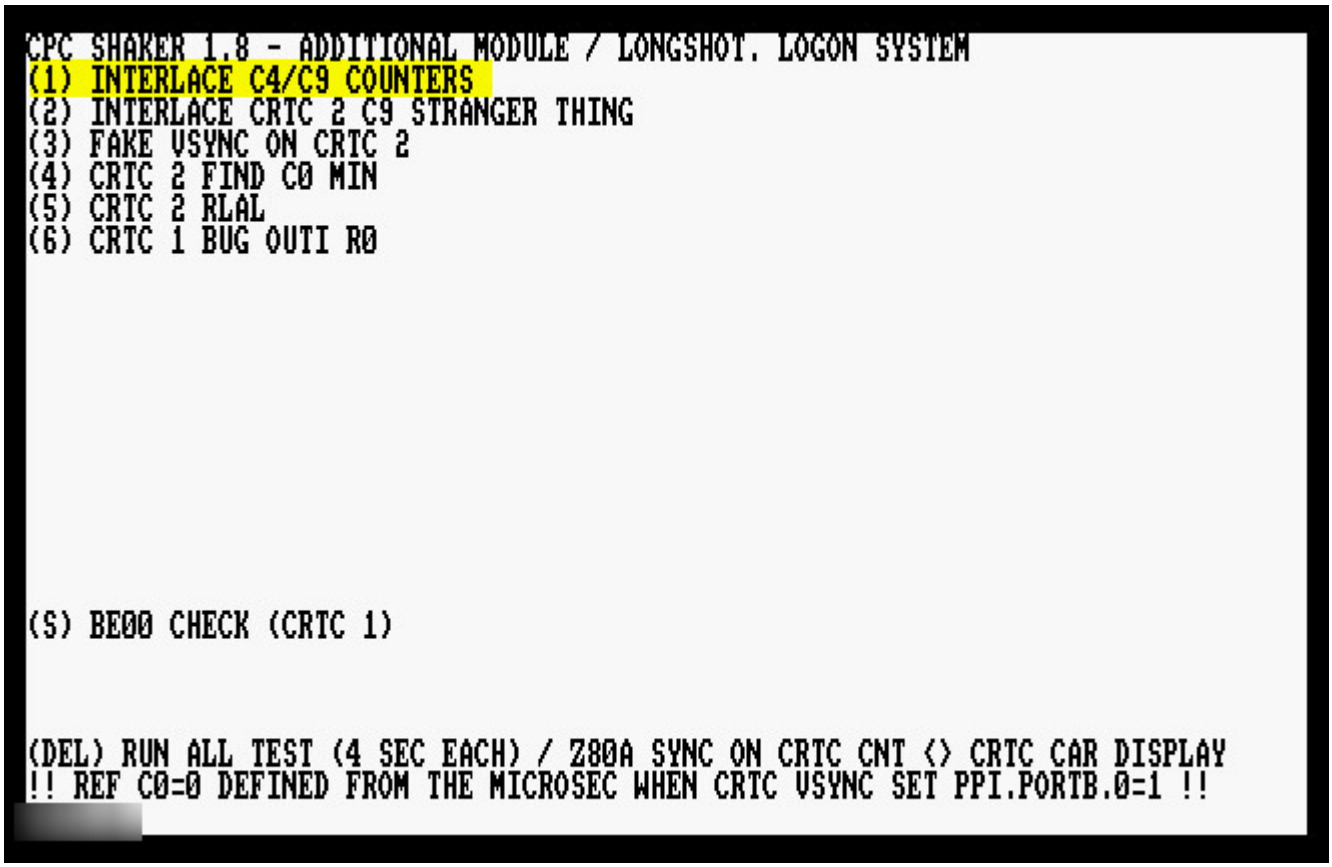
INTERLACE VM

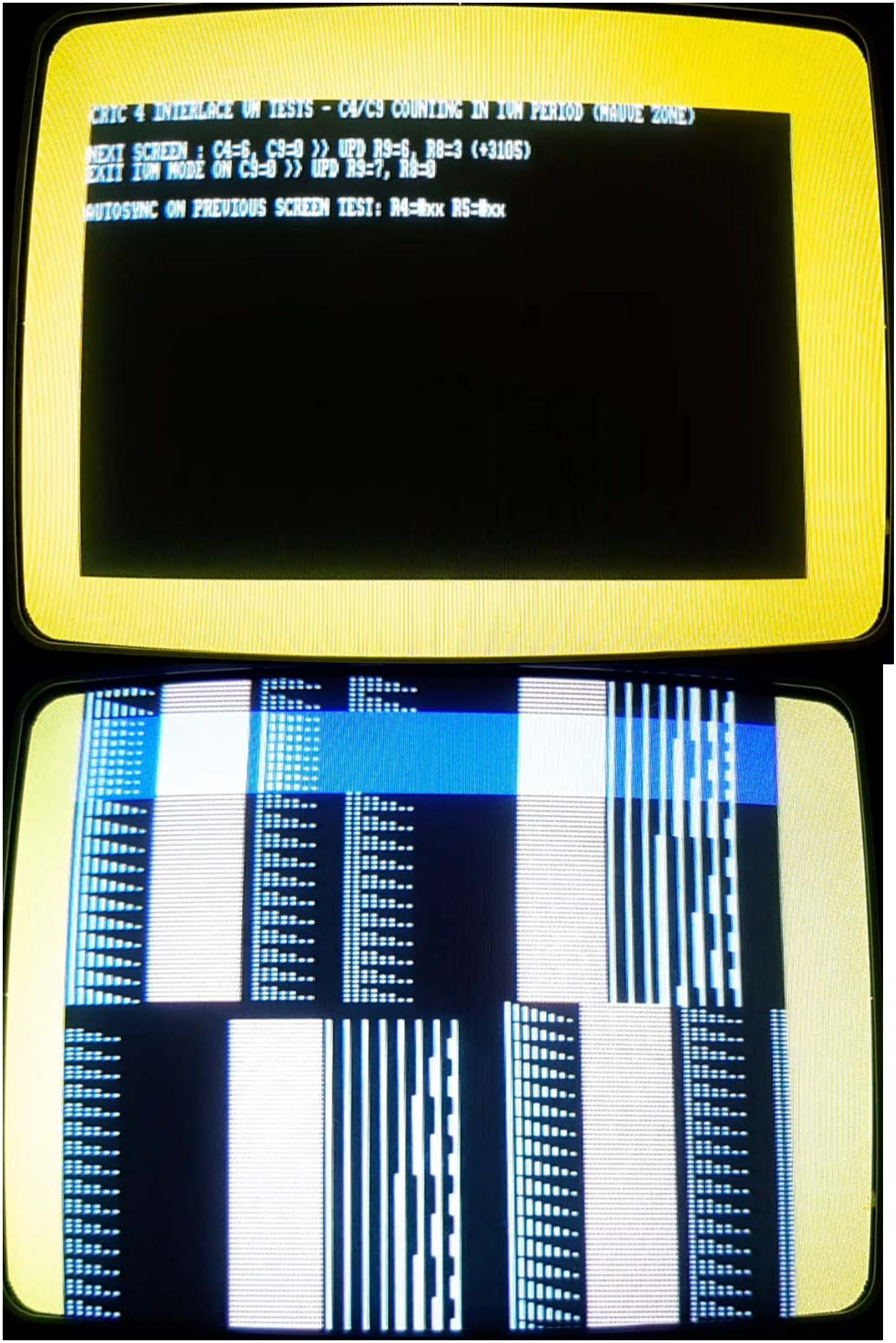
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



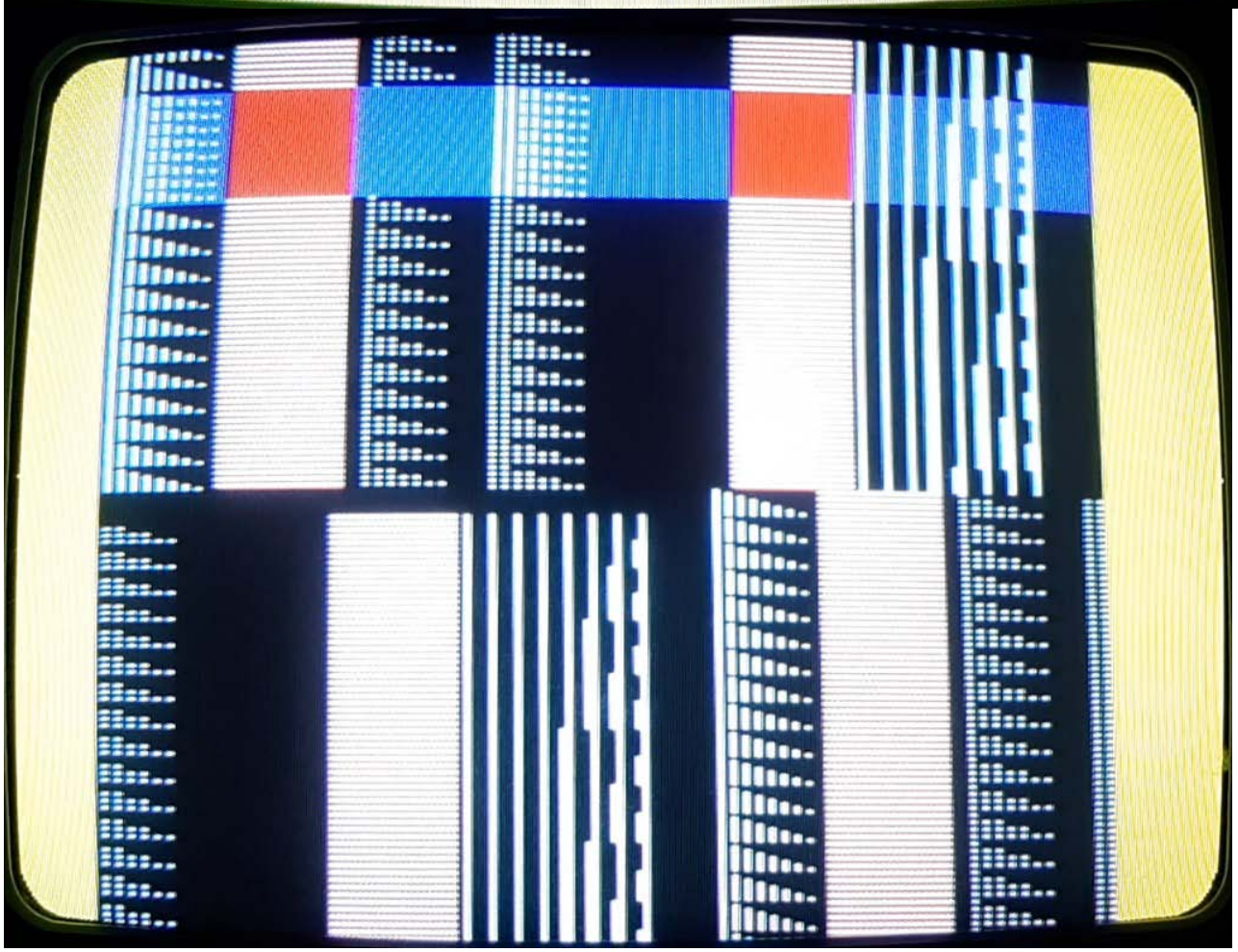

CRTC 4 INTERLACE VIDEO MODE
R8 UPDATE DELAY + 0 FRAME DELAY
R8=3 ON C9=0, C0=#3D : FRAME SIZE=#2C00 usec (R9=7)
R8=3 ON C9=0, C0=#3E : FRAME SIZE=#2C20 usec (R9=7)
R8=3 ON C9=0, C0=#3F : FRAME SIZE=#2C00 usec (R9=7)
R8=3 ON C9=1, C0=#00 : FRAME SIZE=#2C00 usec (R9=7)
R8=3 ON C9=1, C0=#01 : FRAME SIZE=#2C20 usec (R9=7)
R8 UPDATE DELAY + 0 FRAME DELAY
R8=3 ON C9=0, C0=#3D : FRAME SIZE=#2C20 usec (R9=7)
R8=3 ON C9=0, C0=#3E : FRAME SIZE=#2C00 usec (R9=7)
R8=3 ON C9=0, C0=#3F : FRAME SIZE=#2C20 usec (R9=7)
R8=3 ON C9=1, C0=#00 : FRAME SIZE=#2C20 usec (R9=7)
R8=3 ON C9=1, C0=#01 : FRAME SIZE=#2C00 usec (R9=7)
R8 UPDATE DELAY + 1 FRAME DELAY
R8=3 ON C9=0, C0=#3D : FRAME SIZE=#2C00 usec (R9=7)
R8=3 ON C9=0, C0=#3E : FRAME SIZE=#2C20 usec (R9=7)
R8=3 ON C9=0, C0=#3F : FRAME SIZE=#2C00 usec (R9=7)
R8=3 ON C9=1, C0=#00 : FRAME SIZE=#2C00 usec (R9=7)
R8=3 ON C9=1, C0=#01 : FRAME SIZE=#2C20 usec (R9=7)
DELAY FOR EVEN+ODD FRAME (E/O R6=50/50,7F/50,50/7F,7F/7F)
R8=3 ON LINE 0 : FRAME SIZE=#5700 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#5700 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#5700 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#5700 usec (R9=7)(R7=0)

INTERLACE C4/C9 COUNTERS

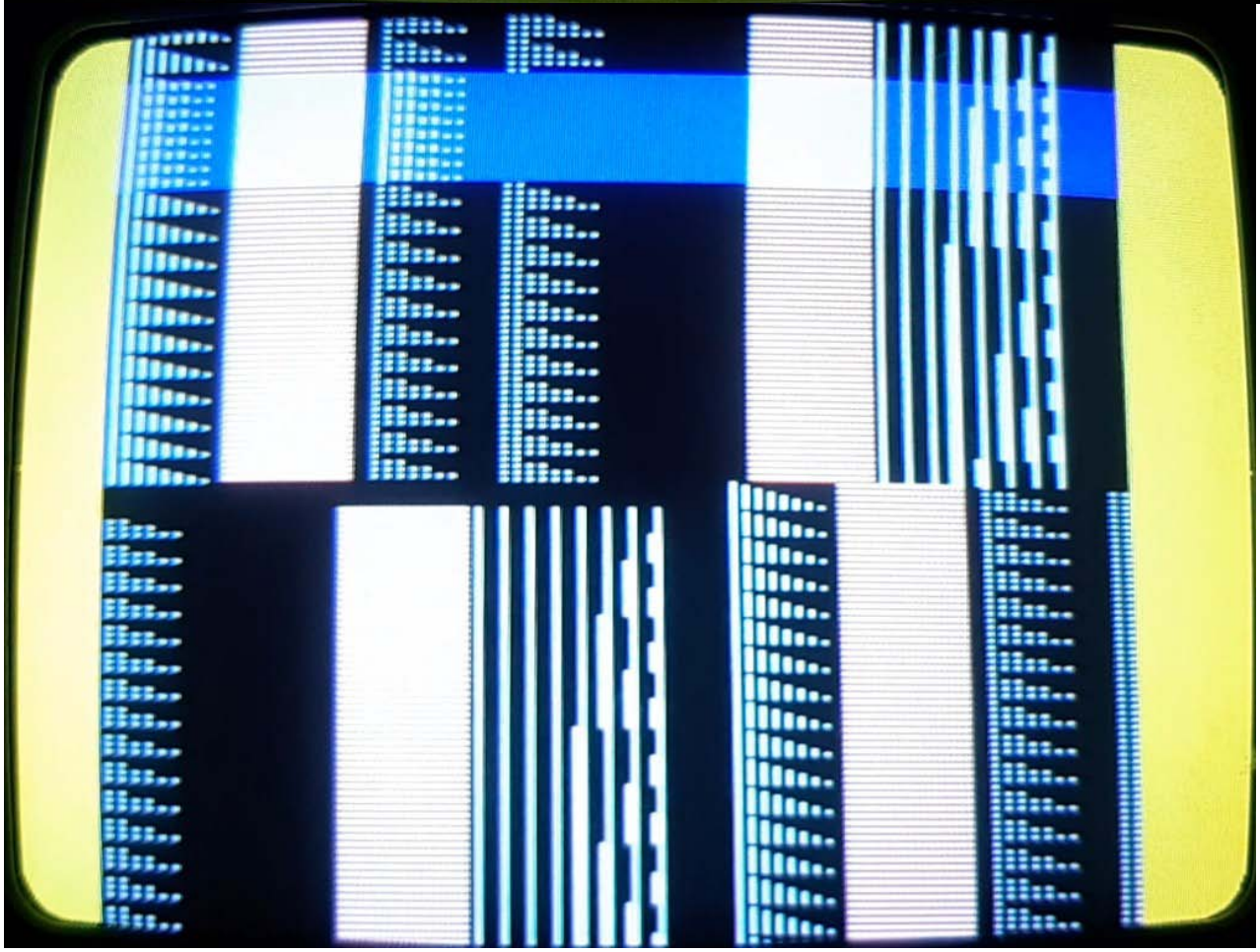



CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=0 >> UPD R9=6, R8=3 (+310S)
EXIT IVH MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#xx R5=#xx

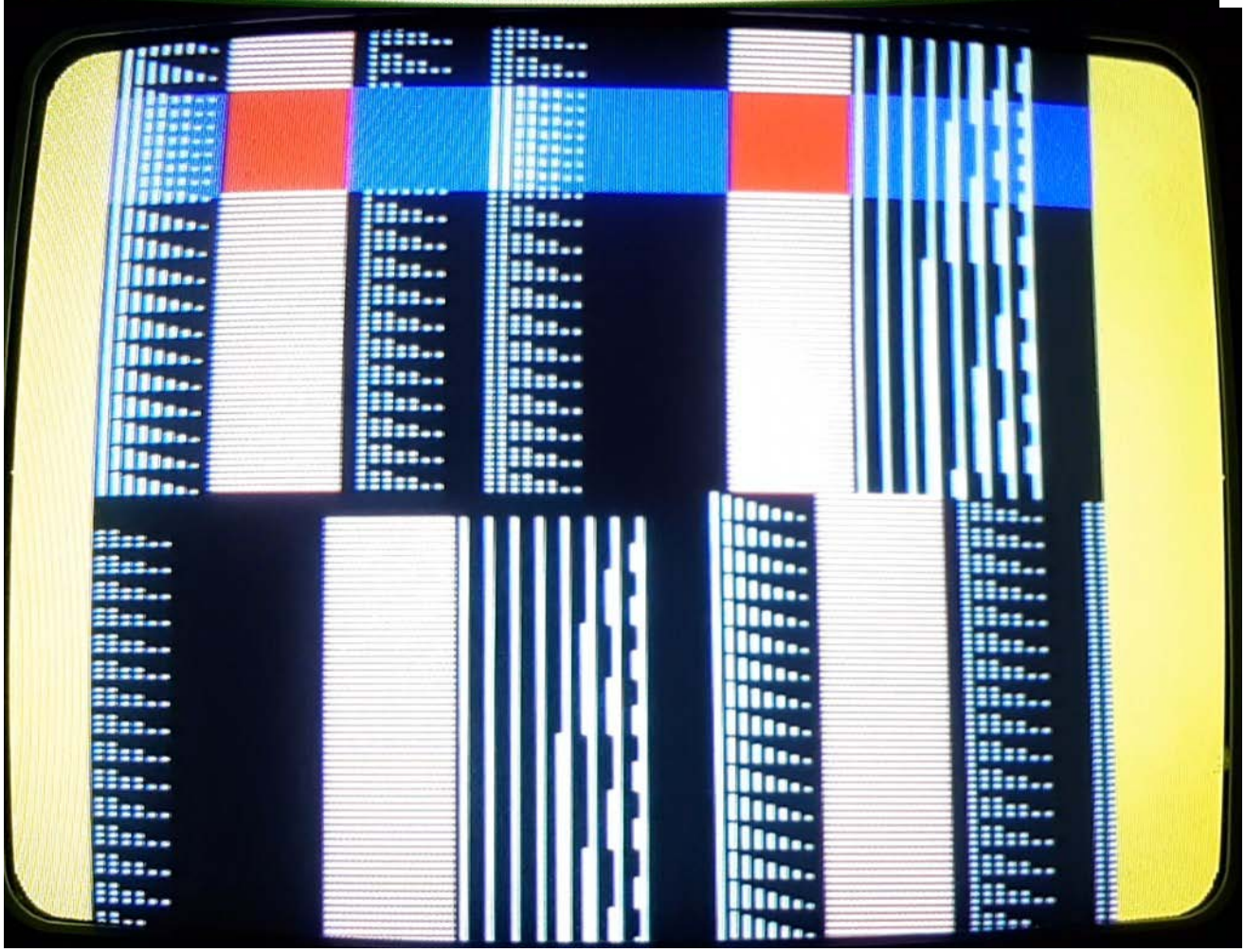

CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN VDW PERIOD (HHUUE ZONE)
NEXT SCREEN : C4=6, C9=1 >> UPD R9=6, R8=3 (+310S)
EXIT IVH MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#2A R5=#00



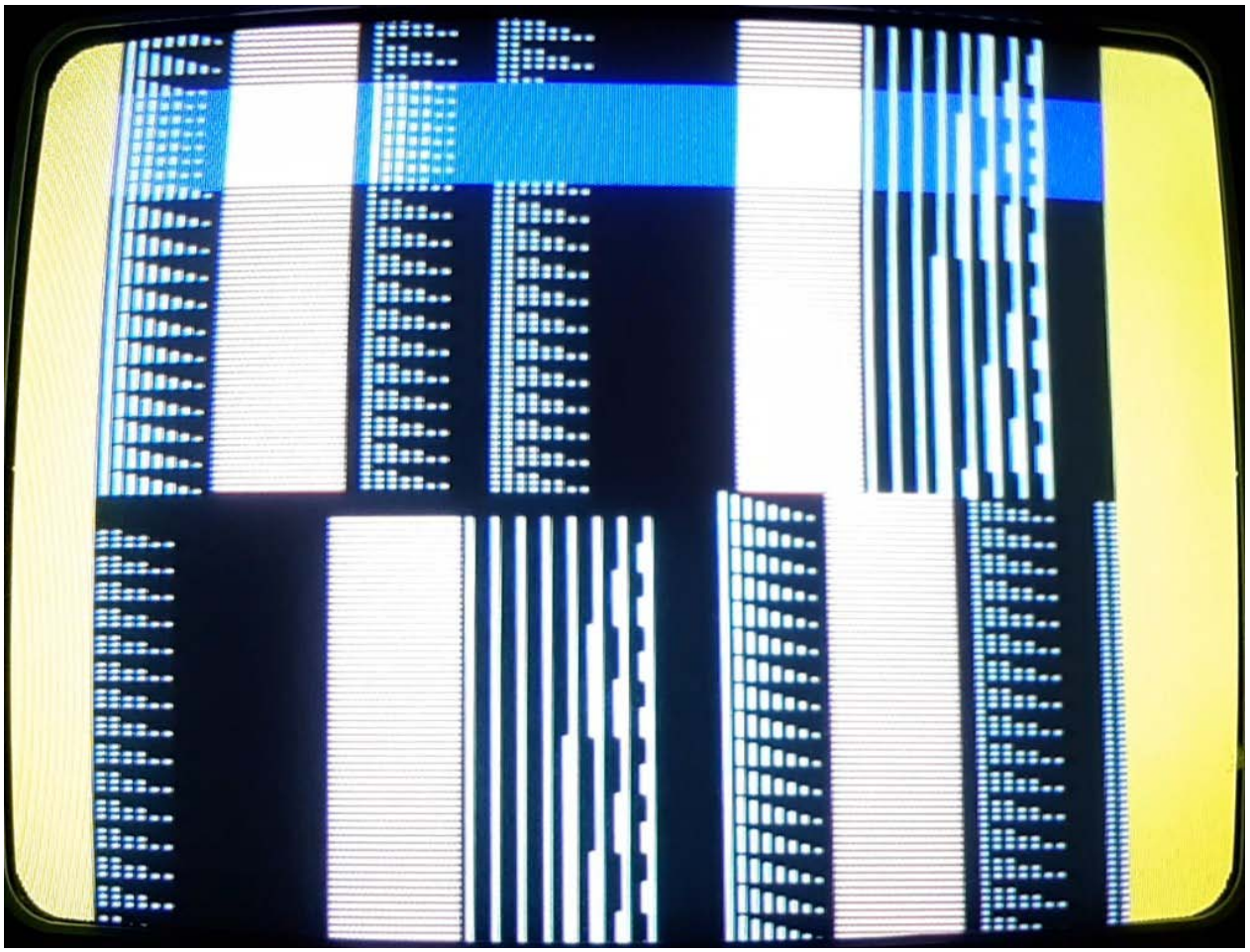

CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=2 >> UPD R9=6, R8=3 (+310S)
EXIT IVH MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=029 R5=007

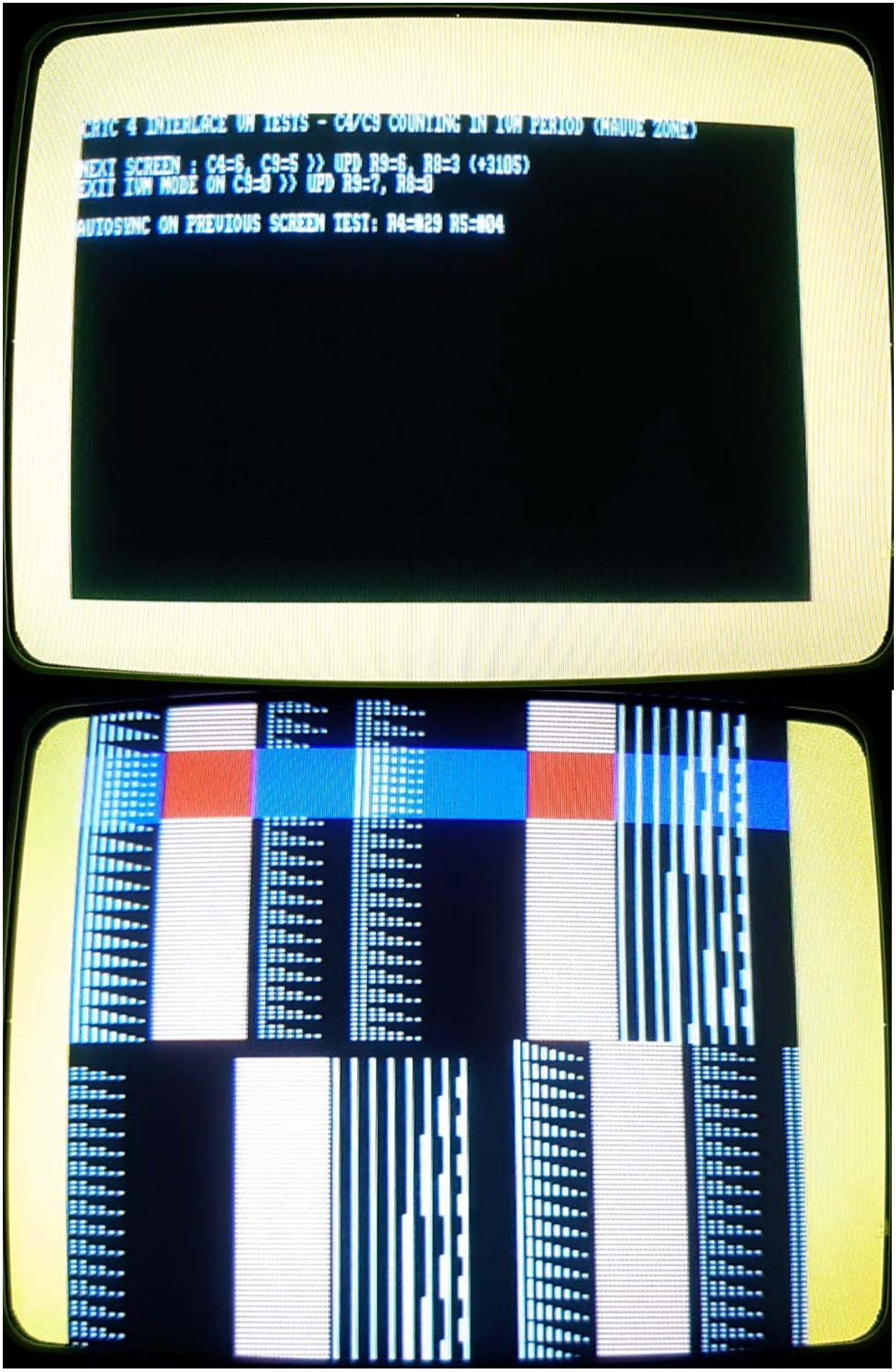



CRTC 4 INTERLACE ON TESTS - C4/C9 COUNTING IN IVW PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=3 >> UPD R9=6, R8=3 (+3105)
EXIT IVW MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#29 R5=#07

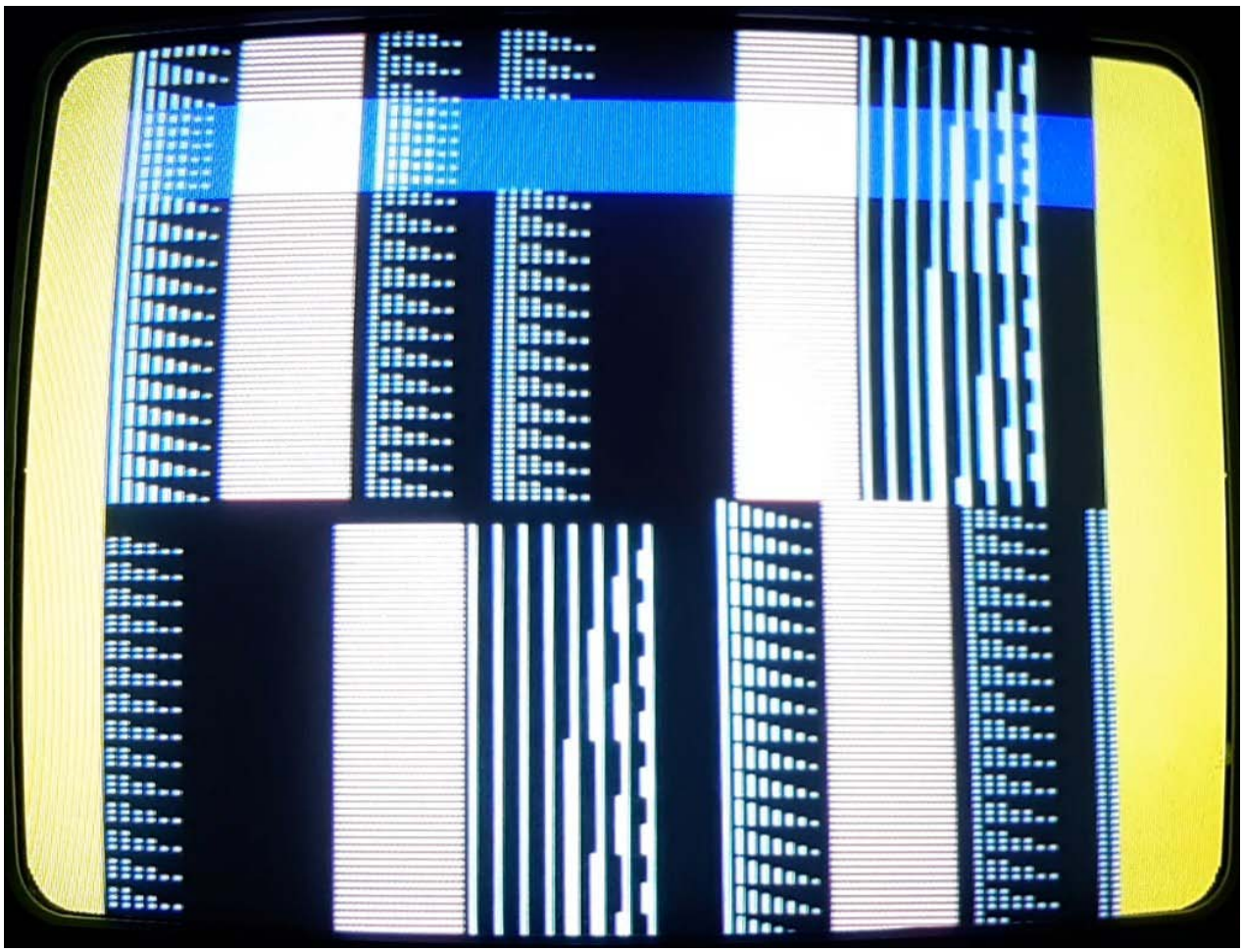



CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=4 >> UPD R9=6, R8=3 (+310S)
EXIT IVH MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#29 R5=#05



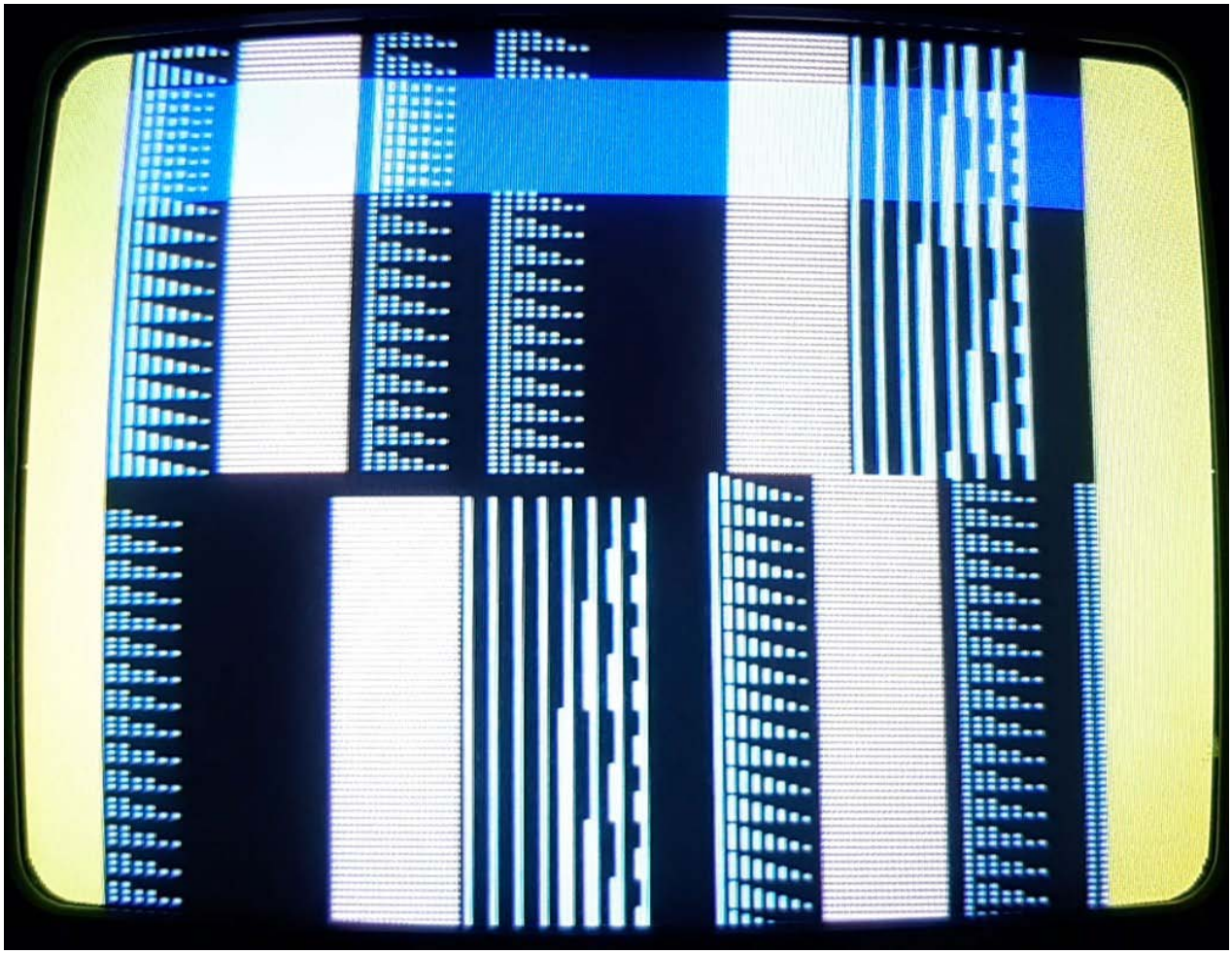

CRTC 4 INTERLACE ON TESTS - C4/C9 COUNTING IN IVW PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=5 >> UPD R9=6, R8=3 (+3105)
EXIT IVW MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=029 R5=004


CRTC 4 INTERLACE ON TESTS - C4/C9 COUNTING IN IVW PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=6 >> UPD R9=6, R8=3 (+310S)
EXIT IVW MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#29 R5=#03

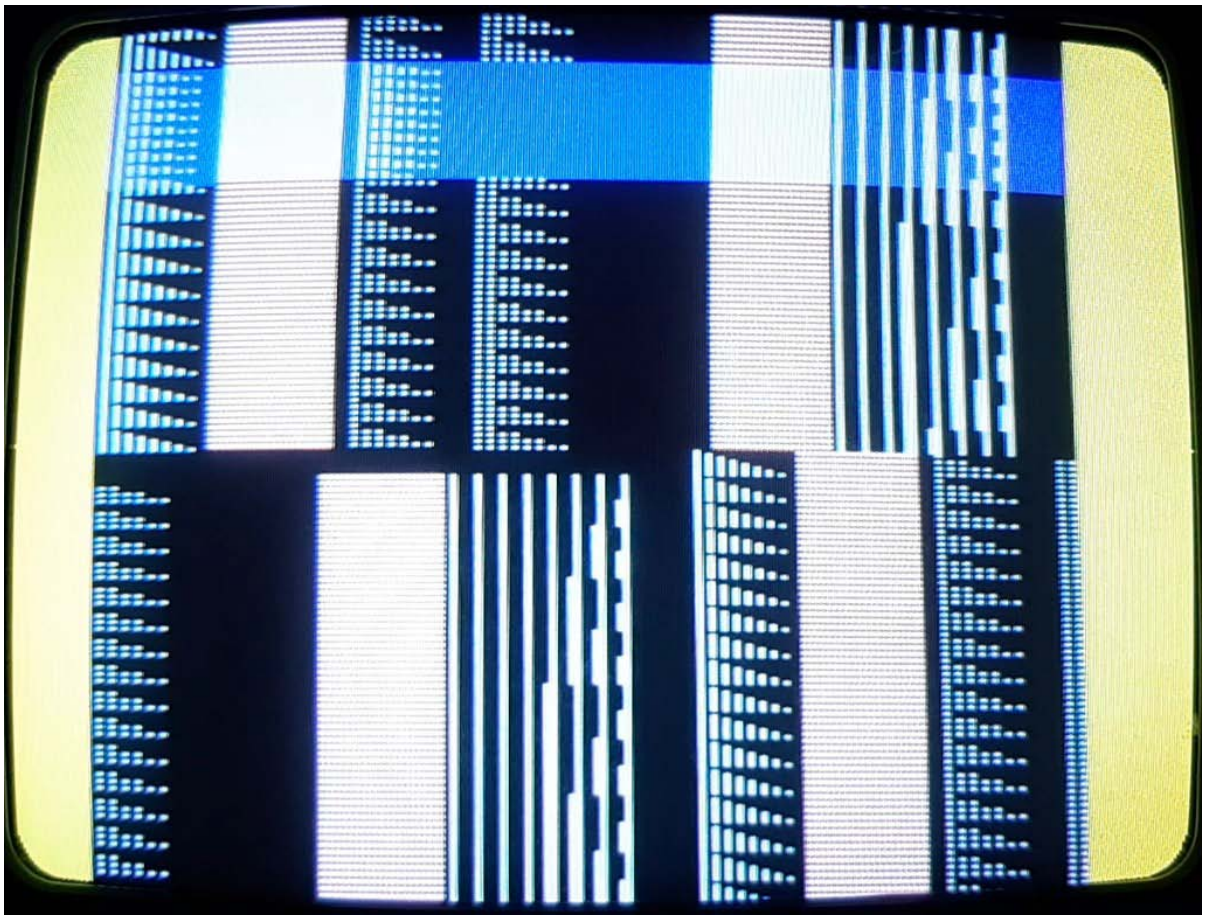



CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MODE 2ONLY)
NEXT SCREEN : C4=6, C9=7 >> UPD R9=6, R8=3 (+3105)
EXIT IVH MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#29 R5=#02


CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN ION PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=0 >> UPD R9=6, R8=3 (+310S)
EXIT ION MODE ON C9=2 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=029 R5=001

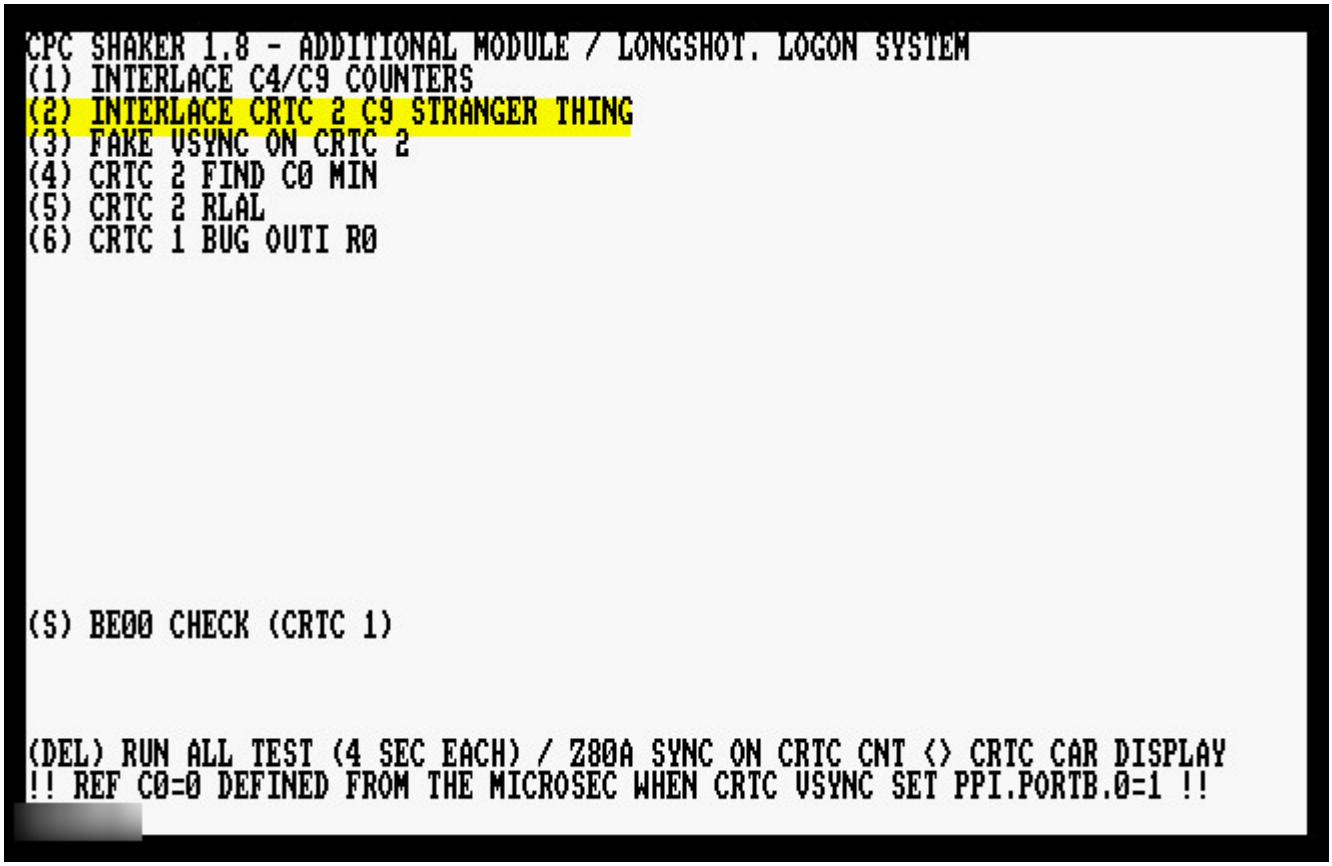



CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (WHOLE ZONE)
NEXT SCREEN : C4=6, C9=0 >> UPD R9=6, R8=3 (+310S)
EXIT IVH MODE ON C9=4 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#2A R5=#01




CRTC 4 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MODUE ZONE)
NEXT SCREEN : C4=6, C9=0 >> UPD R9=6, R8=3 (+3105)
EXIT IVH MODE ON C9=6 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#2A R5=#02

INTERLACE CRTC 2 C9 STRANGER THING



Only for CRTC 2

FAKE VSYNC ON CRTC 2

```
CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0





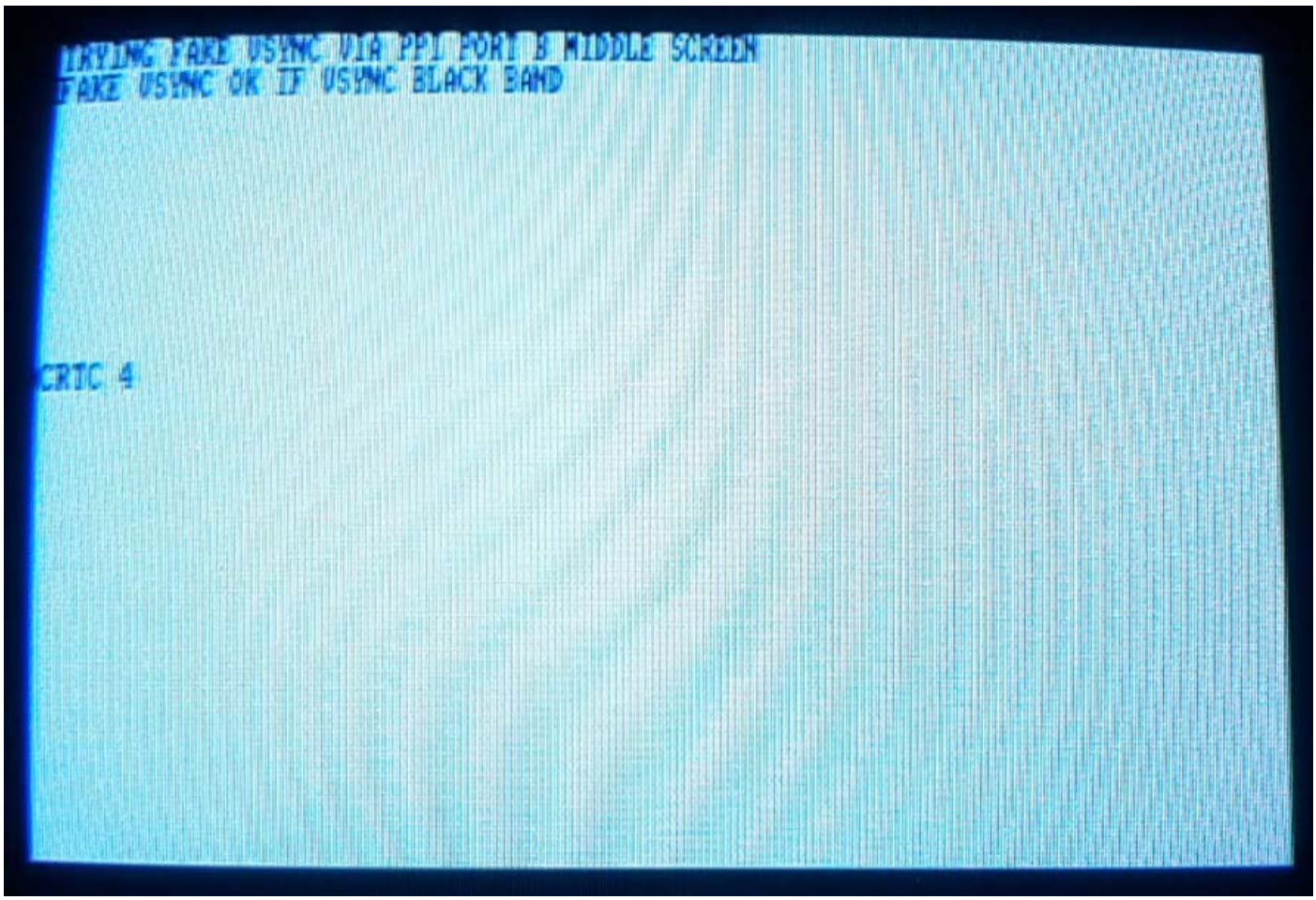




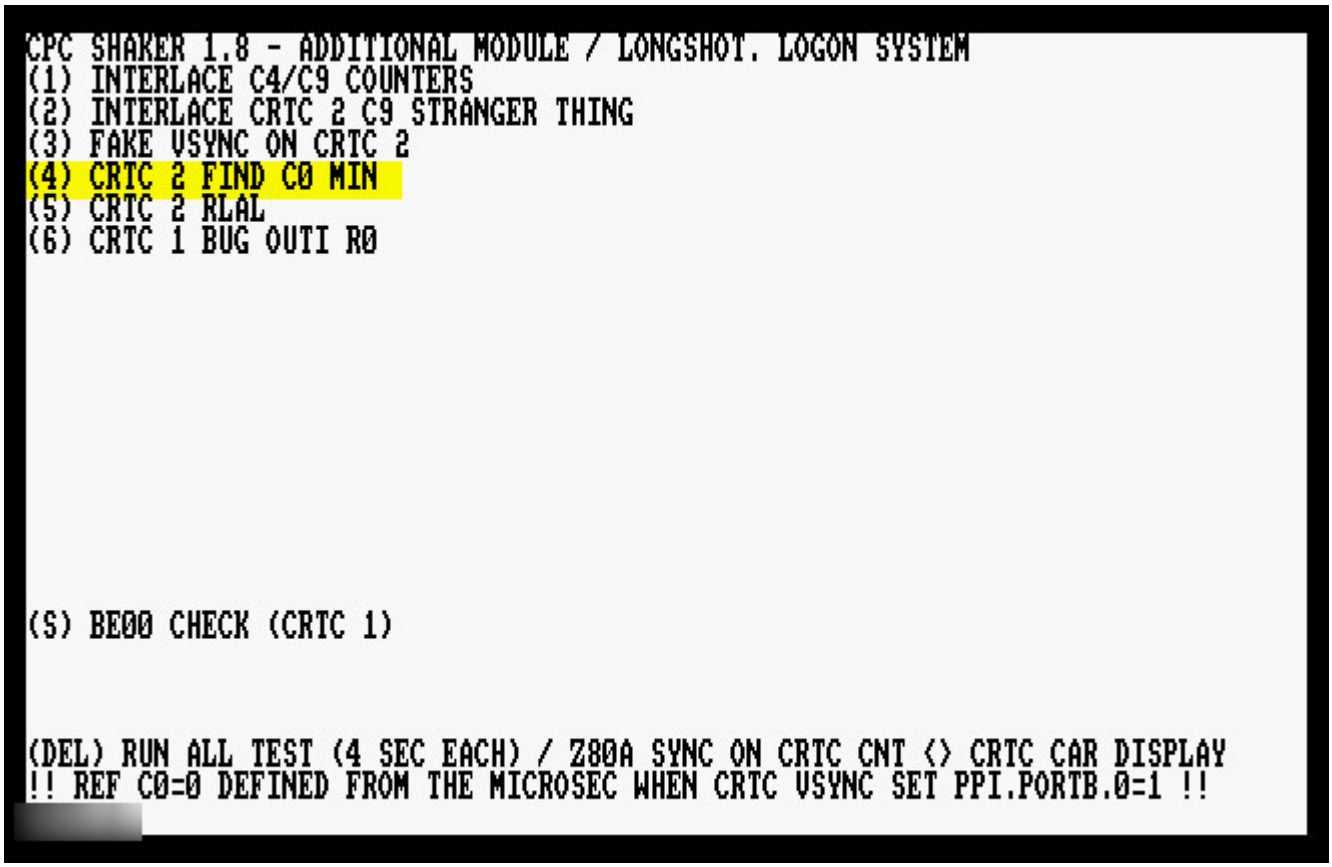
(S) BE00 CHECK (CRTC 1)



(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!
```

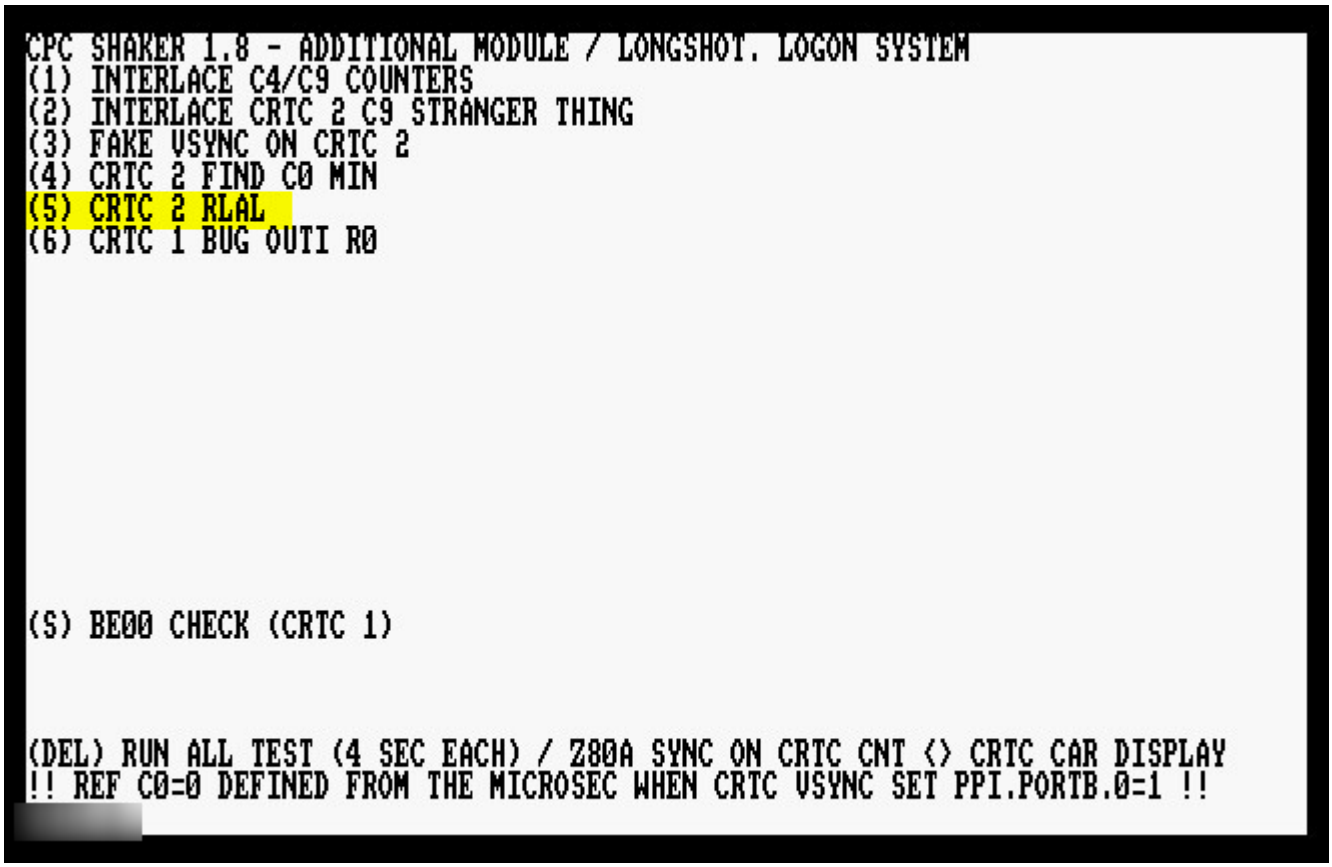


CRTC 2 FIND C0 MIN



Only for CRTC 2

CRTC 2 - 1 LINE RUPTURE



Only for CRTC 2

CRTC 1 – BUG OUTI R0

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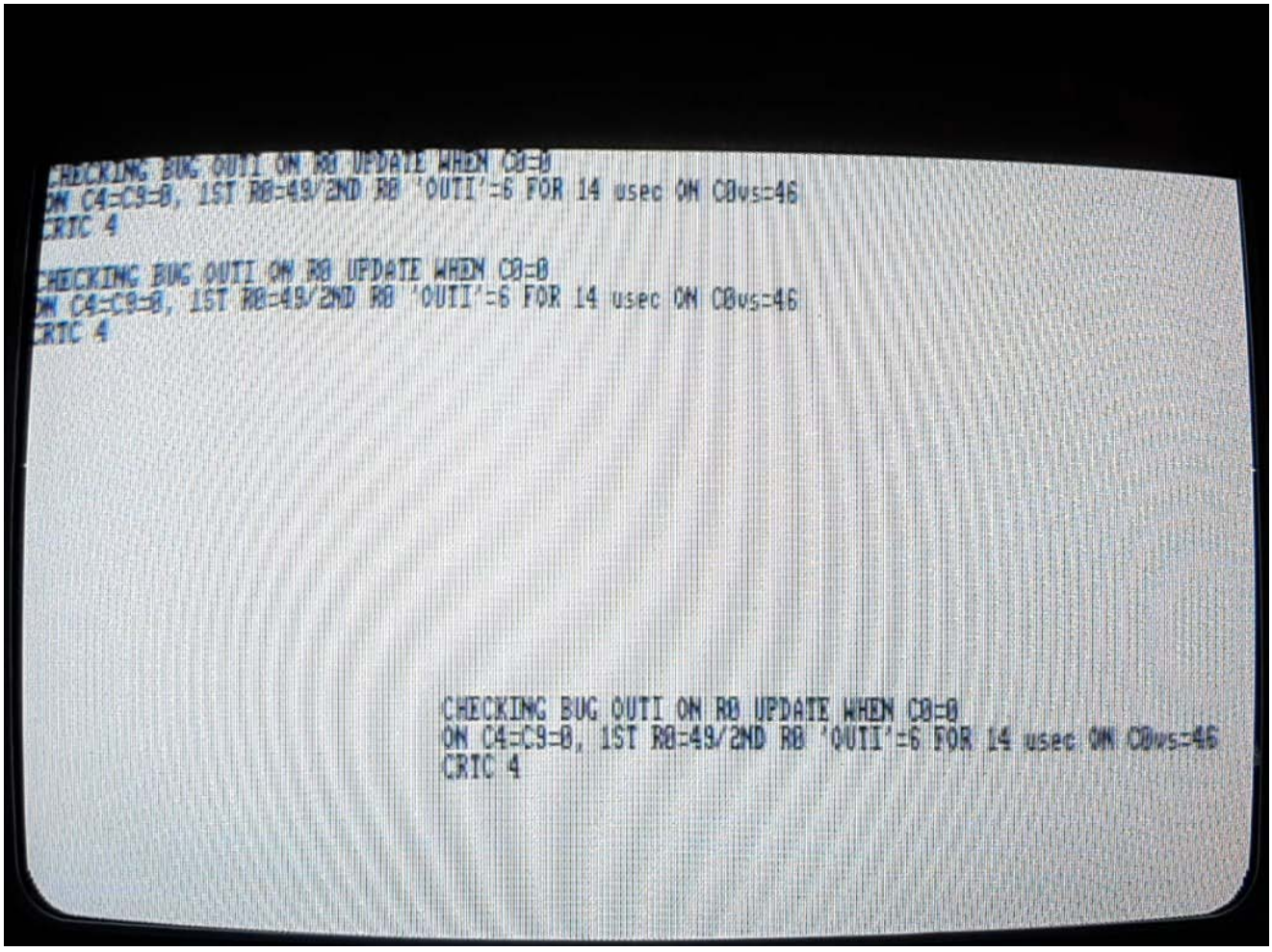
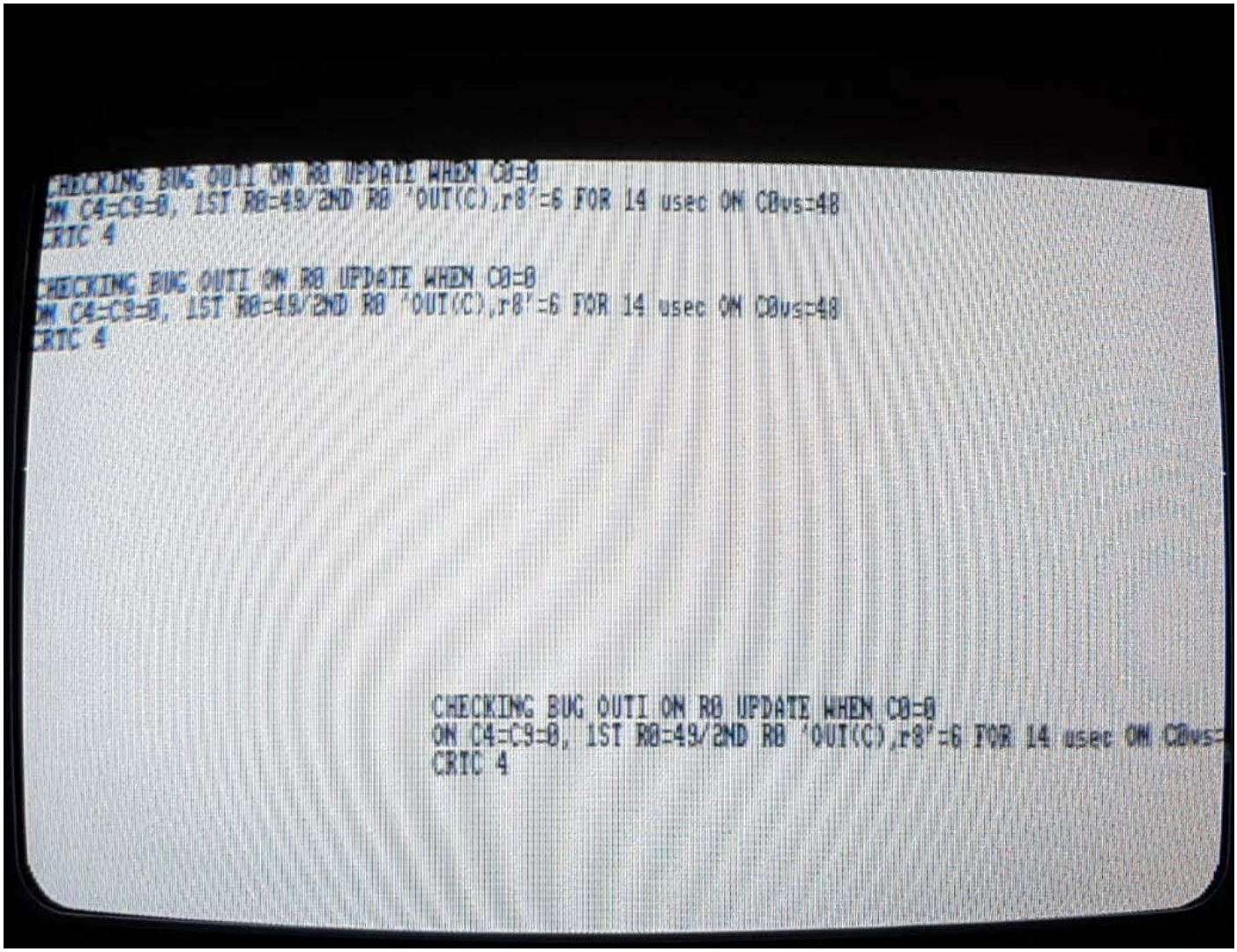
CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0



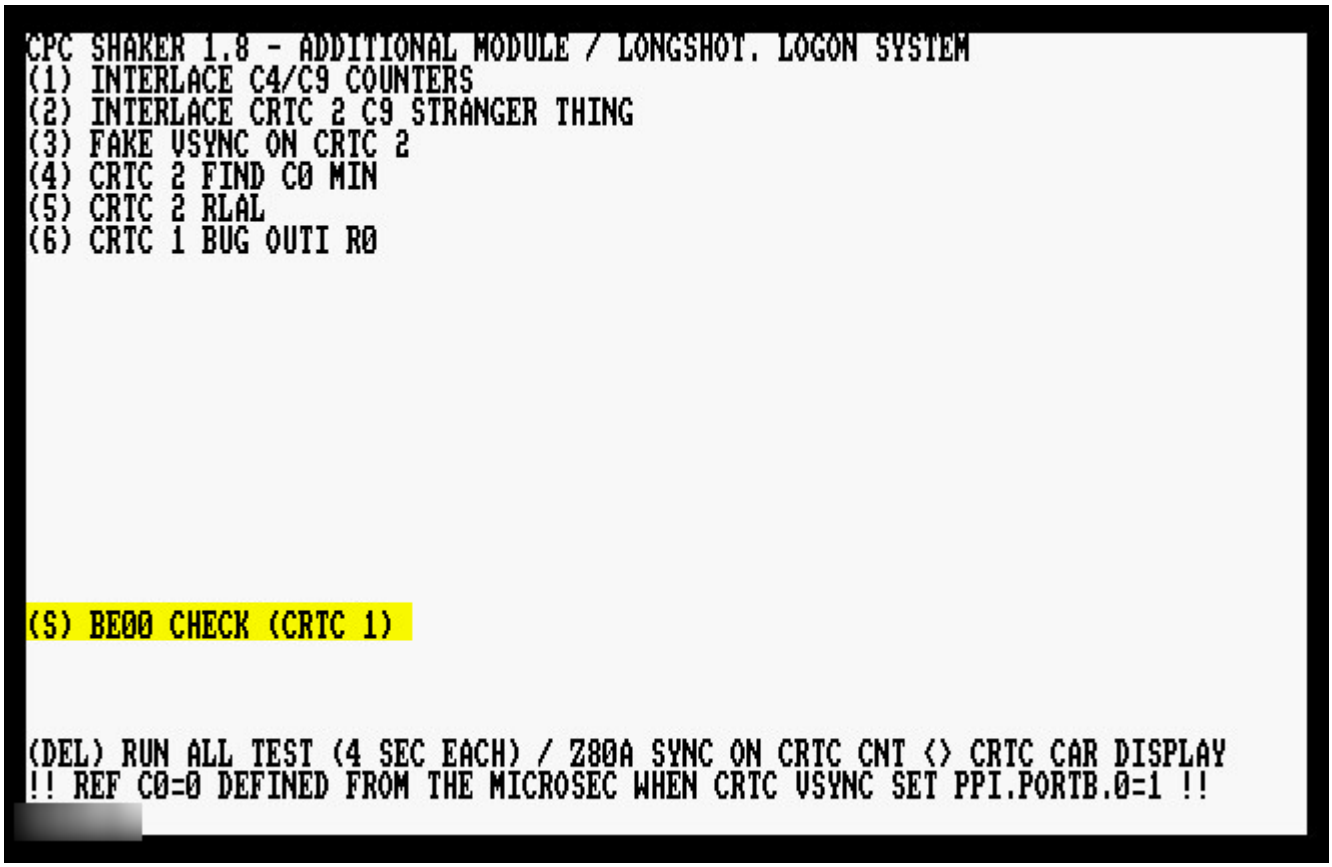

(S) BE00 CHECK (CRTC 1)


(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!
```




CHECKING BUG OUTI ON R8 UPDATE WHEN C8=0
ON C4=C9=8, 1ST R8=49/2ND R8 'OUT(C),r8'=6 FOR 14 usec ON C8vs=48
CRTC 4
CHECKING BUG OUTI ON R8 UPDATE WHEN C8=0
ON C4=C9=8, 1ST R8=49/2ND R8 'OUT(C),r8'=6 FOR 14 usec ON C8vs=48
CRTC 4
CHECKING BUG OUTI ON R8 UPDATE WHEN C8=0
ON C4=C9=8, 1ST R8=49/2ND R8 'OUT(C),r8'=6 FOR 14 usec ON C8vs=
CRTC 4

CRTC 1- BE00 CHECK



Only for CRTC 1