

TOSHIBA MOS MEMORY PRODUCTS

128K BIT (16K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM23128P

220667

DESCRIPTION

The TMM23128P is a 131,072 bit read only memory organized as 16,384 words by 8 bits with low bit cost, thus being suitable for use in program memory for microprocessor and character generator.

The TMM23128P is fully compatible with a 128K bits EPROM TMM27128D, so completely replace EPROM socket.

The TMM23128P also features an automatic

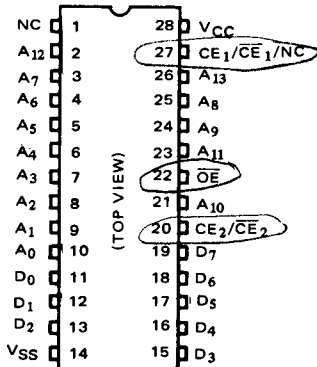
standby power mode. When deselected by Chip Enable (\overline{CE}_1 , $2/\overline{CE}_1$, 2), the operating current is reduced from 80mA (Max.) to 20mA (Max.). Output Enable (\overline{OE}) is effective in preventing data conflation of a common bus line. The TMM23128P is fabricated with ion implanted N-channel silicon gate technology. The TMM23128P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Fully Static Operation
- 16,384 word x 8 bit Structure
- Single 5V Power Supply
- $t_{ACC} = 200\text{ns}$ Max.
- $T_{opr} = 0 \sim 70^\circ\text{C}$
- $I_{CC\ op} = 80\text{mA}$ Max.
- $I_{CC\ sb} = 20\text{mA}$ Max.

- Input and Output TTL Compatible
- Three State Outputs
- Programmable Chip Enable
- Pin Compatible with EPROM TMM27128D
- 28 pin 600 mil. width DIP Plastic Package

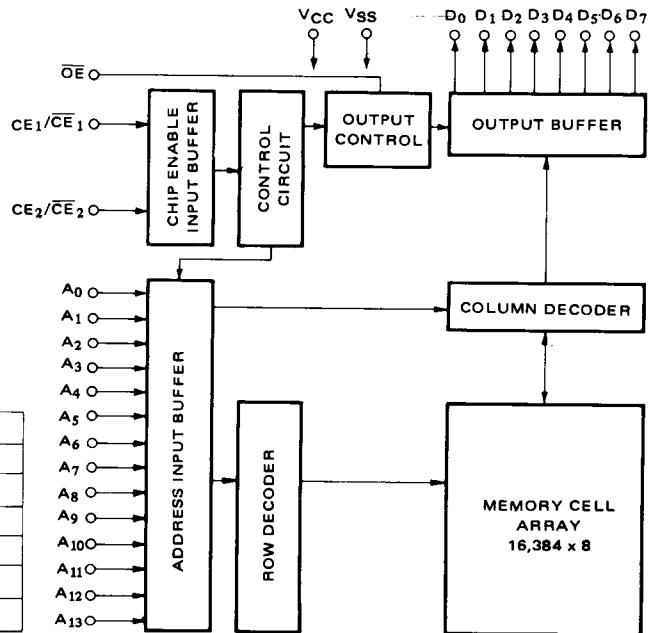
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$\overline{CE}_1 \sim 2/\overline{CE}_1 \sim 2$	Chip Enable Inputs
\overline{OE}	Output Enable Input
NC	No Connection
VCC	5V Power Supply
VSS	Ground

BLOCK DIAGRAM



TMM23128P

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN} , V _{OUT}	Input and Output Voltage	-0.5 ~ 7.0	V
P _D	Power Dissipation (T _a = 70°C)	1.0	W
T _{OPR}	Operating Temperature	0 ~ 70	°C
T _{STG}	Storage Temperature	-55 ~ 150	°C
T _{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	ITEM	MIN.	MAX.	UNIT
V _{CC}	Power Supply Voltage	4.5	5.5	V
V _{IH}	Input High Voltage	2.2	V _{CC} + 1	V
V _{IL}	Input Low Voltage	-0.5	0.8	V

D.C. AND OPERATING CHARACTERISTICS (T_a = 0 ~ 70°C)

SYMBOL	ITEM	CONDITIONS	MIN.	MAX.	UNIT
I _{IN}	Input Current	0V ≤ V _{IN} ≤ V _{CC}	—	±10	μA
I _{LO}	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC}	—	±10	μA
I _{OH}	Output High Current	V _{OH} = 2.4V	-400	—	μA
I _{OL}	Output Low Current	V _{OL} = 0.4V	3.2	—	mA
I _{CC ope}	Operating Current	Min. Cycle	—	80	mA
I _{CC sby}	Standby Current	Note 1	—	20	mA

Note 1: Standby state occurs when either CE₁/ \overline{CE} ₁ or CE₂/ \overline{CE} ₂ is disabled.

CAPACITANCE (T_a = 25°C, f = 1MHz)

SYMBOL	ITEM	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = AC GND	—	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = AC GND	—	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

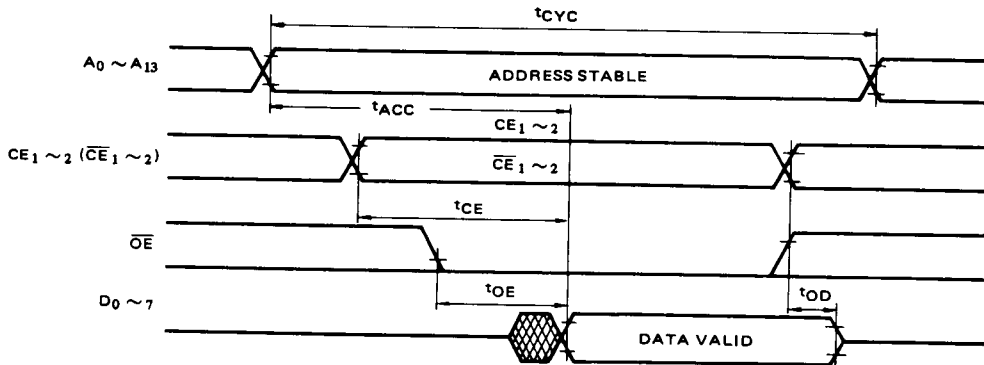
A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%)

SYMBOL	ITEM	MIN.	MAX.	UNIT
t _{ACC}	Access Time	—	200	ns
t _{CE}	Output Delay Time from CE _{1~2} /CE _{1~2}	—	200	ns
t _{OE}	Output Delay Time from OE	—	70	ns
t _{OD}	Output Turn Off Delay	—	60	ns
t _{CYC}	Cycle Time	200	—	ns

AC Test Conditions

- Output Load : 1 TTL + 100pF
- Input Rise and Fall Times (10% to 90%) : 5 ns
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Levels : Input : 0.8V and 2.2V
Output : 0.8V and 2.0V

TIMING WAVEFORMS



Note:

- 1) t_{CE} specifies the time interval of CE₁ ~ 2 (CE₁ ~ 2) to become active until it is actually being output.
- 2) t_{OD} is specified from OE or CE, whichever occurs first.

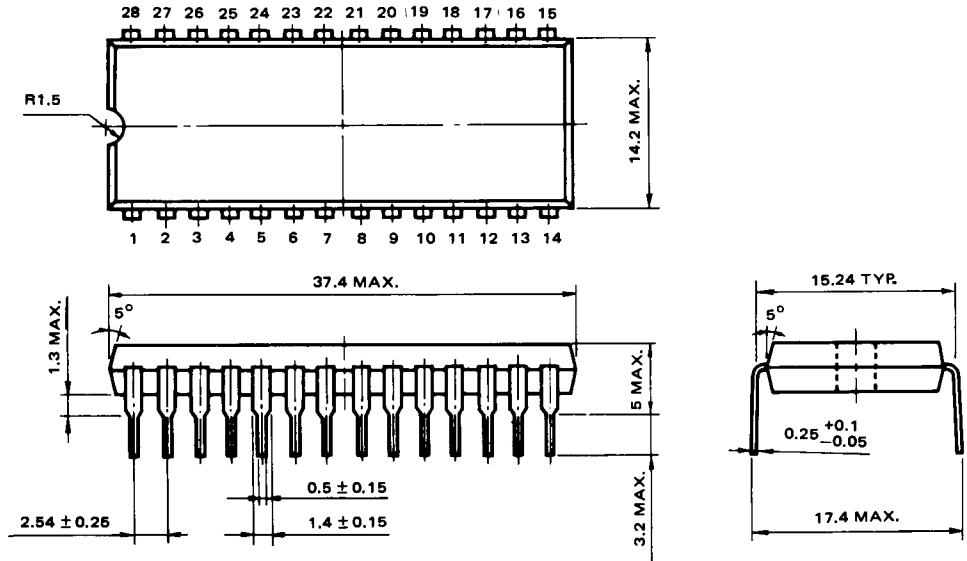
APPLICATION INFORMATION

TMM23128P has self substrate-bias generator internally. So a minimum 100μs time delay is required after the application of V_{CC} (4.5V to 5.5V) before proper device operation is achieved.

TMM23128P

OUTLINE DRAWINGS

Unit In mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.