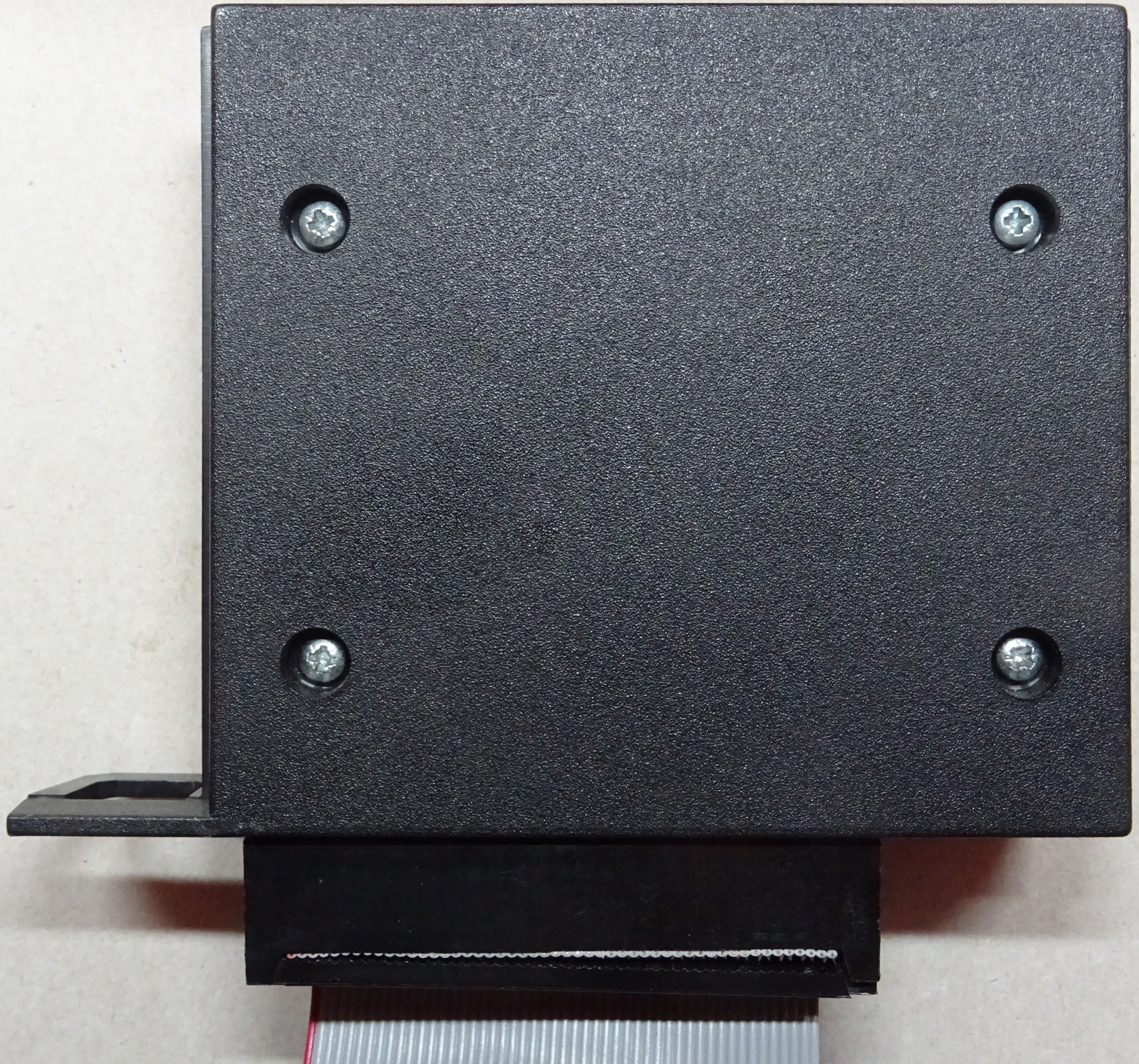
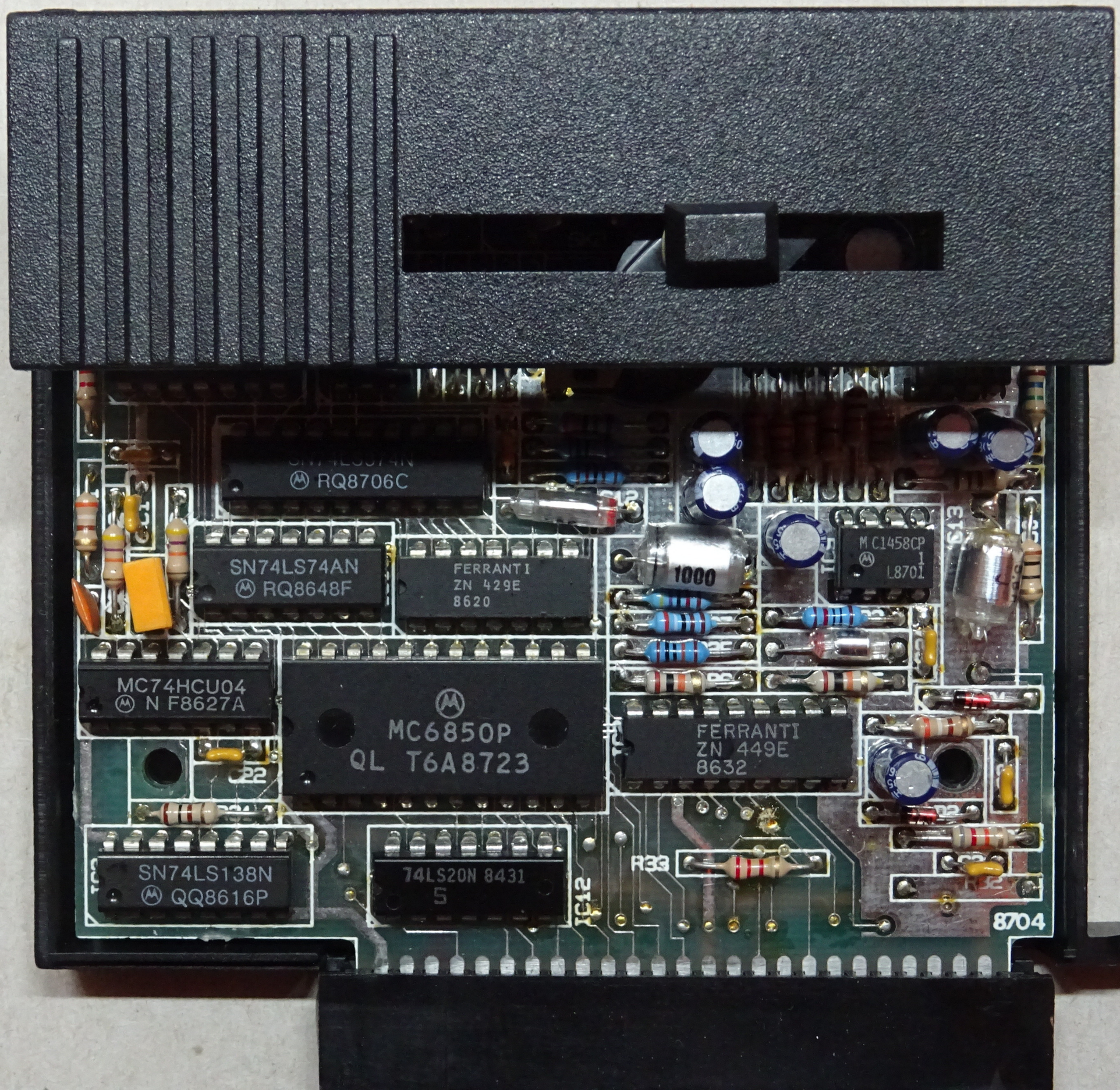

MUSIC
MACHINE

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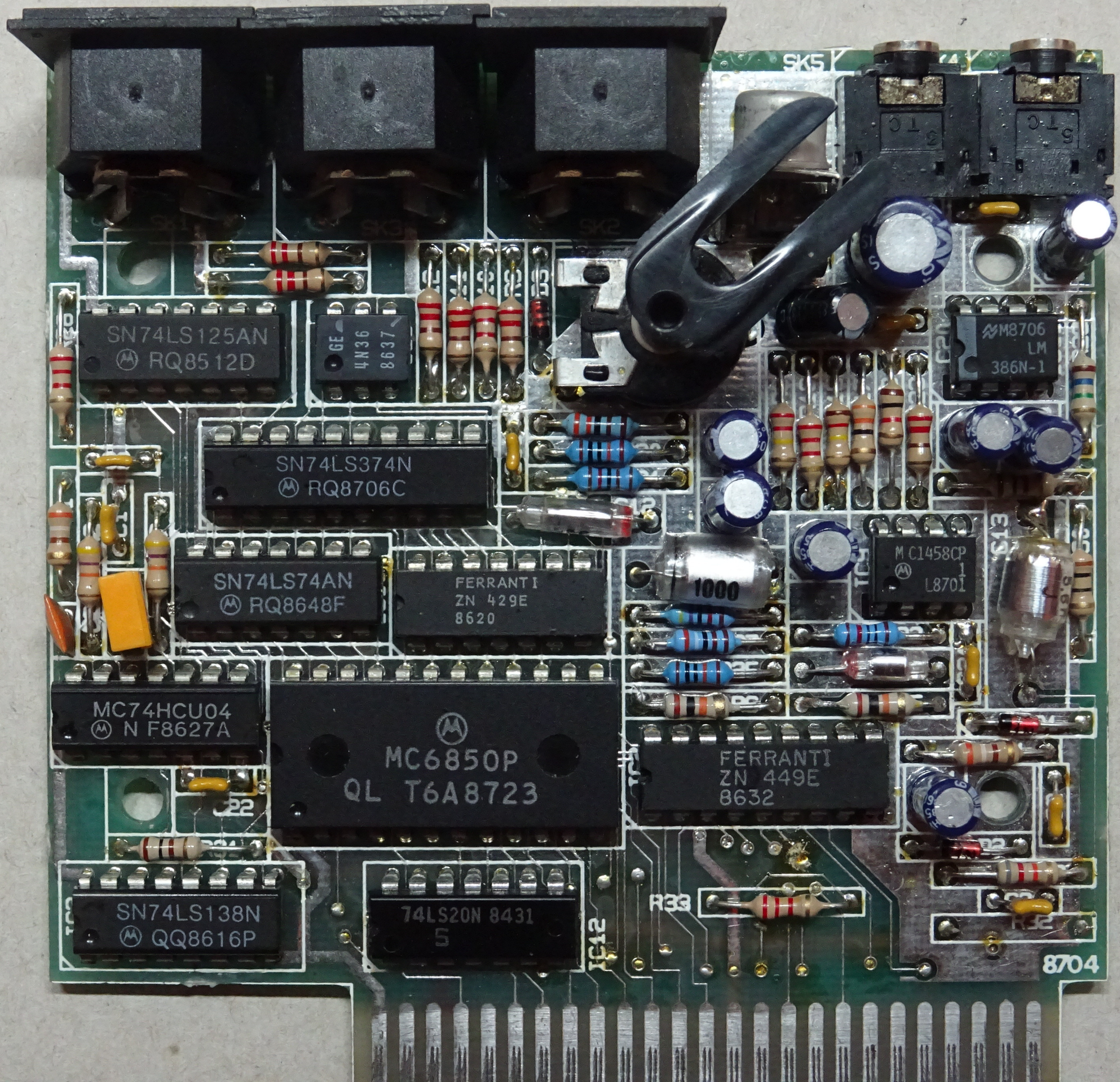
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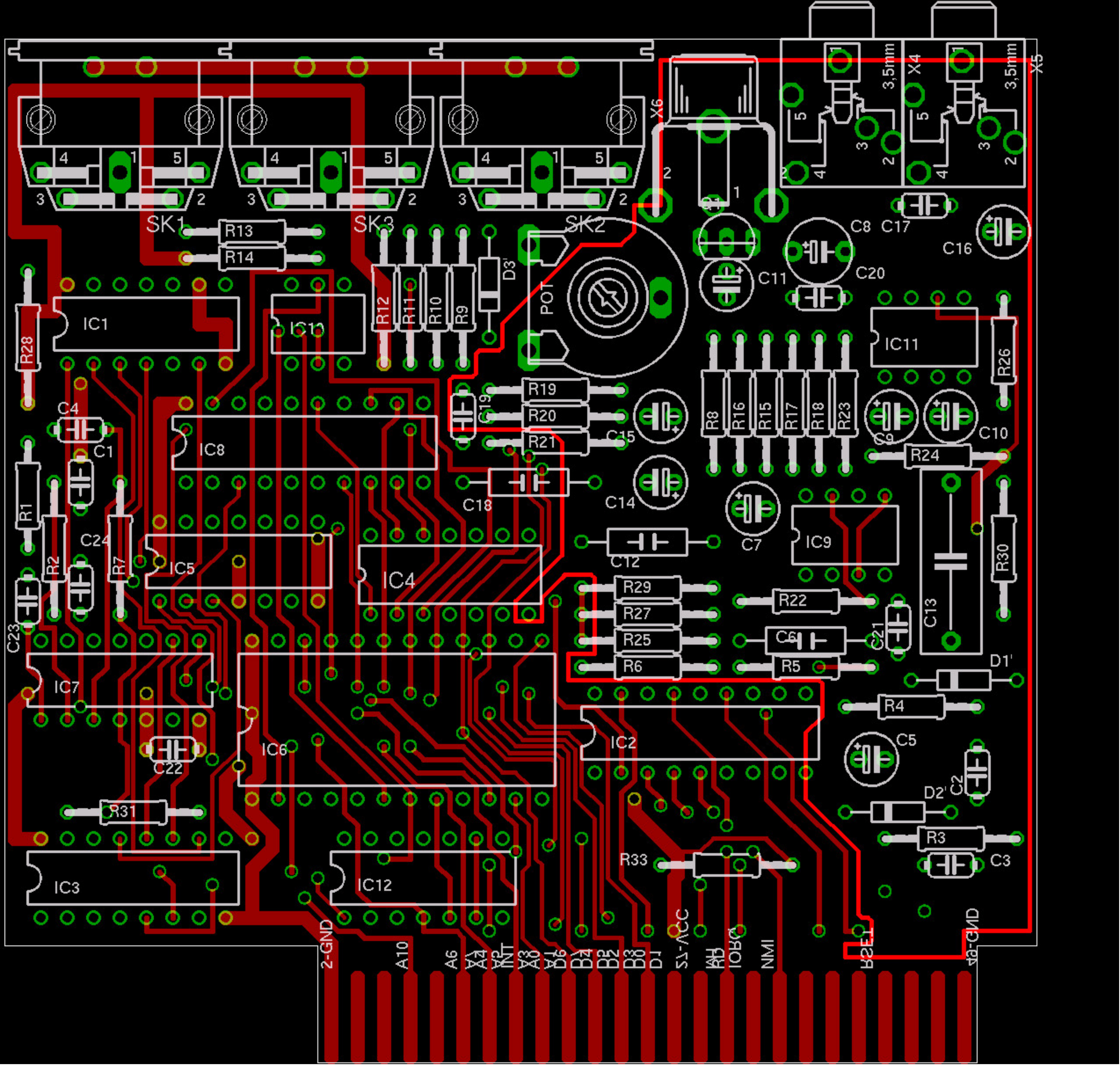
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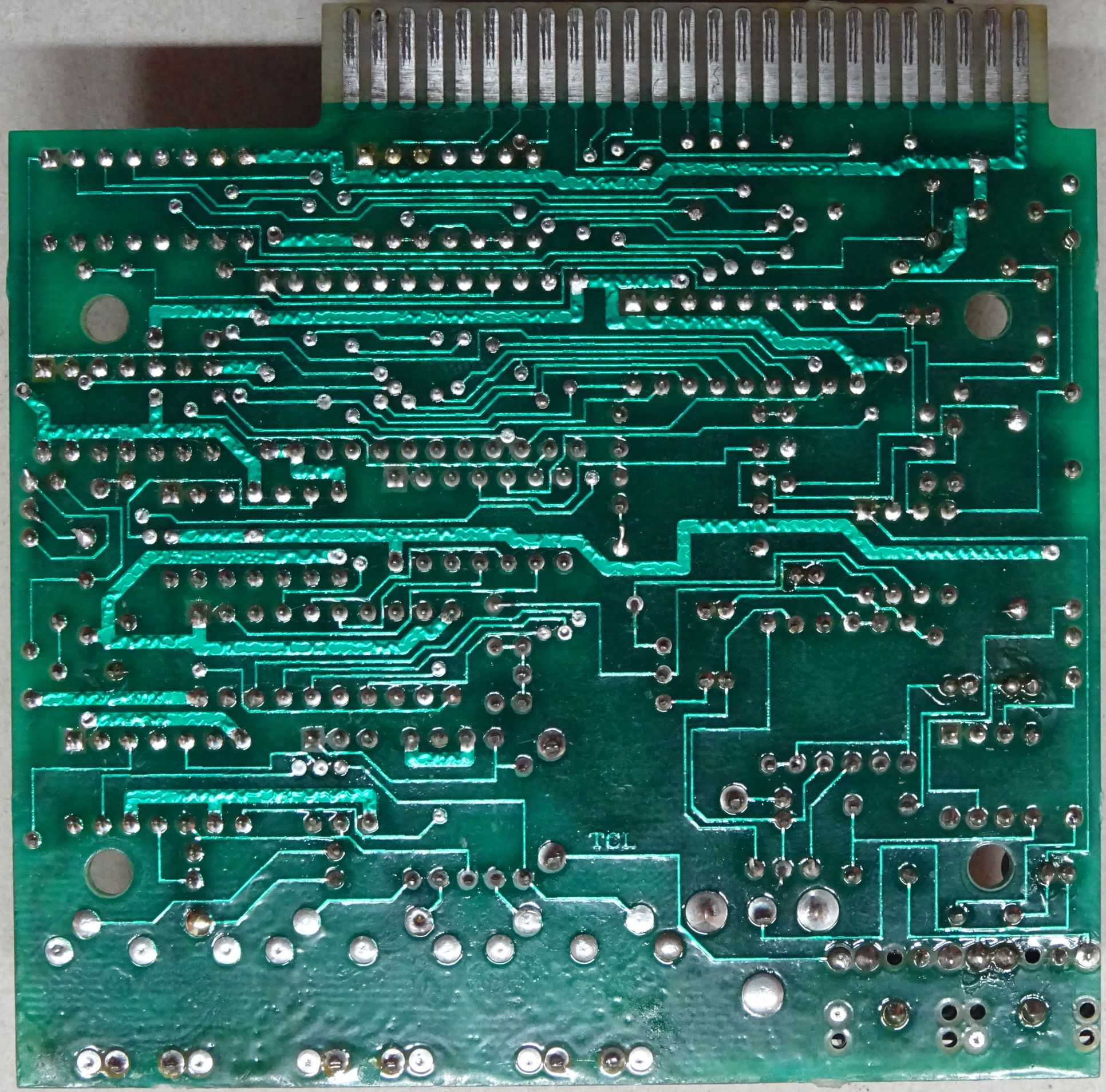
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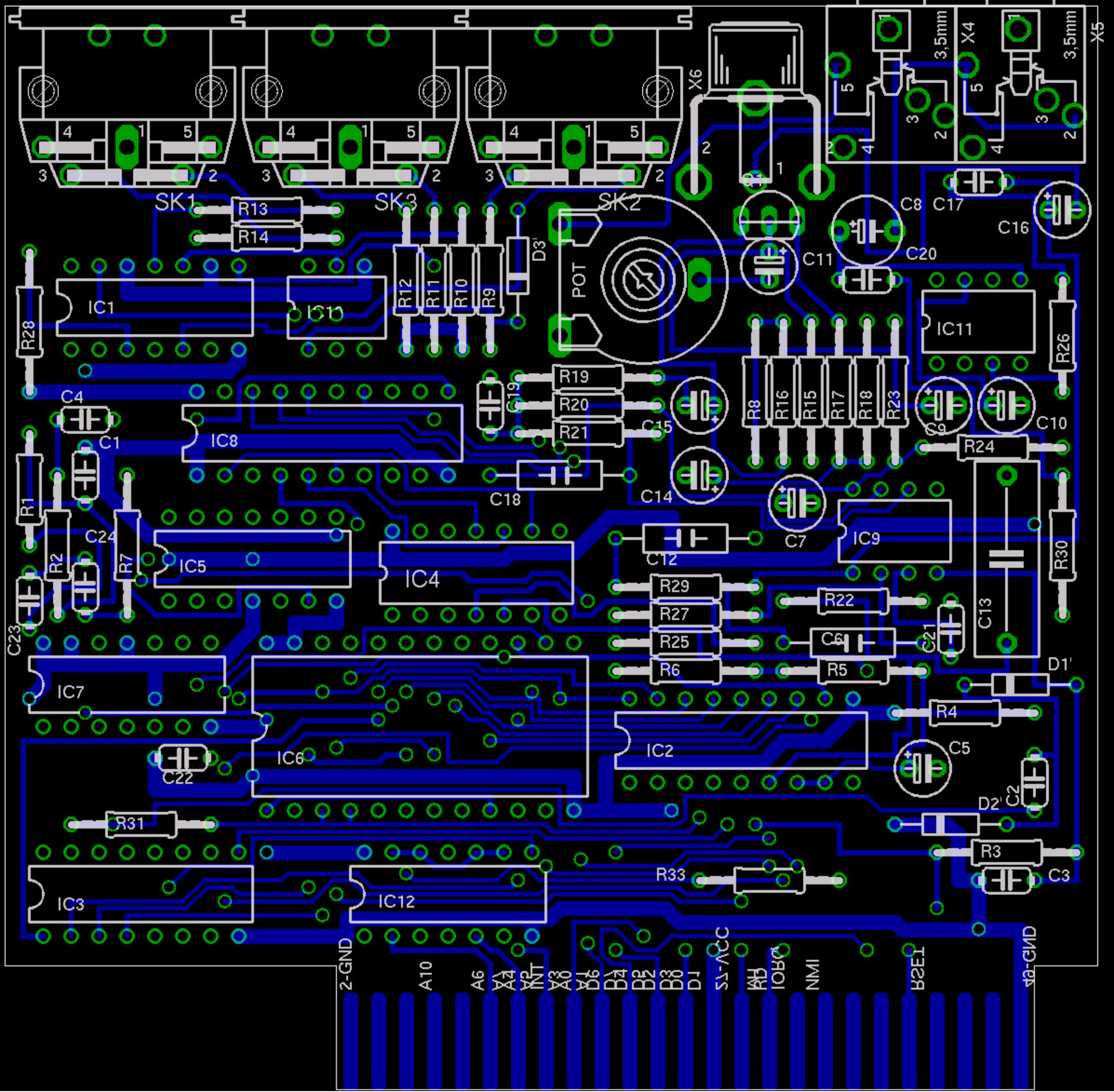
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IORQ
NMI
RSET
5a-GND

MUSIC MACHINE

THE COMPLETE HOME COMPUTER MUSIC SYSTEM

AMSTRAD

USER GUIDE

RAM Electronics and Flare Technology thank you for choosing one of our products; we hope that you have as much fun using The Music Machine as we did designing and building it.

About RAM:
RAM Electronics are manufacturers of a wide range of computer peripherals. Perhaps they are best known to you for their successful Spectrum Turbo joystick interface? If you want to know more about their other Spectrum hardware, just look out for their adverts in the home computer press or drop them a line at the address below.

About Flare:
All of the people who work for Flare used to work for Sinclair Research, so is it any wonder that The Music Machine (which Flare designed) is so good? Look out for future exciting products from this team.

Please remember to complete and return the guarantee card which is enclosed with The Music Machine. Not only will doing this help you (see your rights as a purchaser on the card), but it will enable us to keep you informed of additions to the range of Music Machine software from time to time. Thank you.

Whilst we have made every effort to ensure that the contents of this manual are accurate, we reserve the right to make hardware and software improvements from time to time.

RAM Electronics (Fleet) Ltd
Unit 16, Redfields Industrial Park,
Redfield Lane, Church Crookham,
Aldershot, Hants GU13 0RE

CONTENTS

0. CAN'T WAIT TO TRY IT, HUH?

This chapter is for those users who want to use the Music Machine before they read the manual. Only start here if you really know what you are doing. If you are in any doubt at all, read chapters 2 and 3 NOW. Do not hurt yourself by using an amplifier stupidly!

1. Power off everywhere.
2. Connect Music Machine to bus using ribbon cable supplied.
3. Plug in amplifier or phones.
4. Plug in microphone.
5. Power on computer (and amp if you are using one).
6. Load software.
7. Select function by pressing capital letter associated with menu choice.
8. Play the drum rhythm supplied by pressing 'P'.
9. Play the song supplied by pressing 'M' then '7' then 'Q' then 'P'.
10. Experiment, then read chapter 4.

1. INTRODUCTION

We believe that The Music Machine is the most powerful and exciting Amstrad add-on ever to reach the market. If your friends have already told you about the amazing things it can do, then skip this section of the manual and go to Chapter 2.

Q. What is The Music Machine?
A. It is a peripheral that plugs into the back of the Amstrad CPC 464, 664, and 6128 computers. There is also a version for the Sinclair Spectrum range of computers.

The machine lets you compose your own sounds, tunes, songs and drum rhythms - even if you don't know much about music at all. It also lets you do special effects.

Q. What sort of things can The Music Machine do?
A. This question would be easier to answer if it asked what The Machine cannot do!

It can do ALL of the following:

The Amstrad version of the Machine can act as a one-voice synthesiser and can also play the computer's programmable sound generator. By using the computer keyboard, it can play both simple notes and complex sounds. Effects can be based on the sound of a piano or an electric guitar or a trombone: in fact, it can be made to sound similar to any musical instrument you care to name.

You can even make it sound like your own voice (try N-n-n-n-nineteen for example!), or a dog barking, or a police car, or a window breaking. Any noise that can be picked up by microphone can be played back at different pitches by the computer.

Eight sounds are supplied on the software cassette with The Machine and this User Manual tells you how to make others.

The machine can be used to make drum sounds. You can play up to three drums simultaneously from a selection of eight. If you don't like

any of the percussion sounds supplied, you can use your own. Perhaps you would rather replace the tom-tom with a telephone ring? Simple!

You can compose songs from individual bars of music. You can edit bars on the screen, and merge them with bars from other tunes to make new songs. You can build up a library of tunes, record and save sounds and instruments, and record and save drum sounds and rhythms.

The Music Machine can be used as a digital delay box. Play music or speak through the microphone and you will be able to alter the delay rate (short or long echoes, for example) of the sounds as they come through your amplifier's loudspeaker.

If you have a MIDI synthesiser keyboard, you can plug this into The Machine in order to send and receive MIDI data. This means that your own sounds and effects can be played by The Machine by hitting keys on the synthesiser keyboard.

Also, sounds produced by The Machine can be mixed with the synthesiser's own voices. It is possible to send notes from The Machine to the MIDI keyboard, (or, because several MIDI devices can be plugged in simultaneously, some other MIDI peripheral).

The Machine enables songs created with the screen editor to generate MIDI data, and will allow you to play MIDI together with your drum rhythms. At the same time as The Machine sends songs to the synthesiser and plays the drums, you can play accompaniments on the keyboard.

Q. What can I plug into The Machine?
A. The Machine has the following connectors:

Amstrad bus connector
An audio-out phono socket for connection to your hi-fi
An earphone socket so that you can use your personal stereo headphones
A socket into which you plug the supplied microphone for capturing sounds

MIDI in, out, and through for hooking up MIDI devices such as synthesisers or sequencers.

Q. What will the software let me do?
A. All of the things described above. Example bars, songs, sounds and rhythms are supplied with the tape in program form.

If you have bought a cassette version of the software, on the reverse side of the tape is an audio track that you can play through a tape-recorder in order to hear what The Machine can do. We hope to bring you other clever and sophisticated software in the future.

Q. Is there anything else like the Music Machine available for the Amstrad?
A. Some suppliers sell peripherals that do one or two things that the Machine does, but you can't easily use lots of their peripherals together. And even if you could, you would have to spend about three times as much.

Q. Can the Music Machine be used with the Amstrad's programmable sound generator?
A. Yes. It can play one instrument and several percussive pre-selected sounds.

2. PLUGGING EVERYTHING TOGETHER

Because The Music Machine can do so many things, we have provided you with a range of sockets into which you can plug various pieces of equipment. However, before you start sticking plugs into sockets, you must connect The Music Machine to your Amstrad.

If you have never used an Amstrad before, then please read your User Instructions before going any further.

2.1 Connecting The Music Machine to your Amstrad

Although it is not absolutely necessary, we recommend that you unplug the monitor and keyboard leads from your Amstrad before you start. This will make things easier for you when you assemble your music system.

However, you MUST unplug the mains cable from your computer and remove any peripherals from the bus before you start. (Did you know that the most common way of blowing-up computers and peripherals is by plugging and unplugging them while the power supply is connected? Don't ruin your computer system before you've had a chance to use your terrific Music Machine!)

Here we go:

(a) With the mains disconnected from your Amstrad connect the ribbon cable supplied onto the front of the Music Machine and then push the other end onto the expansion bus edge connector. Look at the user instructions if you aren't sure where the expansion bus connector is.

(b) Re-connect the Amstrad monitor and keyboard.

(c) Switch on the power to your computer.

You should now get the standard Amstrad copyright message screen.

(If you don't get this screen, switch off the power, disconnect The Music Machine, then try the computer by itself. If the copyright message screen still does not appear, then you may not have plugged everything in and switched on properly. See your Amstrad User Instructions.

You are now ready to plug other leads in.

Please remember the golden rule: ALWAYS UNPLUG THE POWER SUPPLY LEAD BEFORE ADDING OR REMOVING PERIPHERALS THAT USE THE EDGE CONNECTOR.

2.2 Plugging in The Music Machine and an amp/phones/mic

In order to hear the fabulous quality of the sound produced by The Music Machine, we have supplied you with both an amplifier socket and a headphone socket.

Figure 1 shows you the position of the phono socket which carries the audio output signals. Into this can be plugged a lead to your hi-fi amplifier, or maybe a guitar amplifier. Because there are so many different amplifier plugs and sockets on the market, we have not been able to supply leads that will suit everybody's equipment. However, it should not be difficult for you to get an appropriate lead from either your local hi-fi supplier or an electrical shop.

IF YOU ARE IN ANY DOUBT AT ALL ABOUT WHAT TO DO, GET HELP FROM AN ADULT OR A SPECIALIST. NEVER FOOL AROUND WITH ELECTRICITY AS IT CAN KILL YOU. Remember that we cannot be held responsible for any dangerous things that you do. Please be careful!

Before you connect your hi-fi to The Music Machine, turn the volume right down on the amplifier, plug the lead into a spare socket (probably marked 'AUX' or 'Auxillary', and select the appropriate input on the amplifier's controls. If you are using a guitar or PA amp, it should be obvious which socket you should use - but again, don't forget to turn the volume down.

If plugging The Machine into an amplifier is too much like hard work right now, then why not use a pair of personal-stereo headphones? Simply plug these into the headphone socket shown in Figure 1.

Finally, plug the supplied microphone into the small jack socket shown in Figure 1. Make a mental note of the position of the gain control (this is a bit like a volume control) on the top of The Music Machine, as you will need to use this as soon as you start experimenting with sounds.

Don't worry about the three DIN sockets (marked MIDI in, out and through) for the time being. We'll come back to these later.

2.3 Loading the software from the tape or disk

Almost ready now! As soon as you've loaded the program, you can begin your music-making.

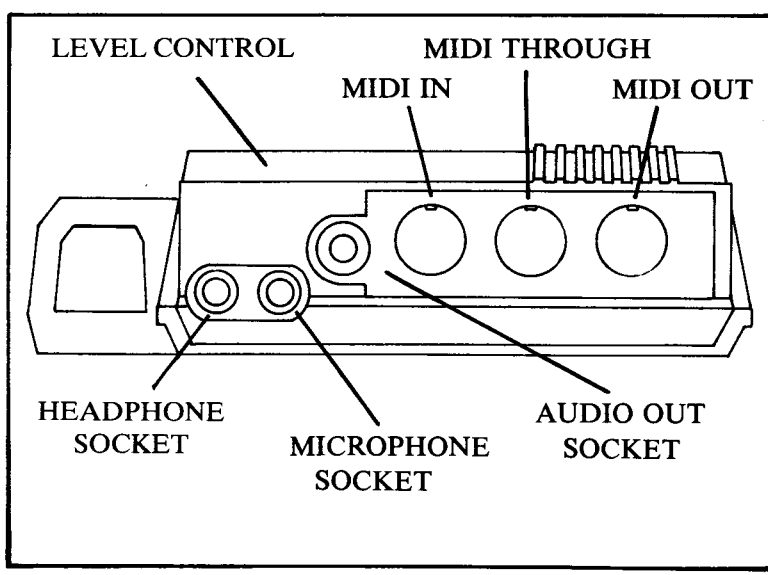


Figure 1, Music Machine Connector details

Tape loading

(a) Place the cassette in your player with side A uppermost.

(b) Rewind the tape to the beginning of side A.

(c) Type RUN "MM" and press RETURN.

If you get stuck, read your Amstrad User Instructions.

If you see The Music Machine title screen appear on your monitor, you will know that all is well. You should wait several minutes for the main program to load after which you will see the Main Menu screen shown in Figure 2.

(If you cannot get either the title screen or the Main Menu to load, do not despair. Just wind the tape back to the beginning, and try to load the program again. See your User Instructions for more help.)

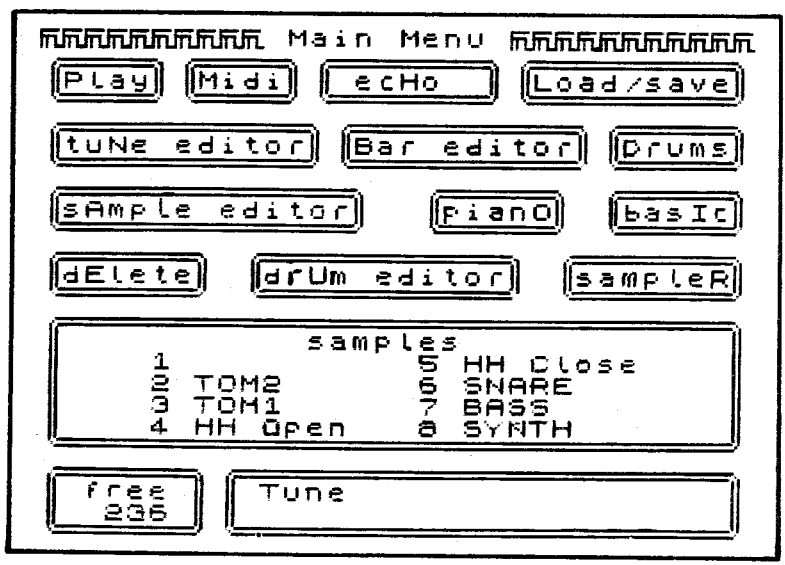


Figure 2, First screen of Main program. Main Menu

Disk loading

Insert the disk with side A uppermost, type RUN "MM" and press RETURN. The program will load and run automatically in about 20 seconds.

3. GETTING STARTED QUICKLY

Now that you've got everything plugged together, you probably want to start making sounds, playing songs, and playing the drums straight away.

That's what this Chapter is for. When you've tried all the things described here, you can spend a bit of time later on reading the detailed descriptions of what The Machine can do in Chapter 4.

So you are all plugged in and the software has loaded and looks like Figure 2? Good.

3.1 Playing the sounds, rhythms, and songs supplied

The way in which you make selections from the menu screens is to press the key on the Amstrad keyboard associated with the capital letter shown in the panel you want to choose.

Example: If you want to play the piano, simply press 'O'. Try that now. The screen will look like that shown in Figure 3.

To get back to the Main Menu straight away, simply press 'Q' for Quit. Try that now.

Playing the tune:

Select 'Play' (by pressing 'P') and you will hear the tune whose name is shown in the panel at the bottom of the screen.

(What, no sound? Perhaps you have forgotten to turn up the volume on your amplifier, or maybe you haven't connected the leads properly?)

You can play the tune supplied with the software through your computer's internal programmable sound generator (psg). To do this, select 'M' from the Main Menu, key '9', then 'P' for Play. Adjust the computer's volume control to the level you want. You

can also play the drum rhythm through the psg, by keying '8' then 'P' for Play. The sounds produced by the psg are pre-selected and cannot be altered. They sound very different to the voices produced by the Music Machine. To interrupt a tune or rhythm, press ESCAPE.

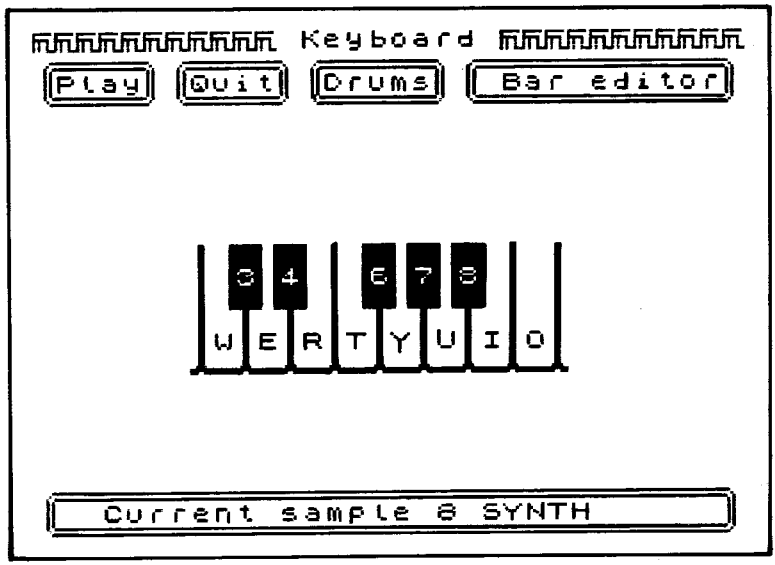


Figure 3, The Piano Keyboard

Playing the piano:

Select 'pianO' and the screen will change to the one you've already seen in Figure 3. The numbers and letters shown on the screen correspond to the notes that you can play from the Amstrad's keyboard.

Press some of the 'musical' keys. Doesn't sound much like a piano, does it? That's because you are actually playing one of the sample voices which makes the sound called 'Synth' every time you press a key. We'll tell you how to make your own musical-instrument sounds later on.

Changing the sound:

Before we record some new sound effects, let's change the sound that the 'piano' plays. Select 'Quit', and from the Main Menu select 'sAmple editor'.

What you are now looking at is the waveform of the sound that plays 'Synth'. This is shown in Figure 4. Don't worry about this screen too much because we'll tell you more about it in Chapter 4. Whilst you're here, you might as well press 'Play' again just to see that you can hear the sound from more than one screen.

Select 'Current sample' and you will see that the title in the bottom panel clears and a red flashing cursor appears to prompt you for an input.

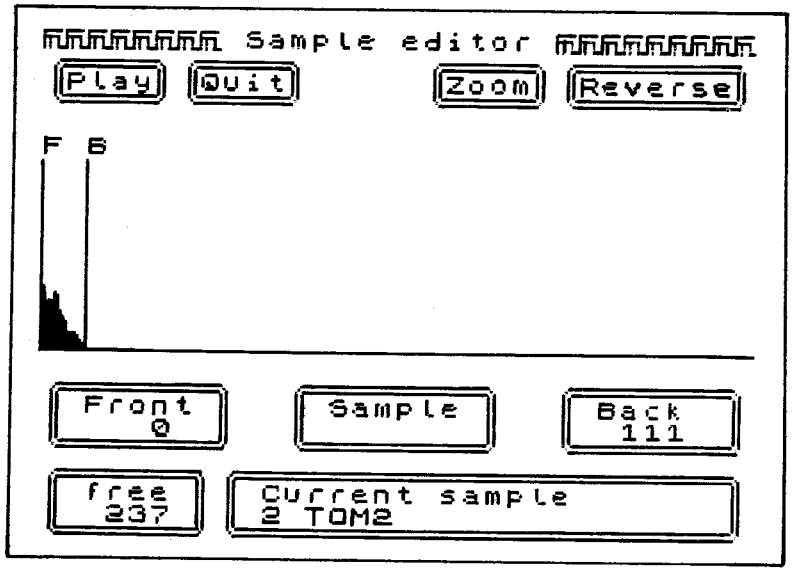


Figure 4, The Sample Editor

Type '7' and press ENTER. The bottom panel will now read '7 Bass'. Note that this is one of the sample sounds listed in the big panel on the Main Menu screen. Press 'Play' again and listen. See how easy it is to change instruments!

Return to the Main Menu by selecting 'Quit', and then go to the 'pianO' screen. Press a few of the 'keyboard' keys on your Amstrad and listen to the difference. 'Quit' back to the Main Menu and select 'Play' before you go on to the next exciting instalment.

Playing the drums:

From the Main Menu, select 'Drums'. The screen will look like that shown in Figure 5. If you want to hear the rhythm that we have supplied, you must ensure that the drum channel, rather than the music channel, is selected on the Midi screen. To do this, 'Quit' to the Main Menu, select 'Midi', and then key '4' to redirect the output to the earphone and phono sockets. 'Quit' back to the Main Menu and just select 'Play'. If you want to tap out your own rhythm, select 'Drums' then press the keys on the Amstrad's keyboard that are shown on the screen. (To stop the rhythm playing, press ESCAPE.)

Want to change the drum sound? Well you can either play all the eight sounds that correspond to the keys shown in Figure 5, or you can make a new sound. Because this is a bit more complicated, we'll describe how to do it in a moment.

Echo and reverberation:

The echo effect is created by a delay that's adjustable from one thousandth of a second to around one whole second. How much you can delay the sound depends on how many different samples you've already got stored in your computer.

If this is the first time you have loaded the software, you will have automatically loaded a full set of sounds and you will have to make a bit of room for the echo. This is done by deleting one or more samples. (Don't worry – they're still on the tape or disk, so you

won't lose them forever.) Select 'Quit' then 'dElete'. Press 1, to delete one sample, and when asked "Which sample?", type in '6' and press ENTER. You have now made room for your echo.

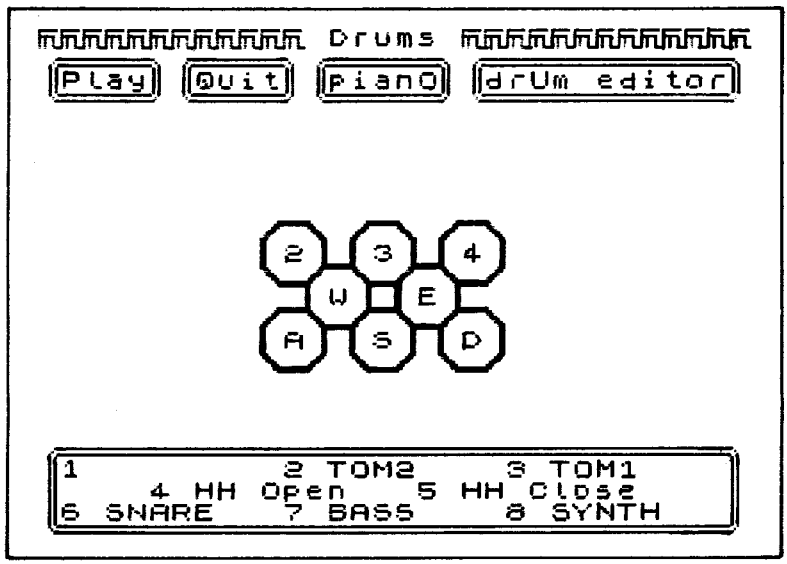


Figure 5, The Drum Machine

'Quit' back to the Main Menu and select 'ecHo'. Press'Play' and as you speak into the microphone, what comes out of the amplifier is exactly the same, but delayed! You will get even more extreme effects if the volume control of your amplifier is turned up, because the sound from the amplifier is then mixed in and delayed too. You can make some quite startling sounds using this technique, but don't turn the volume up too loud or you'll get feedback howls.

3.2 Some quick experiments for making your own sounds

You plugged the microphone in some time ago and have so far used it to delay your voice; let's use it creatively now.

We mentioned earlier that you can capture your own sounds and play them back in a sort of musical way through The Music Machine. Any sound that can be picked up strongly enough by the microphone (as long as that sound is not too long) can form the basis of your works of art.

We will give you some simple examples of how this is done now, but read Chapter 4 if you want some more detailed information.

Capturing a sample

From the Main Menu, select 'sampleR'. You will see the screen shown in Figure 6. It might look complicated, but it is really very simple. Notice how the coloured bar resembles the recording-level display on most modern hi-fi cassette decks. Well, that's exactly what it is - a level meter.

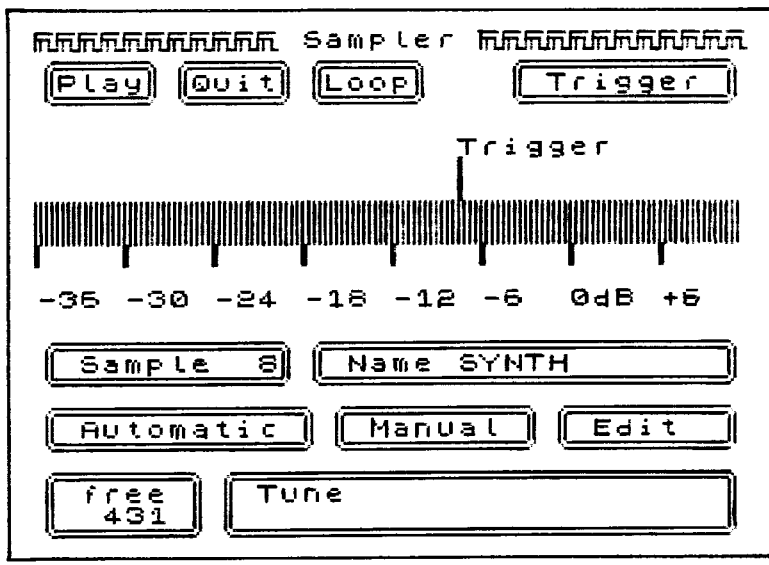


Figure 6, The Sampler

When you are using the microphone with The Machine to capture noises (just like a recording), the level meter of the sampler will respond to the loudness of the noise.

Try this. With the 'Manual' panel on the Sampler screen highlighted, say a few words into the microphone and see how the level meter moves from left to right. The louder you speak, the further right the meter moves.

If you have to shout in order to get the meter to read higher than the point marked 'Trigger', you should adjust the slider on top of The Music Machine's case (see Figure 1 to see where this slider is positioned). You have found the ideal position for the slider when, as you speak into the microphone, the screen level meter just goes into the red bar (marked 0dB and above).

OK, when you've set the level of the slider so that the meter just goes into the red bar when you speak, we can capture your voice. This can be done manually or automatically, but we'll do a quick example automatically now and explain more in Chapter 4.

So that you can experiment with several sounds, you should delete all those that are currently stored in your computer. So select 'Quit', then 'dElete', and then '2'. (Remember that you can always reload the original sounds from the tape or disk.) 'Quit' back to the Main Menu, and select 'sampleR' again.

Choose 'Automatic', and repeat "This is me" into the microphone.

As soon as the volume of your voice gets loud enough to cause the level meter to go over half-way into the yellow bar, press 'Trigger' and what you say will be captured automatically. What is happening is that the volume of your voice, when sufficiently loud, will trigger The Machine.

Until you get used to the level meter, you might have to try capturing your voice two or three times before you get it right. Don't worry though, you'll quickly get the hang of it.

So that you know which sample is your voice, select 'Name', and when you see the red flashing cursor, type in "My voice" and press ENTER.

Select 'Play' in order to hear what you sound like inside a computer!

Now that you have a new sample you can 'Quit' back to the main menu, and play the Amstrad 'piano' keyboard to produce your new sounds.

Note that you can alter the position of the Trigger point with respect to the bar meter by moving it left and right with the cursor keys. This lets you control the level at which the automatic trigger occurs.

What other handy short sounds can you capture conveniently? How about a snippet from the radio, or a raspberry?

OK, that's the easy stuff done with. Now we are really going to show you how to make the best use of The Music Machine. The next chapter explains how to capture and edit your own sounds, and then build them into your own songs, tunes and rhythms.

We will show you everything that The Machine and the software can do but, because it is so powerful, we might use words or phrases that are new to you. Wherever possible, we will describe what we mean so that you'll understand. Even if you've never composed any music or rhythms before, we'll be very surprised if you still haven't after reading the next chapter and experimenting with The Music Machine.

4. DETAILED DESCRIPTIONS OF WHAT DOES WHAT

In this chapter, we have assumed that you have already read chapters 2 and 3, and that you are familiar with the simpler things that The Music Machine and its software can do. If you haven't read these parts of the manual, we recommend that you do so now. Thank you.

4.1 Playing using the Amstrad keyboard

'pianO'

On selecting 'pianO' from the Main Menu, the system behaves as a simple monophonic (single voice) synthesiser. Pressing any of the appropriate keys from the keyboard screen will play the currently selected sample (indicated in the panel at the foot of the screen).

If you want to change the voice that is played by the 'piano', then simply select 'Current sample' and, when prompted by the red flashing cursor, enter the number of the voice you want to use and press ENTER. Press one of the "musical" keys to hear the sound. (Note that the music channel must have been selected from the Midi screen in order to listen to the audio output from The Machine: see the next paragraph.)
A directory of the available voices is shown on the Main Menu screen.

'Play'

Once you have composed a song, you can play it from more than one screen. You will probably play the song most often from either the Main Menu or the Tune Editor screens, it doesn't matter which. (Note that you can only play the displayed bars from the Tune editor.)

You must direct the music or drum output to the 'Ear' channel from the Midi screen if you want to listen to compositions through either the earphone socket or an amplifier connected to the phono output. This is simply done by selecting 'Midi', and keying either '4' or '7' according to whether you want to hear drums or music.

You can also play the drums or music through the Amstrad's programmable sound generator (psg) by selecting '8' or '9' respectively. Note that the sounds from the psg will sound nothing like those generated by the Music Machine.

4.1.1 The Bar Editor

In the context of The Music Machine, the difference between a bar and a tune is as follows:-

Bar: this is a sub-set of a tune. In other words, a tune comprises one or more bars. Obviously enough, you use the Bar Editor to compose a short piece of music.

Tune: this is a compilation of separate bars. Once you have composed a number of bars, you can string them together in any order you want, using the Tune Editor, to form your song.

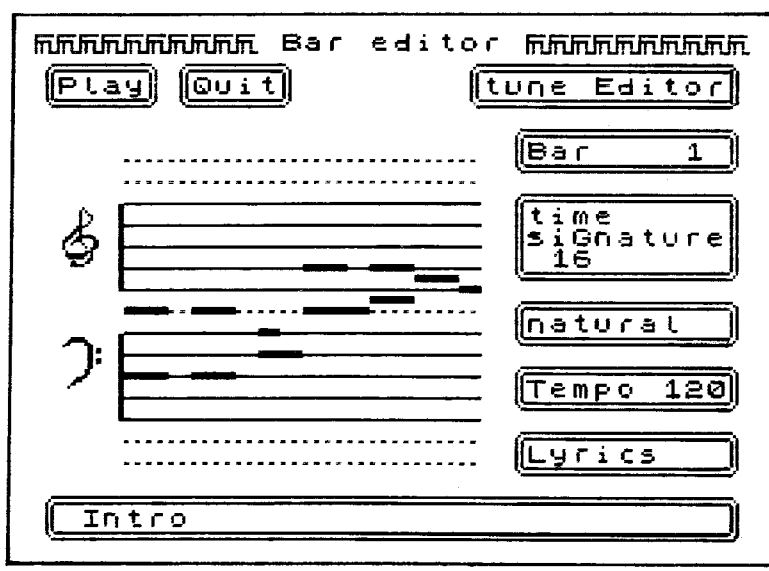


Figure 7, The Bar Editor

Select the 'Bar editor' from the Main Menu and you will see the screen shown in Figure 7. The major part of the screen is set aside for your music composition and consists of a conventional pair of staves for treble and bass clefs. (Each stave is set of horizontal parallel lines; the upper is called the treble clef, and the lower is called the bass clef.)

'Time Signature' and 'Tempo'

You may change the Time Signature and the Tempo of the music at any time, but note that any bar already displayed on the screen will be lost if you change the time signature after the music is composed. The time signature dictates the number of beats to the bar and may have a value of 16 or less whilst the Tempo indicates the rate at which the bar is played. The figure associated with the tempo is the number of beats per minute and may be any value in the range of 60 to 240.

If you want to plant sixteen notes on a stave, then you should select a time signature of sixteen; you will then have one complete bar for every sixteen notes. Or, if the signature is eight, you will be able to play eight notes to the bar.

Entering music

The way in which you enter music is illustrated in the following example. Because the software with which we supply you already has bars and tunes built into it, we shall edit the supplied tune which is called "Snap the Boogie".

Sharps and flats

'Quit', then select the 'Bar editor'. You will see the first bar of the song displayed. The black rectangles on the staves each represent a note. The notes may be natural (white notes on a piano), or sharps and flats (the black notes). If a note is sharp, then a '#' is displayed at the top or bottom of the stave nearest to that note. Notes entered as sharps are denoted by a '#' sign whereas flats are shown either as naturals or sharps. An example of this is B-flat which is actually displayed as A-sharp; see below.

Try this. Make the second note sharp by firstly keying 's' (to alter the box showing 'natural'), moving the cursor to the note, and pressing the space bar, backspacing and then pressing the space bar again. Change the third note to a flat by repeating the above process except for pressing 'f' for flat instead of 's' for sharp. You will notice that if you call for a sharp or a flat note that doesn't actually exist in musical terms (for example, there is no such thing as 'C flat'), the Music Machine software will select the appropriate natural note or semitone.

Whenever you press the space bar, you either plant a note at the cursor position or you remove one. Because the Amstrad Music Machine is a one-voice synthesiser, you can only play one note at a time. However, it can act as a two-voice device when driving MIDI. Thus, you can have two notes aligned vertically on the staves. If you attempt to enter a third note, the one nearest to it will disappear automatically. You can nevertheless, play two notes simultaneously on the internal Amstrad sound chip.

Changing bars

Experiment with the bar editor by moving notes around the staves; select 'Play' from time-to-time to see what your composition sounds like. When you have completely ruined the first bar, select 'Bar' and, when prompted, key in the number of another bar and press ENTER.

Changing the lyrics

Select 'Lyrics' and when prompted by the red flashing cursor, enter a name for the bar. When you come to compile your song, the bar number and the first part of the lyric name will be displayed in a screen panel. If you use lyrics that remind you of the music in that particular bar, you will find it easier to assemble your song; this will be illustrated with an example in a moment.

4.1.2 The Tune Editor

Select 'tuNe editor' from the Main Menu and you will see the screen

shown in Figure 8. This editor is not nearly as complicated as the Bar Editor. All you need do with this screen is construct a list of numbers.

Each number and name represents a bar that you have already composed. To make a song, you simply string together bars in the order that you want.

As an example, we can compose a variation of the song "Snap the Boogie" that is supplied with the software, just by re-ordering the bars and adding the new bar that we ruined - sorry, composed - in section 4.1.1.

Drum rhythm bars are assembled in the left-hand panel, and music bars in the right-hand one. Move the cursor right, to the music tune editor, and then scroll through the music using the up and down cursor keys. Overtype at the cursor position to replace a few bar numbers and watch how a handful of letters of the lyric are displayed to remind you of what the bars are. If you want to insert new bar numbers, just press ENTER (bar number 1 will then be inserted by default) and add the number you want.

To change the voice, select 'Current sample' and enter the new voice number. To edit the tune name, select 'Tune' and enter the new name.

If you select 'Play' from the Drum editor screen, you can only play the displayed bar and not the whole rhythm sequence (composed from lots of bars); the whole is playable from the Tune editor. Whether music or drums play when you select 'P' depends on which side of the screen the cursor is displayed. Move between music and drums using the cursor left and right keys.

The number in the 'free' panel indicates the amount of space you have available for composing your tunes.

If you want to interrupt a song whilst it is playing, press ESCAPE.

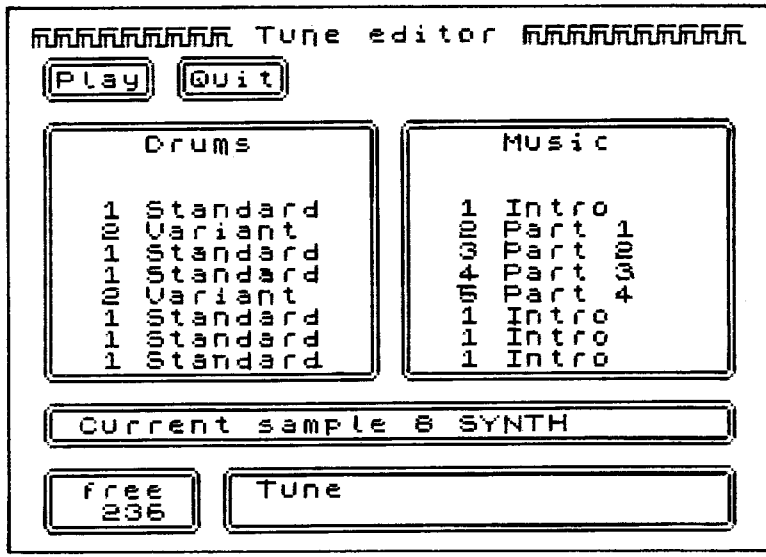


Figure 8, The Tune Editor

4.2 The Drum Machine

On selecting 'Drums' from the Main Menu, you will see the screen shown in Figure 5. Pressing the appropriate keys on the Amstrad keyboard will result in the sounds listed in the bottom panel of the screen being played.

The relationship between the keys and the number of the sound is a function of their physical positions:

Amstrad Key	Sound Number
2	1
4	3
E	5
S	7

Amstrad Key	Sound Number
3	2
W	4
A	6
D	8

Note that from the Drums screen, you can only play one drum sound at a time (but you still have eight sounds to choose from). However, it is possible to play any three sounds from these eight at the same time when using the drum editor to build a rhythm.

4.2.1 The Drum Rhythm Editor

When you select 'drUm editor' from the Main Menu, you are confronted with the screen shown in Figure 9. The column of numbers from 1 to 8 lists the memory-resident sound samples. If you load the software from the original cassette or disk, you will see listed the drum sounds supplied.

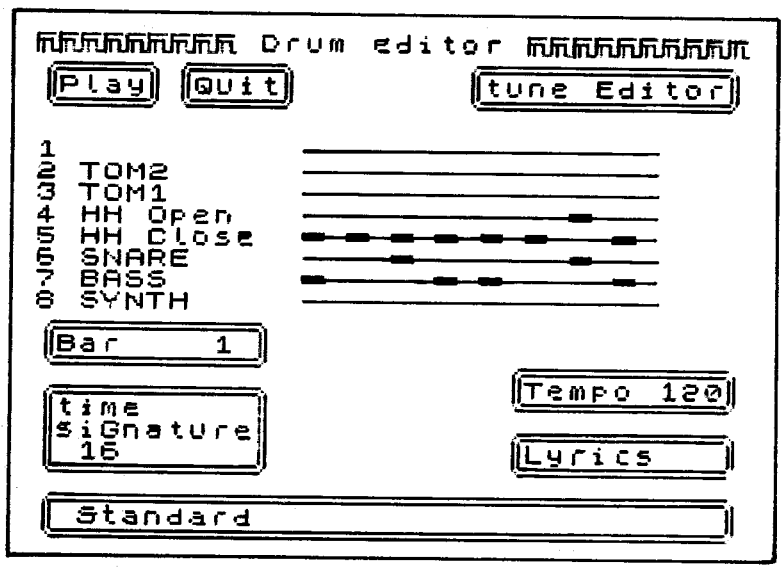


Figure 9, The Drum Editor

Writing your own rhythms is straightforward; wherever there is a beat planted on a horizontal line, then the sample associated with that line will sound when the rhythm is played. There are several similarities with the tune editor described in section 4.1.2 of this manual, and these are as follows:

The tempo may be changed to any value between 60 and 240 beats per minute. The lyrics editor enables you to describe each bar with a meaningful name. The time signature may have a value of 16 or less and denotes the number of beats per bar. The bar number panel is used both to create new bars and edit existing ones.

As an example of how to create a drum rhythm, first select a time signature of 16 and a slow tempo of 120 beats per minute. Insert a bass drum line of one drum beat every fourth space, starting with the first space, along the line. Add a sound like a hi-hat every second and third space. Add a tom-tom every fourth space starting with the third. Now add sounds that take your fancy elsewhere in the bar (but don't forget that you can only play three samples simultaneously). Now you can change the tempo to suit your mood.

Once you have composed several bars of different rhythms, you can use the tune editor to string them together and play them. If you have forgotten how to use the tune editor, read section 4.1.2 above.

4.3 Recording real-life sounds

Before you try the examples in this section of the manual, delete all of the resident samples. ('Quit', 'dElete', select '2'.)

The microphone supplied with the Music Machine can be used for capturing sounds from virtually any source. Both quiet and loud sounds can be captured; you will need to adjust the level control and maybe the distance of the microphone from the source to get the effect that you want.

Select 'sampleR' to bring up the screen shown in Figure 6. The level meter on this screen behaves in the same way as do bar meters on

modern cassette decks. The louder the sound source, the higher is the reading on the level meter.

You will find by experiment which combination of slider position (on the top of the Music Machine's case) and volume level of the source give the best results. Start by setting the slider to a position that corresponds to a screen reading averaging -6 dB; speaking into the microphone is probably the easiest way to experiment.

When you have found a suitable level, select 'Automatic', get ready to speak, press 'Trigger' and say "Testing testing". Press 'Play' to see what it sounds like.

(If the level is too low, you will not capture a sample because you will not have set off the automatic trigger. When a sample is being taken, the "Trigger" panel is high-lighted. The bar meter must reach approximately -6 dB before the Music Machine is triggered although this can be adjusted using the left/right cursor keys. On the other hand if, when you play the sample, it is very distorted then the slider control is set too high.)

The Manual control option on this screen enables you to capture a sample right from the moment that you press 'Trigger' and is useful if you want to record at a particular instant in time.

The 'Loop' option on this screen enables you to play a particular sample continuously. Once Loop is selected, anything you play from the 'piano' or MIDI screen will continue to sound until a key is released or note-off data is sent.

4.3.1 Editing captured sounds

When you capture a sound, that sample will fill all of the allocated free memory space. Assuming that you currently have no samples resident and, say, you want to capture a sound lasting 1000 milliseconds, then most of the free space will be taken. This is why the sample editor is provided.

Capture a sound (some speech, for example). Select 'Edit' and you will see the screen shown in Figure 4. The peaks in the displayed signal represent the captured sound. The horizontal sections of the display are most probably dead space. Edit out this dead space by moving the front cursor (F) with the cursor keys to the start of the rise. Play the sound to see what effect this has on the sample. Select 'B' and move the back cursor to the end of the fall, and you will now have sandwiched the useful part of the signal. Play it to ensure that you have eliminated the dead space.

Some signals, if truncated at a high signal level will sound "spitty" when played. This may be overcome by starting and stopping the sample at points where the spectrum is at or near the base-line. Because rapid variations in the signal level are difficult to spot when the spectrum is displayed normally, you can 'Zoom' into the part of the graph nearest the selected cursor (that is, either front or back) and examine it in close-up. You will then find it very much easier to truncate the signal at a minumum and thus avoid "spit".

You may play your sample backwards by invoking 'Reverse'.

The positions of the front and back cursors are expressed in terms of elapsed time in units of milliseconds (thousandths of a second). The "free" figure is also in milliseconds and gives you a measure of how much space you have left for other samples. You have in total about one and a quarter seconds at your disposal. This might not seem like very long, but bear in mind that realistic drum sounds can be made with samples less than one-tenth of a second long.

4.4 Playing using an external keyboard

To connect a MIDI (Musical Instrument Digital Interface) keyboard to the Music Machine, you should plug appropriate DIN cables into the MIDI-IN and MIDI-OUT ports of both devices. As you would expect, IN on one device should be connected to OUT on the other, and vice versa.

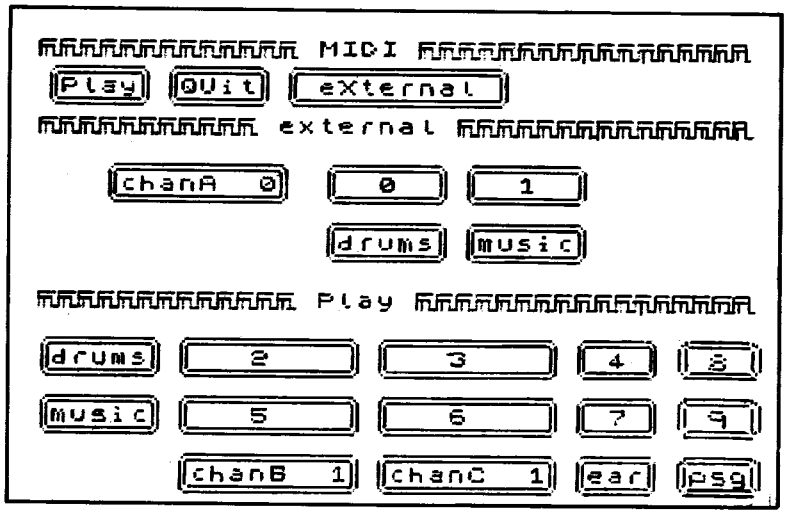


Figure 10, The Midi Screen

You are now free to do several things.

(a) You may play any captured sample held in the Amstrad's memory from the MIDI keyboard over its full musical range.

(b) You may send composed tunes to the MIDI synthesiser and play either the captured samples or any of the voices that your MIDI device might already hold, or both simultaneously.

(c) Using the microphone, you may capture any of the MIDI keyboard's voices and edit them using the sample editor.

(d) You may switch between voices on your MIDI keyboard to simulate different instruments.

(e) Using a MIDI synthesiser, you may play two Music Machine notes simultaneously (whereas this can't be done directly from the computer's keyboard).

Figure 10 shows the MIDI screen. The important thing to note about this screen is that it is actually two screens in one; the top half is for external playing. In particular, the bottom half is relevant to what happens when data is sent to a particular output (whether this be drums or music sent to the ear/phono or MIDI sockets, or the Amstrad's internal psg).

Note that you can define which of the 16 MIDI channels both receive and transmit data. You have complete freedom over where you send the Music Machine's drum and musical signals. Channels A, B and C correspond to external drums or music, internal drums, and internal music respectively; each may be assigned to any MIDI channel.

Note that the software will not allow you to map both drums and music onto the earphone (or phono) outputs of The Music Machine. You can only play drums OR music through these outputs, and not both simultaneously. The same limitation applies to the Amstrad's internal psg. Please see section 4.4.2.

To allow a MIDI synthesiser to play a Music Machine voice, select the MIDI channel you want to use (channel zero is the 'omni' mode that can receive from all channels), and select 'eXternal'. If music is mapped onto the MIDI channel in the lower half of the MIDI screen (key 5 or 6), your synthesiser will play a resident sample. If drums are mapped onto the MIDI channel (key 2 or 3), the complete sample set will map onto consecutive sets of keys.

You might wish to play some pretty advanced musical compositions (using the MIDI keyboard), store them, edit them, and play them back later. At the moment, the software we supply takes up a great deal of the available RAM and we just have not had the space to provide you with these latter facilities. Please write and let us know what you want to do with your Music Machine and we will try to take account of your needs with future developments.

4.4.1 MIDI in, out and through

The MIDI-IN and MIDI-OUT sockets on The Music Machine conform to the MIDI standard. The MIDI-THROUGH socket is used for daisy-chaining devices that conform to the MIDI standard. The instructions supplied with whatever it is that you wish to connect should give you more information about assigning masters and slaves.

As The Music Machine conforms to the MIDI standard, you can of course connect up to 16 Amstrads together and orchestrate them!

If you are fortunate enough to own a MIDI sequencer, you can use this as the master device for controlling, say, an external keyboard, an external drum synth, AND your Music Machine. The world of MIDI is large and fairly complicated; without knowing what devices you are going to plug together, it is very difficult for us to provide you with detailed instructions. Suffice to say, whatever you are plugging in should come with its own instruction manual to help you.

4.4.2 Combining tunes and drums

You have just read that it is not possible to direct drum and music outputs to the headphone or phono sockets simultaneously. However, you can use your MIDI keyboard to play the music whilst The Music Machine plays the drum rhythm in synchronisation.

Channel selection is straightforward from the MIDI screen menu, and you can assign any of the sixteen channels to any stream you want.

4.5 The effects box; echo and reverberation

Echo and reverberation effects are generated via a simple variable delay line. You will hear markedly different effects by listening either through your headphones or an amplifier.

The length of the delay that you can use is dependent on the amount of free RAM; if you have stored a number of samples, there will be less

space to alot to the delay effect. To maximise the delay, you should delete all resident samples. The delay time is displayed in a screen panel in millliseconds.

Using headphones, you can faze yourself by trying to speak coherently into the microphone. Alternatively, with an amplifier and speakers connected, you will find that you can generate some pretty startlihg effects as the delayed signal is regenerated via the speakers and microphone. Be warned that at high sound levels, you can generate feedback howls.

By experimenting with the length of the delay, the microphone level slider, and the amplifier output volume, you should be able to produce a wide range of strange noises.

4.6 Recording and replaying your compositions

Loading and saving is an extremely simple affair. The options available to you on selecting 'Load/save' are self-explanatory.

You can save the data parts of the program either with the program or separately. The advantages of this are that you can load and save individual samples, sub-libraries of samples, individual tunes and sub-libraries of tunes to suit your particular needs. If you would rather, you can save all your samples and tunes together with the program so that when you next load the software, it is ready to run.

The program is smart enough to recognise whether what it is loading is samples or tunes, so you need not necessarily specify which. You may use the usual Amstrad "CHAIN" command if you cannot remember the name of what you want to load (tape only), or you can look for specific named files. If you are using disk, you can get a directory from the filing menu.

4.6.1. Cassette and Disk storage

If you have software on cassette you can transfer it to disk using the

Load/save option from within the program. To do this simply select Floppy from the menu and then option 4, enter a name as requested and then hit RETURN.

If you have not got a disk fitted you may choose to reduce the cassette loading time by saving the program without the loading screen. To do this follow the procedure above but do not select the Floppy option.

5. TECHNICAL SPECIFICATION OF THE MUSIC MACHINE

If you have some technical knowledge and machine code programming experience, you may well be interested in the contents of this chapter. (On the other hand, you might not want to know anything at all about the technicalities of The Music Machine - in which case you won't miss much by not reading this.)

5.1 Technical Spec.

The Music Machine incorporates two Ferranti devices for digital-to-analogue (DAC) and analogue-to-digital (A to D) conversion. The part numbers are ZN429E8 and ZN449 respectively. The circuit also includes a Motorola 6850 ACIA (Asynchronous Communications Interface Adapter) for handling the MIDI channel, two anti-alias filters (one for input and one for output), a discrete microphone amplifier and a headphone amplifier. The clock signal for the ACIA and the ZN449 is provided by a ceramic oscillator.

The incoming signal from the microphone amplifier is sampled to an 8-bit resolution at a rate of 19.444 thousand samples per second. This yields an analogue bandwidth of approximately 9.5 KHz which is in fact the cutoff frequency of the filters.

All of the devices on The Music Machine data bus are accessible to the Amstrad within its IO space. ACIA transactions must use 16-bit IO instructions; the converters are accessible via 8-bit IO instructions.

IO Map

ADC START	OF8F8 hex	Reading (or writing) to this port will start analogue to-digital conversion.
ADC READ	OF8F4 hex (read only)	The contents of the A-to-D can be read via this port. Note that the A-to-D must have been 'started' at least 20 uS before this port is read.

DAC WRITE	OF8FO hex (write only)	Date can be written to the DAC via this port.
INTER'PT SEL	OF8E8 hex (write only)	Writing 01 to this port disables internal Amstrad interrupts and replaces the IRQ signal from the ACIA. Writing 0 restores normality.
ACIA status	OF8EE hex (read only)	
ACIA data read	OF8EF hex (read only)	} See Motorola Data Sheet
ACIA control	OF8EC hex (write only)	
ACIA data write	OF8ED hex (write only)	

Sampled-data capacity	1223ms
Clock frequency	500 kHz
A-to-D conversion time	20 uS
Sampling frequency	19,444 samples per second
Sampling bandwidth	20 Hz to 9.5 KHz
Input sensitivity	2mV RMS into 50 kOhms
Headphone output	15mW RMS into 15 Ohms
Amplifier (phono) output	450 mV RMS
Signal-to-noise ratio	42 dB

MIDI

The only MIDI facilities provided as standard with The Music Machine are the ability to control internal or external note-on or note-off events. In most cases the action of turning a note on or off requires the transmission of three bytes.

Note-on event:

1001nnnn	NOTE-ON control byte. nnnn is a four-bit number corresponding to the MIDI channel number. 0000 is Channel 1, 0001 is Channel 2, and 1111 is Channel 16, for example.
0ppppppp	Pitch value. 0010 0000 is middle C.
0vvvvvvv	Velocity value. The Music Machine can only recognise velocity 0 which is, in effect, NOTE OFF or another value for note on. There are no facilities for volume control and so, quite reasonably, it is ignored.

Note-off event:

1000nnnn	NOTE-OFF control byte
0ppppppp	Pitch value of the note to be turned off.
0vvvvvvv	After-touch velocity, ignored.

Drum Pitch

In common with other drum machines, each drum has a note-number; unfortunately, different machines use different numbers. The Music Machine uses the following note numbers:

Middle C = 1, C# = 2, D = 3, and so on.

5.2 Music capacity

RAM is consumed at the rate of one byte per sample. With a sample rate of 19.444 kHz and about 23K of data space, approximately 1.22 seconds of continuous digitised data can be stored. The amount of free RAM is indicated on most screens, and is given in units of milliseconds.

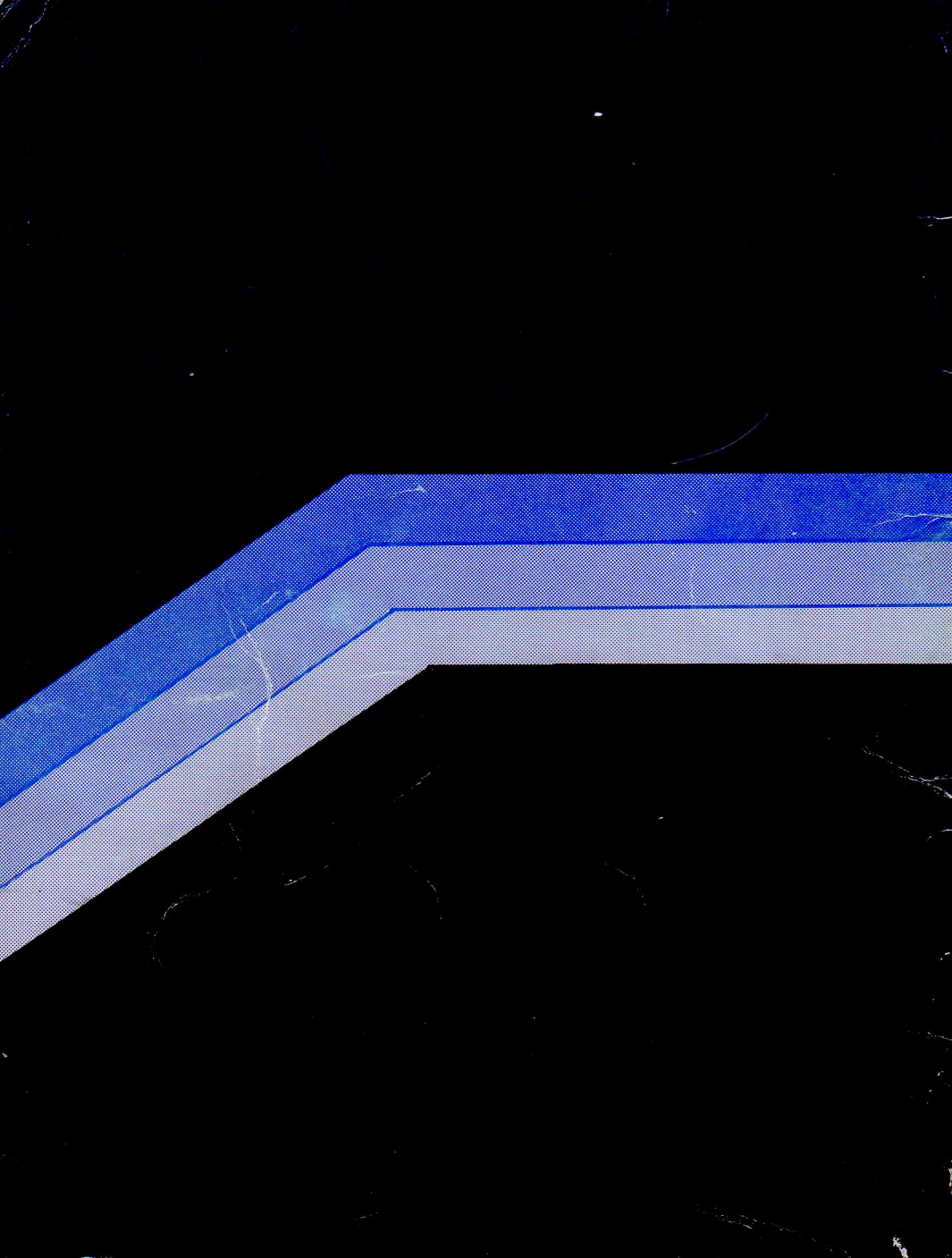
Up to eight digitised samples can be stored in RAM simultaneously. At full capacity, the average duration of each sample is about 0.15 seconds. In practice, the digitised drum sounds consume around one tenth of a second each, leaving half a second or so for user-sounds. You do of course have the option of deleting the resident samples in order to make use of the full data space. The total duration available of around 1.2 seconds is, we believe you will find, a surprisingly long time for most musical sounds.

A song or rhythm can comprise a sequence of up to 255 different bars. Because most music repeats a range of bars, the final song or drum sequence can last very many minutes.

5.3 Additional notes

You must use headphones whose lead is terminated with a 3.5 mm *stereo* jack plug as a mono plug may short the output and you will hear nothing. Aim to use headphones with an impedance between 8 and 64 Ohms.

By all means experiment with microphones other than the one we supply; in general, the better the quality of the microphone, the better the results.



An Amstrad like you've never heard it before.

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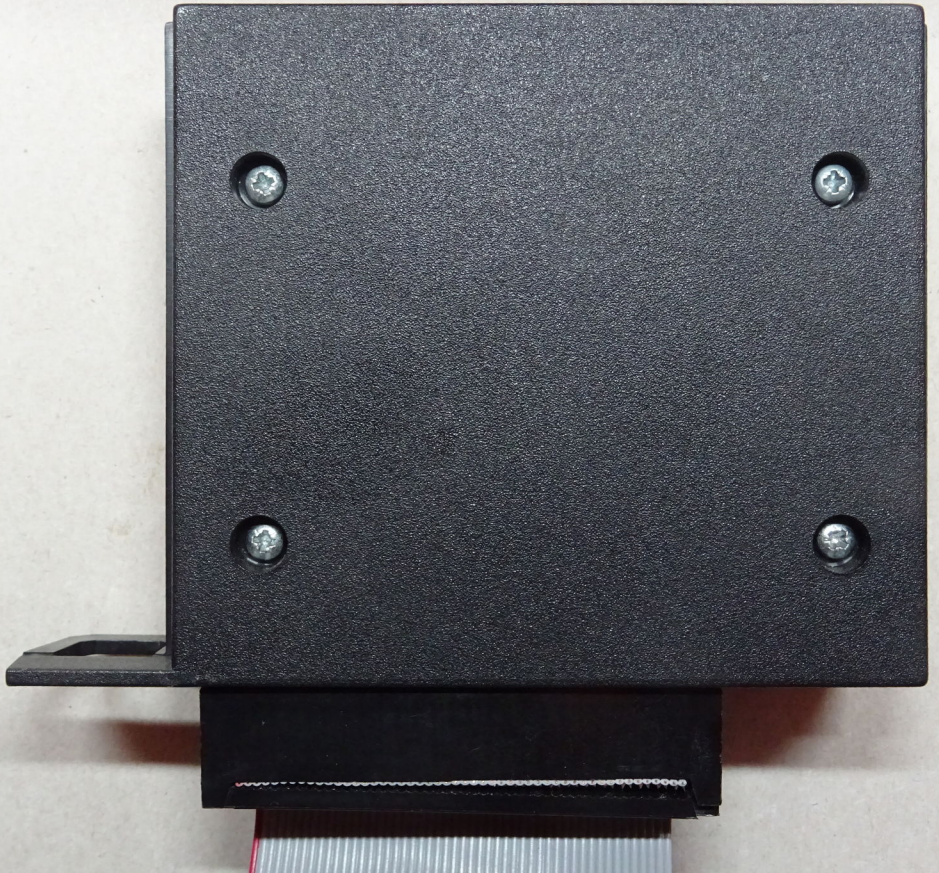

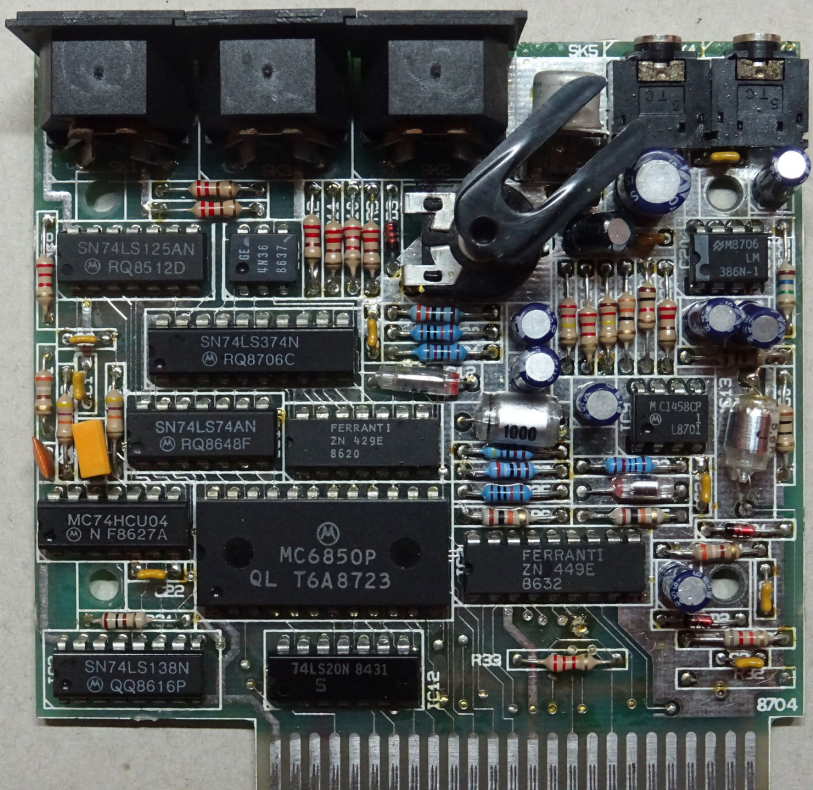
SK5
SN74LS125AN
RQ8512D
SN74LS374N
RQ8706C
SN74LS74AN
RQ8648F
FERRANTI
ZN 429E
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MC74HCU04
N F8627A
MC6850P
QL T6A8723
FERRANTI
ZN 449E
8632
SN74LS138N
QQ8616P
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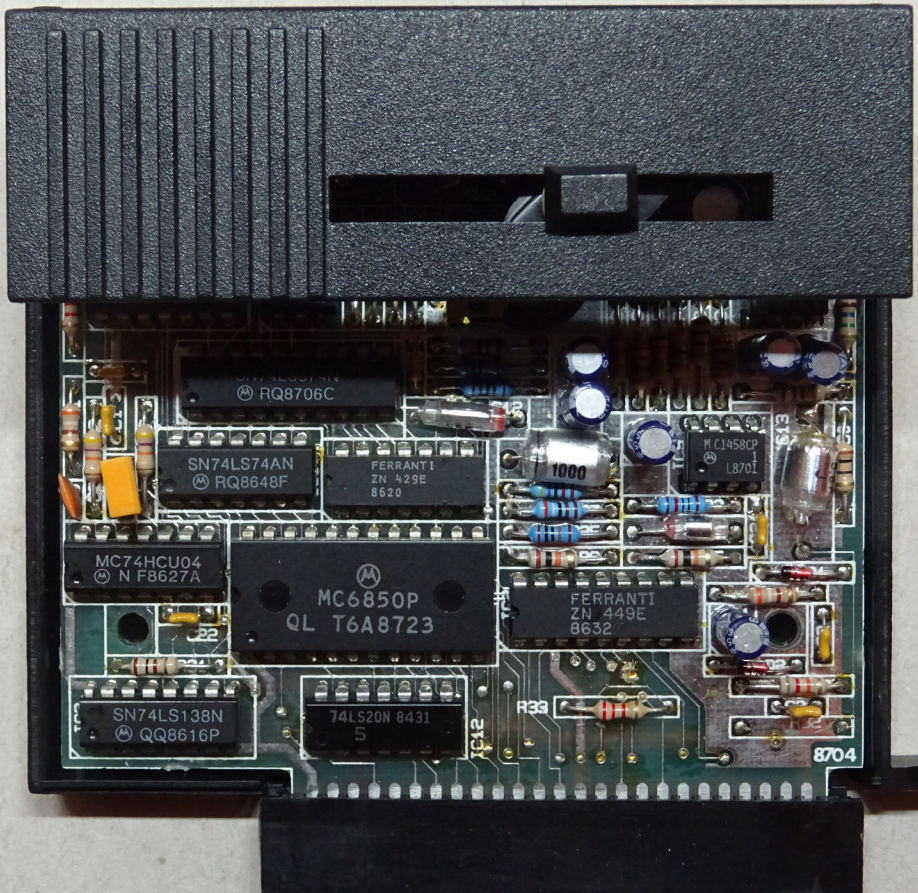
R39
M8706
LM
386N-1
M C1458CP
1
L870I
8704


RQ8706C
SN74LS74AN
RQ8648F
FERRANTI
ZN 429E
8620
1000
M C1458CP
1
L8701
MC74HCU04
N F8627A
MC6850P
QL T6A8723
FERRANTI
ZN 449E
8632
SN74LS138N
QQ8616P
74LS20N 8431
5
R33
8704


SANYO
ON
OFF


MUSIC
MACHINE
MUSIC
MACHINE
ALTAI

AMSTRAD
6128

MUSIC MACHINE
The complete home computer music system

MUSIC MACHINE
The complete home computer music system

MUSIC MACHINE
THE COMPLETE HOME COMPUTER MUSIC SYSTEM

AMSTRAD

USER GUIDE

RAM
MUSIC MACHINE
SOFTWARE
FOR THE AMSTRAD 6128

MUSIC MACHINE

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6128

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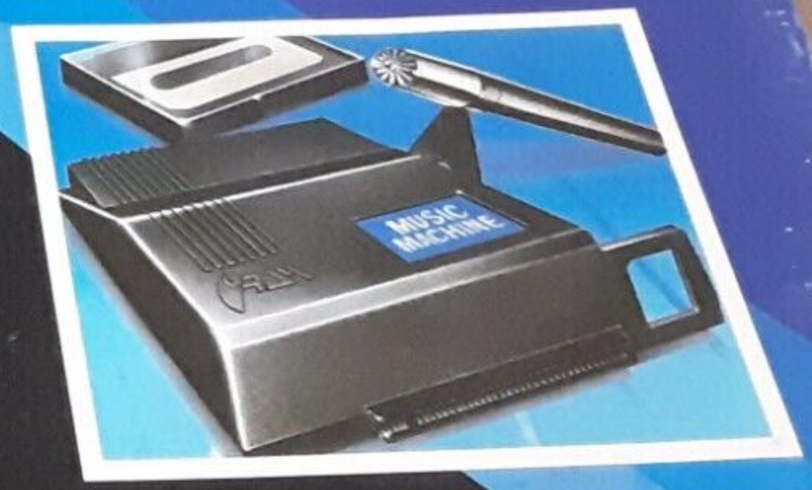
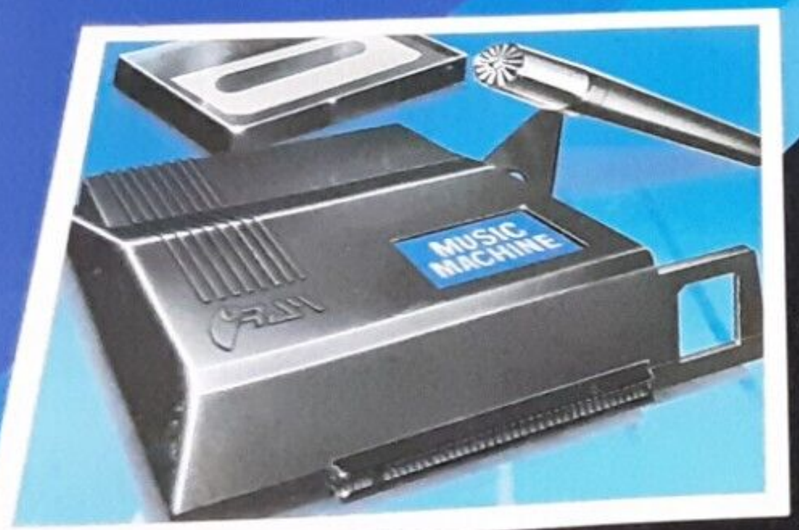
MUSIC MACHINE®

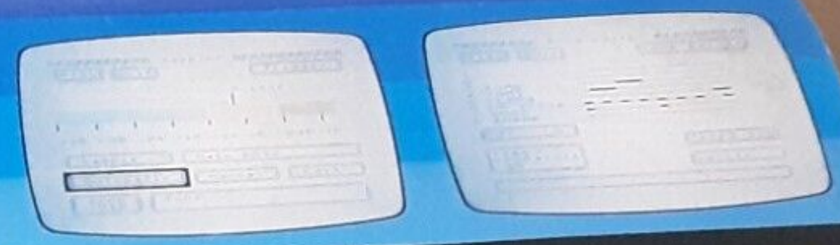
The complete home computer music system



MUSIC MACHINE
The complete home computer music system
MUSIC MACHINE

FULL 1 YEAR GUARANTEE





- Easy to use with fast menu-driven screens
- High quality drum machine with real pre-recorded drum sounds
- Any external sound can be recorded, altered and played through the keyboard
- Write your own music quickly and easily using the on-screen facilities
- MIDI interface to other musical instruments
- Pack includes easy-to-understand user guide, microphone and demonstration tape
- Plug in your headphones or listen through your hi-fi

*Music Machine is a trademark of Ram Electronics (Fleet) Ltd. Designed in the UK by Flare Technology Ltd. and manufactured in the UK by Ram Electronics (Fleet) Ltd. We reserve the right to amend specifications without notice.

Ram Electronics (Fleet) Ltd., Unit 16, Redfields Ind. Park, Redfield Lane, Church Crookham, Aldershot, Hants. GU13 0RE.

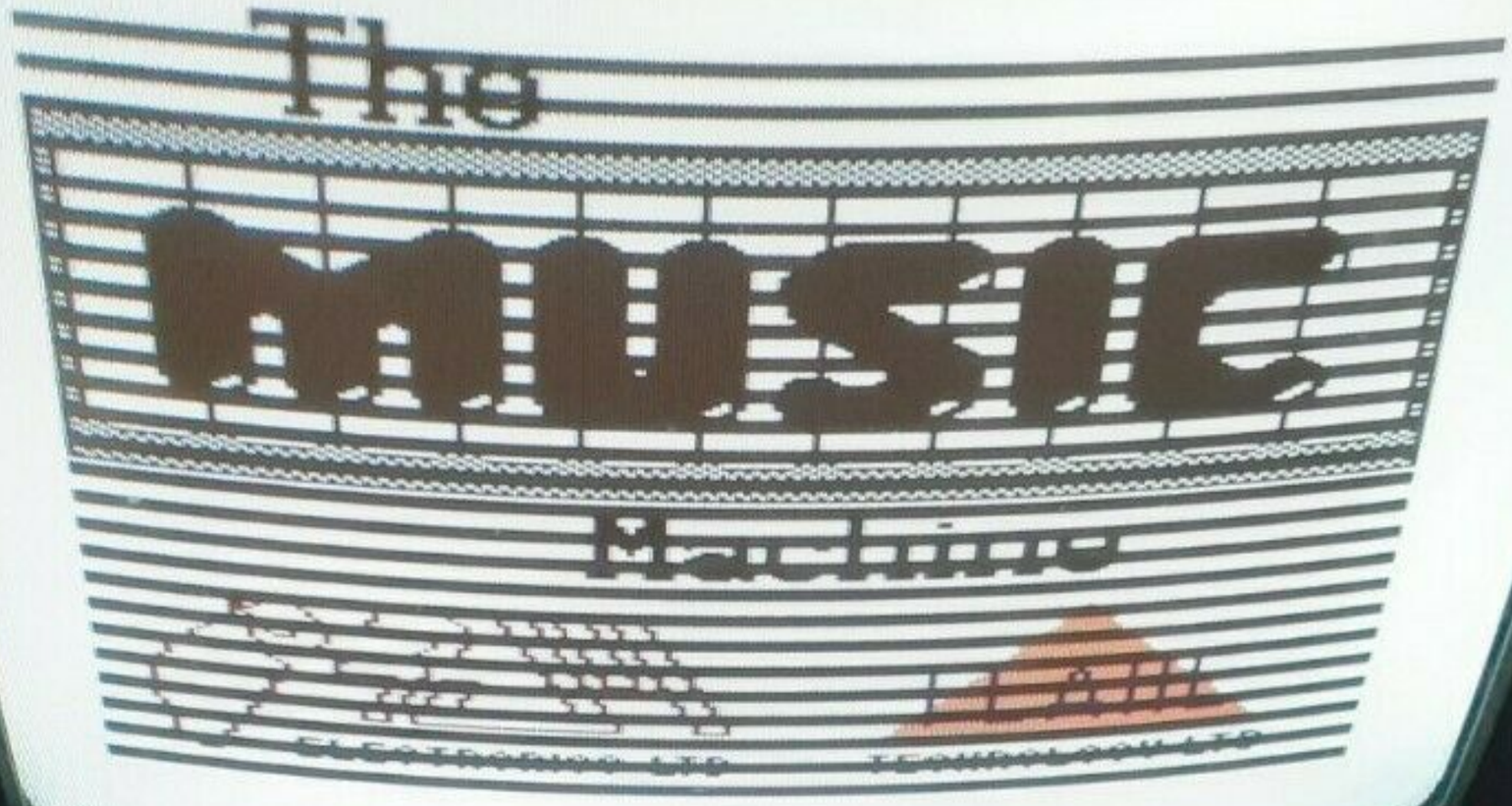
MUSIC MACHINE
The complete home computer music system

MUSIC
MACHINE

AMSTRAD VERSION

MUSIC MACHINE

The complete home computer music system



AMSTRAD VERSION

MUSIC MACHINE

The complete home computer music system

MUSIC MACHINE

The complete home computer music system

Main Menu

Play | Midi | ecHo | Load/save

tuNe editor | Bar editor | Druns

sAmple editor | pianO | exIt

dElete | drUm editor | sampleR

Samples

1	COWBELL	5	HH close
2	TOM2	6	SNARE
3	TOM1	7	BASS
4	HH open	8	SYNTH

free 2

Tune
Snap the boogie

Main Menu

Play | Midi | ecHo | Load/save

tuNe editor | Bar editor | Drums

sAmple editor | pianO | exIt

dElete | drUm editor | sampleR

samples

1	COWBELL	5	HH close
2	TOM2	6	SNARE
3	TOM1	7	BASS
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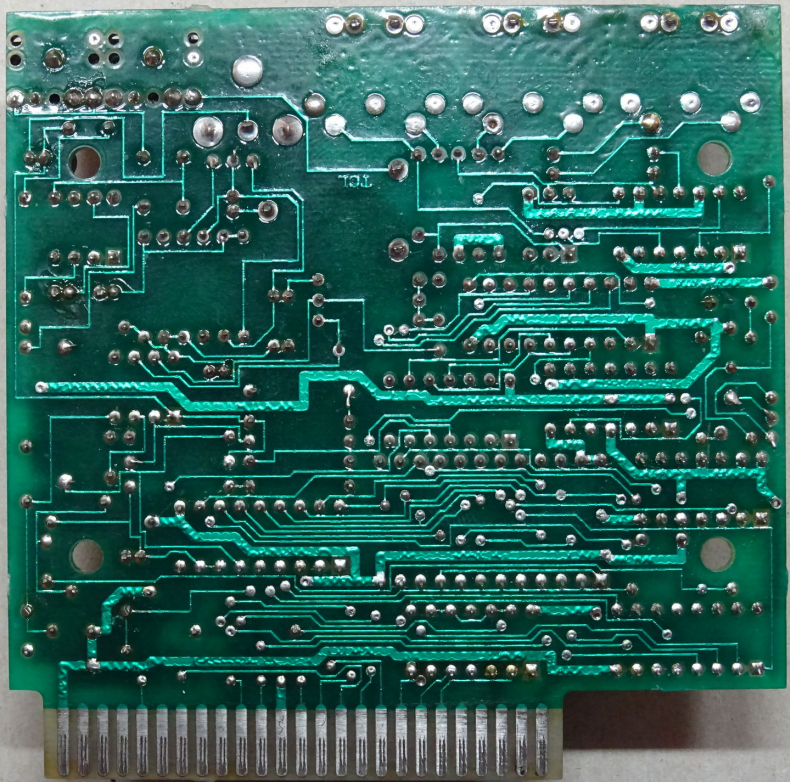
free 2

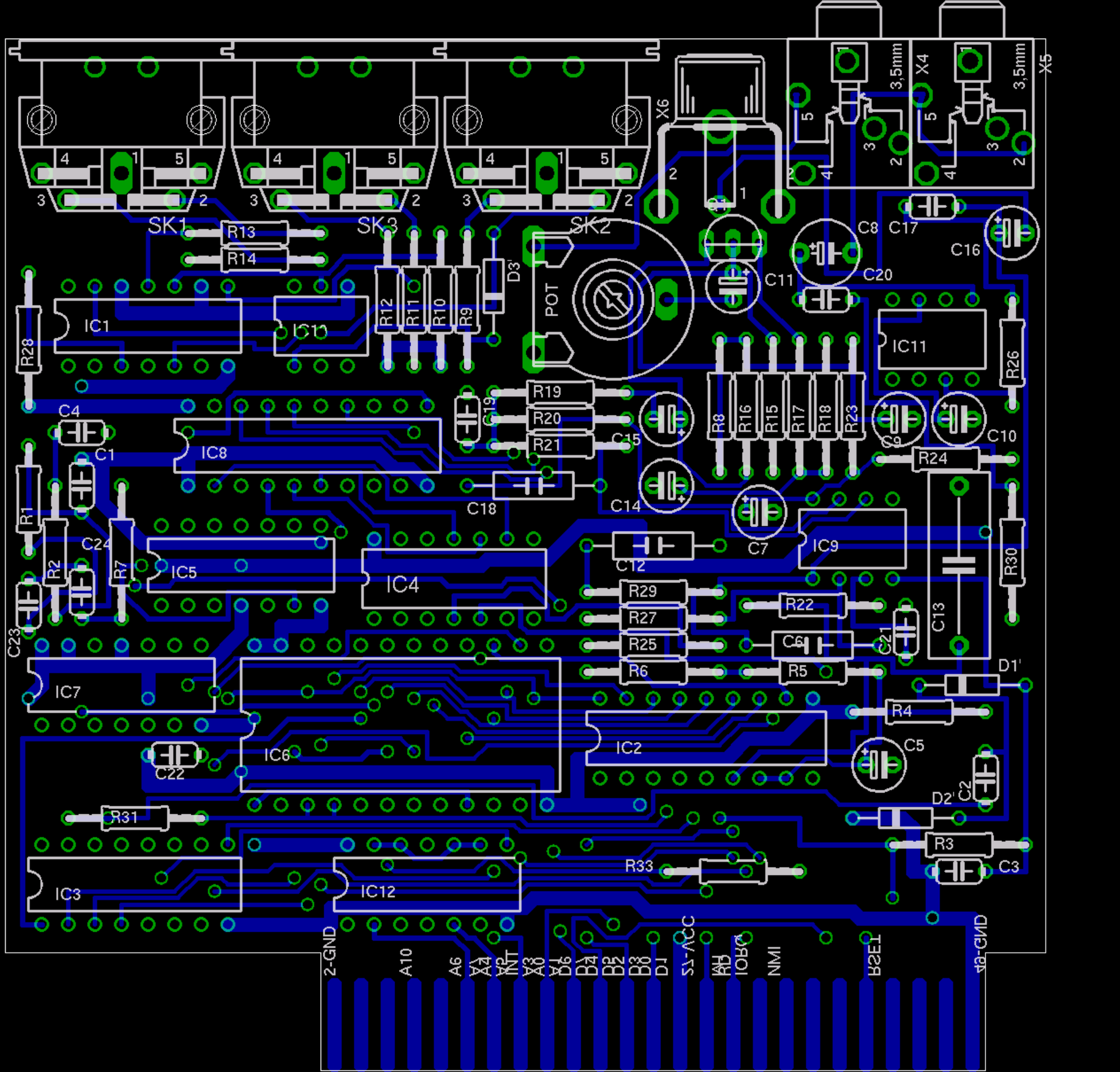
Tune
Snap the boogie

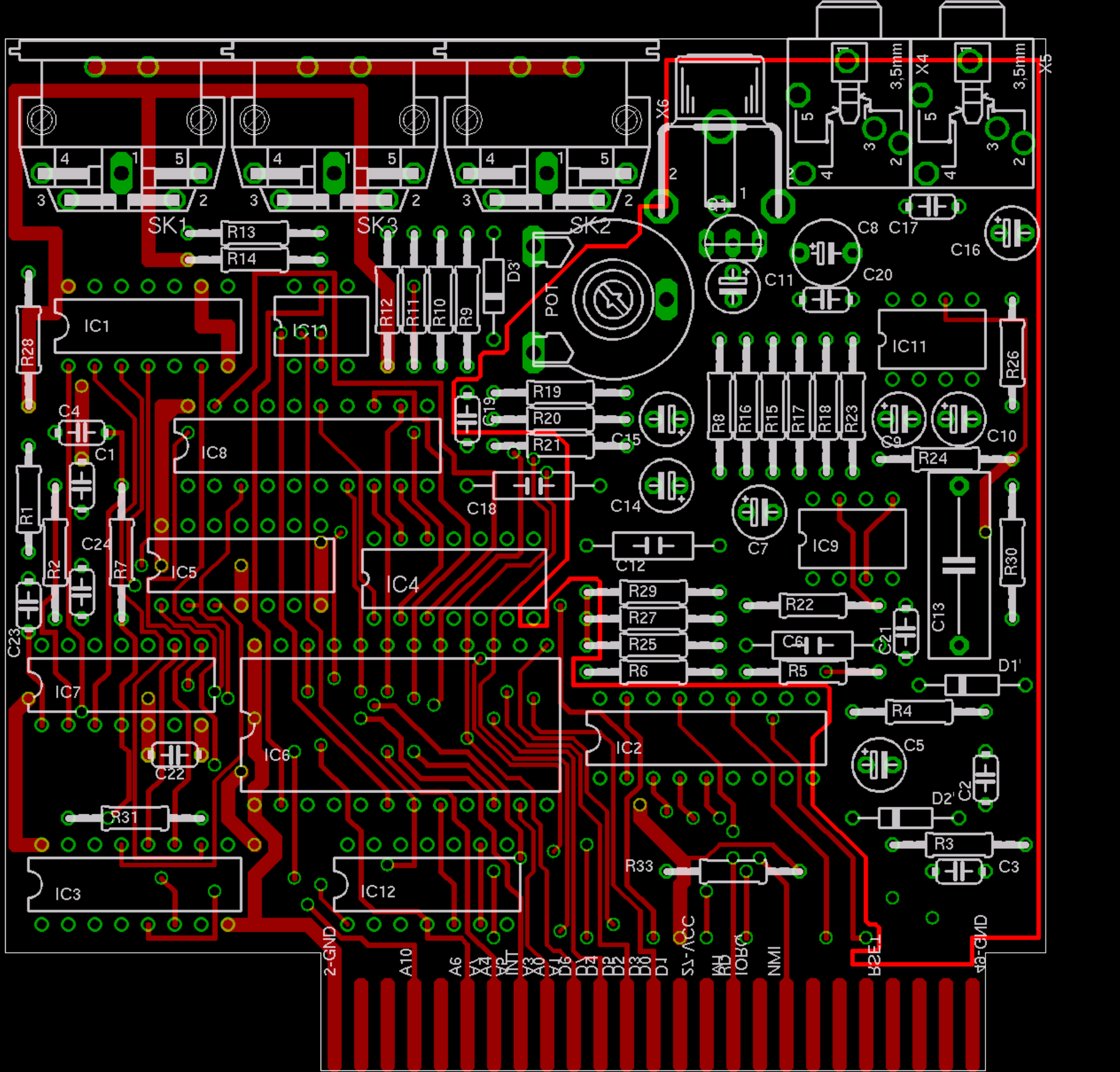
AMSTRAD VERSION

MUSIC MACHINE

The complete home computer music system




SK1
SK3
SK2
X6
X4
X5
3,5mm
3,5mm
POT
R13
R14
R12
R11
R10
R9
D3'
R28
IC1
IC10
C19
R19
R20
R21
C15
C18
C14
R8
R16
R15
R17
R18
R23
C9
C10
C8
C17
C16
C11
C20
IC11
R26
R24
C4
C1
IC8
R1
R2
R7
C24
IC5
IC4
C12
C7
IC9
R30
C23
R29
R27
R25
R6
R22
C6
C21
C13
D1'
R4
C5
IC7
IC6
IC2
C22
C2
D2'
R31
R3
C3
R33
IC3
IC12
2-GND
A10
A6
A4
A2
A0
D6
D4
D2
D0
+5V
IORQ
NMI
RESET
+9-GND


SK1
SK3
SK2
X6
X4
X5
3,5mm
POT
IC1
IC10
IC11
IC8
IC5
IC4
IC7
IC6
IC2
IC3
IC12
IC9
R13
R14
R12
R11
R10
R9
D3'
R19
R20
R21
R8
R16
R15
R17
R18
R23
R24
R26
R28
R1
R2
R7
R29
R27
R25
R6
R22
R5
R4
R31
R33
R3
D1'
D2'
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
2-GND
A10
A6
A4
A2
A0
D7
D5
D4
D3
D2
D1
D0
NMI
RESET

AMSTRAD CPC
MUSIC MACHINE

SIDE A

ISSUE 1

464: Hold down CTRL key and the small enter key.
664/6128: Type **I** (shifted@) tape (ENTER) then type RUN"


AUDIO DEMO
"SNAP THE BOOGIE"
SIDE B
© FLARE
100
50
0
© RAM
ELECTRONICS

IC12A
74LS20B
IC12B
74LS20B
M1
A7
A6
A5
IC3
74LS138B
INT
A3
A4
A10
IORQ
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
RD
IC1A
74LS125B
R28
2K2
VCC
IC5A
74LS74B
PRE
D
CLK
CLR
Q
Q\
D0
RSET
IC1B
74LS125B
NMI
R33
2K2
IC7D
74HCT04B
R9
220
MAB5WH
SK2
D3'
IC10
4N36
NC
PE
IC6
MC6850P
A5
A6
A0
A1
GND
IC2
ZN449
D0
D1
D2
D3
D4
D5
D6
D7
R4
390
R5
10K
R6
10k
C5
1uF/10v
C13
5,6n
27-VCC
2-GND
49-GND
C22
470n
R14
220
SK1
R13
220
IC1D
74LS125B
IC7C
IC7F
IC7E
74HCT04B
R10
220
R12
220
SK3
R11
220
IC1C
74LS125B
IC8
74LS374B
1D
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
OC
CLK
R25
100k 1%
IC4
ZN429
C12
1000
C17
100n
R26
1M6
IC11
LM386
C10
10uF/10v
C20
100n
R30
1
C8
220uF / 16v
X5
PG203J
R29
47k 1%
C16
1uF/10v
X6
TOBU3
R22
10k 1%
R20
2K2
R21
2K2
C18
1000
C6
100
R27
3k9 1%
R3
82k
IC9
mc1458
C3
100n
D1'
C21
100n
R24
100
C7
47uF / 10v
R23
220
C9
10uF/10v
R8
22K
R16
2K2
Q1
BC548
C15
1uF / 63v
R19
2K2
C19
100n
R17
120K
R15
120K
R18
1K
C14
10uF / 16v
C11
1uF/63v
POT
X4
PG203J
C24
CBS500E
R7
47K
R31
100
IC7B
74HCT04B
C4
470n
R2
47K
C1
470n
R1
390
C23
100p
IC7A
74HCT04B
C2
100n
D2'

MOTOROLA

MC6850 (1.0 MHz)
MC68A50 (1.5 MHz)
MC68B50 (2.0 MHz)

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

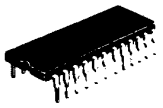
The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

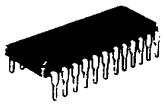
- 8- and 9-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 1.0 Mbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One- or Two-Stop Bit Operation

MOS
(N-CHANNEL, SILICON-GATE)

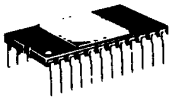
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER



S SUFFIX
CERDIP PACKAGE
CASE 623

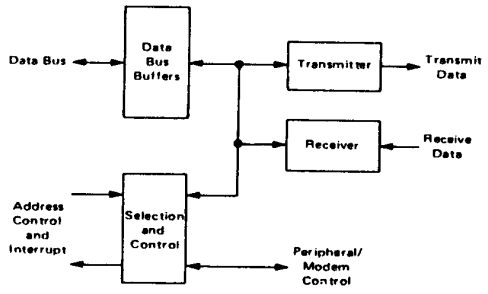


P SUFFIX
PLASTIC PACKAGE
CASE 709

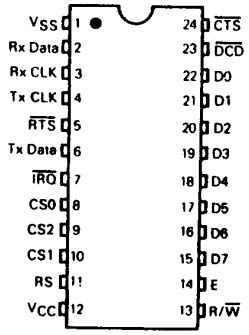


L SUFFIX
CERAMIC PACKAGE
CASE 716

MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6850, MC68A50, MC68B50 MC6850C, MC68A50C, MC68B50C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Ceramic Cerdip	θ_{JA}	 120 60 65	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage		V_{IL}	V_{SS}−0.3	–	V_{SS}+0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	R/W, CS0, CS1, CS2, Enable RS, Rx D, Rx C, CTS, DCD	I_{in}	–	1.0	2.5	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V)	D0-D7	I_{TSI}	–	2.0	10	μA
Output High Voltage (I_{Load} = −205 μA, Enable Pulse Width < 25 μs) (I_{Load} = −100 μA, Enable Pulse Width < 25 μs)	D0-D7 Tx Data, RTS	V_{OH}	V_{SS}+2.4 V_{SS}+2.4	– –	– –	V
Output Low Voltage (I_{Load} = 1.6 mA, Enable Pulse Width < 25 μs)		V_{OL}	–	–	V_{SS}+0.4	V
Output Leakage Current (Off State) (V_{OH} = 2.4 V)	IRQ	I_{LOH}	–	1.0	10	μA
Internal Power Dissipation (Measured at $T_A = T_L$)		P_{INT}	–	300	525	mW
Internal Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7 E, Tx CLK, Rx CLK, R/W, RS, Rx Data, CS0, CS1, CS2, CTS, DCD	C_{in}	– –	10 7.0	12.5 7.5	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	RTS, Tx Data IRQ	C_{out}	– –	– –	10 5.0	pF

SERIAL DATA TIMING CHARACTERISTICS

Characteristic		Symbol	MC6850		MC68A50		MC68B50		Unit
			Min	Max	Min	Max	Min	Max	
Data Clock Pulse Width, Low (See Figure 1)	÷ 16, ÷ 64 Modes	PW_{CL}	600	–	450	–	280	–	ns
	÷ 1 Mode		900	–	650	–	500	–	
Data Clock Pulse Width, High (See Figure 2)	÷ 16, ÷ 64 Modes	PW_{CH}	600	–	450	–	280	–	ns
	÷ 1 Mode		900	–	650	–	500	–	
Data Clock Frequency	÷ 16, ÷ 64 Modes	f_C	–	0.8	–	1.0	–	1.5	MHz
	÷ 1 Mode		–	500	–	750	–	1000	kHz
Data Clock-to-Data Delay for Transmitter (See Figure 3)		t_{TDD}	–	600	–	540	–	460	ns
Receive Data Setup Time (See Figure 4)	÷ 1 Mode	t_{RDS}	250	–	100	–	30	–	ns
Receive Data Hold Time (See Figure 5)	÷ 1 Mode	t_{RDH}	250	–	100	–	30	–	ns
Interrupt Request Release Time (See Figure 6)		t_{IR}	–	1.2	–	0.9	–	0.7	μs
Request-to-Send Delay Time (See Figure 6)		t_{RTS}	–	560	–	480	–	400	ns
Input Rise and Fall Times (or 10% of the pulse width if smaller)		t_r, t_f	–	1.0	–	0.5	–	0.25	μs

FIGURE 1 – CLOCK PULSE WIDTH, LOW-STATE

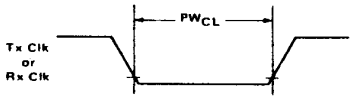


FIGURE 2 – CLOCK PULSE WIDTH, HIGH-STATE

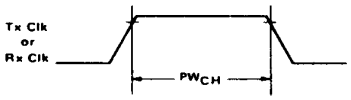


FIGURE 3 – TRANSMIT DATA OUTPUT DELAY

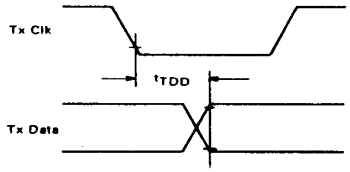


FIGURE 4 – RECEIVE DATA SETUP TIME (÷ 1 Mode)

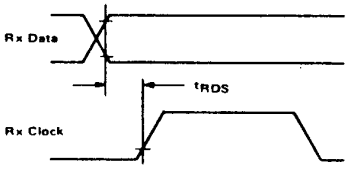


FIGURE 5 – RECEIVE DATA HOLD TIME (÷ 1 Mode)

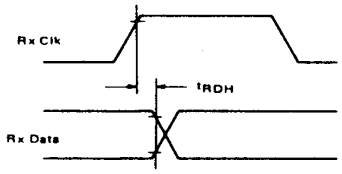
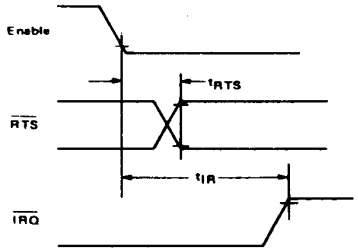


FIGURE 6 – REQUEST-TO-SEND DELAY AND INTERRUPT-REQUEST RELEASE TIMES

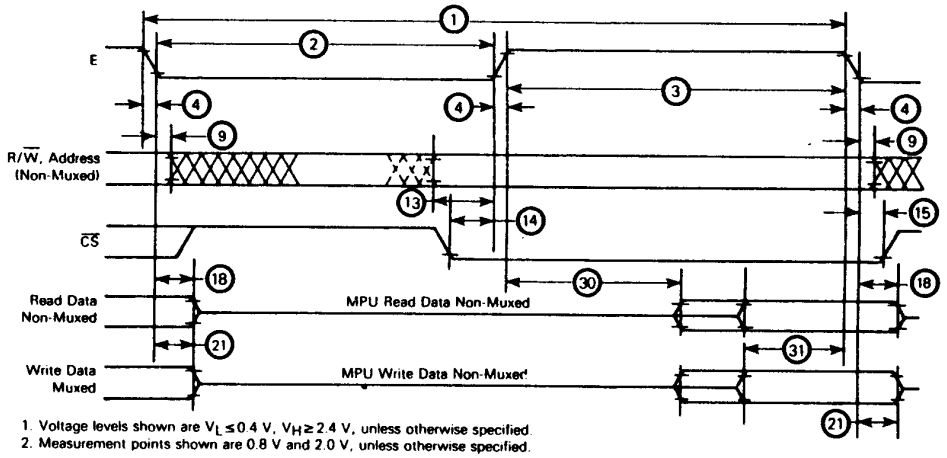


Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

BUS TIMING CHARACTERISTICS (See Notes 1 and 2 and Figure 7)

Ident. Number	Characteristic	Symbol	MC6850		MC68A50		MC68B50		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	µs
2	Pulse Width, E Low	PW_{EL}	430	9500	280	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	100	20	100	20	100	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

FIGURE 7 — BUS TIMING CHARACTERISTICS



1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 8 — BUS TIMING TEST LOADS

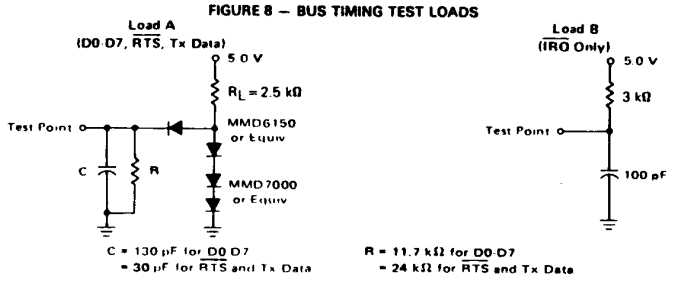
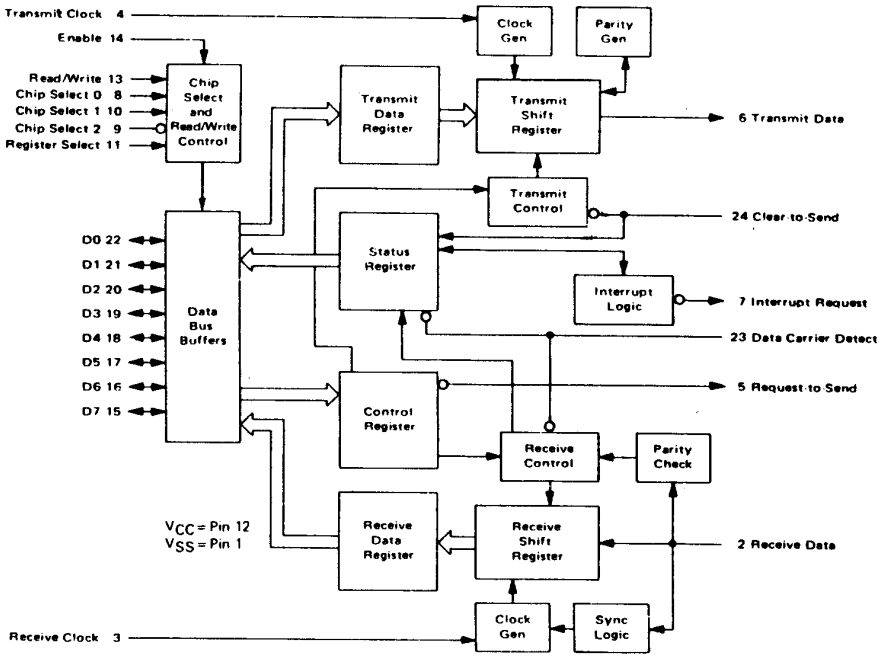


FIGURE 9 – EXPANDED BLOCK DIAGRAM



DEVICE OPERATION

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTS}$ outputs are held at level 1. On all other master resets, the $\overline{RTS}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of

double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

ACIA INTERFACE SIGNALS FOR MPU

The ACIA interfaces to the M6800 MPU with an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the ACIA.

ACIA Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation.

ACIA Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock or MC6809 E clock.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the ACIA.

Chip Select (CS0, CS1, $\overline{CS2}$) — These three high-impedance TTL-compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the ACIA are then performed under the control of the Enable Signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the ACIA being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the ACIA. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the ACIA. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

Transmit Clock (Tx CLK) — The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx CLK) — The Receive Clock input is used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) – The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (Tx Data) – The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) – This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) – The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The RTS output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect ($\overline{DCD}$) – This high-impedance TTL-compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low-to-high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set. The Rx CLK must be running for proper $\overline{DCD}$ operation.

ACIA REGISTERS

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

TABLE 1 – DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • R/$\overline{W}$ Transmit Data Register (Write Only)	RS • R/$\overline{W}$ Receive Data Register (Read Only)	$\overline{RS}$ • R/$\overline{W}$ Control Register (Write Only)	$\overline{RS}$ • R/$\overline{W}$ Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear to Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request ($\overline{IRQ}$)

* Leading bit – LSB – Bit 0
** Data bit will be zero in 7 bit plus parity modes.
*** Data bit is "don't care" in 7 bit plus parity modes.

CONTROL REGISTER

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) – The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) – The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) – Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	$\overline{RTS}$ = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) – The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a low-to-high transition on the Data Carrier Detect ($\overline{DCD}$) signal line.

STATUS REGISTER

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0 – Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 – The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2 – The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 – The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 – Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 – Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has

been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

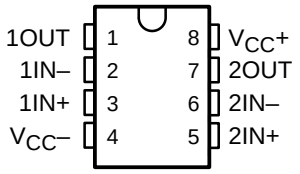
Parity Error (PE), Bit 6 – The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver partiy check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 – The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

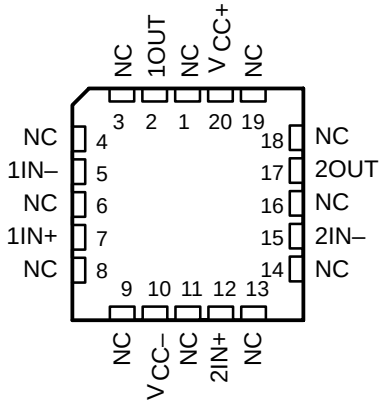
SLOS069B – FEBRUARY 1971 – REVISED SEPTEMBER 2002

- **Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Motorola MC1558/MC1458 and Signetics S5558/N5558**

MC1458 . . . D, P, OR PS PACKAGE
MC1558 . . . JG PACKAGE
(TOP VIEW)



MC1558 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The MC1458 and MC1558 are dual general-purpose operational amplifiers, with each half electrically similar to the μA741, except that offset null capability is not provided.

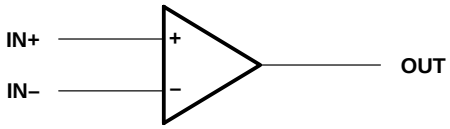
The high-common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

ORDERING INFORMATION

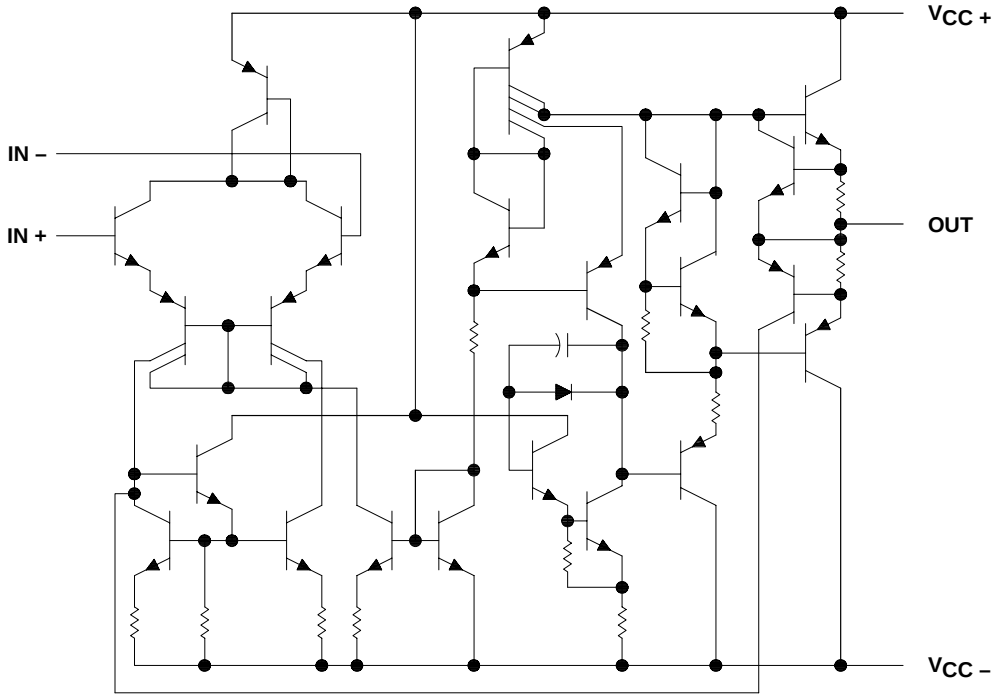
T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (P)	Tube	MC1458P	MC1458P
		SOIC (D)	Tube	MC1458D	MC1458
			Tape and reel	MC1458DR	
		SOP (PS)	Tape and reel	MC1458PSR	M1458
–55°C to 125°C	5 mV	CDIP (JG)	Tube	MC1558JG	MC1558JG
		CDIP (JGB)	Tube	MC1558JGB	MC1558JGB
		LCCC (FK)	Tube	MC1558FK	MC1558FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1): MC1458 . . . . . 18 V
MC1558 . . . . . 22 V
Supply voltage, V_{CC-} (see Note 1): MC1458 . . . . . –18 V
MC1558 . . . . . –22 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±30 V
Input voltage, V_I (either input, see Notes 1 and 3) . . . . . ±15 V
Duration of output short circuit (see Note 4) . . . . . Unlimited
Operating virtual junction temperature, T_J . . . . . 150°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 97°C/W
P package . . . . . 85°C/W
PS package . . . . . 95°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8): FK package . . . . . 5.61°C/W
JG package . . . . . 14.5°C/W
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, P, or PS package . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output can be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		±5	±15	V
T_A	Operating free-air temperature range	MC1458	0	70	°C
		MC1558	–55	125	

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6		1	5	mV
			Full range			7.5			6	
I_{IO}	Input offset current	V_O = 0	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	20	200		50	200		V/mV
			Full range	15			25			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	R_L = 2 kΩ, V_O ≥ ±10 V, A_{VD} = 1, THD ≥ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕm	Phase margin	A_{VD} = 1	25°C		65			65		deg
	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3	2		0.3*	2		MΩ
r_o	Output resistance	V_O = 0, See Note 9	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, V_O = 0	25°C		30	150		30	150	μV/V
			Full range			150			150	
V_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, R_S = 0, f = 1 kHz, BW = 1 Hz	25°C		45			45		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load	25°C		3.4	5.6		3.4	5	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (both amplifiers)	V_O = 0, No load	25°C		100	170		100	150	mW
			Full range			200			200	
V_{O1}/V_{O2}	Crosstalk attenuation		25°C		120			120		dB

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All characteristics are specified under open-loop operating conditions with zero common-mode input voltage, unless otherwise specified. Full range for MC1458 is 0°C to 70°C and for MC1558 is –55°C to 125°C.

NOTE 9: This typical value applies only at frequencies above a few hundred hertz because of the effect of drift and thermal feedback.

operating characteristics, $V_{CC\pm}$ = ±15 V, C_L = 100 pF, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		0.3			0.3		µs
	Overshoot factor	V_I = 20 mV,	R_L = 2 kΩ		5			5		%
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ		0.5			0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

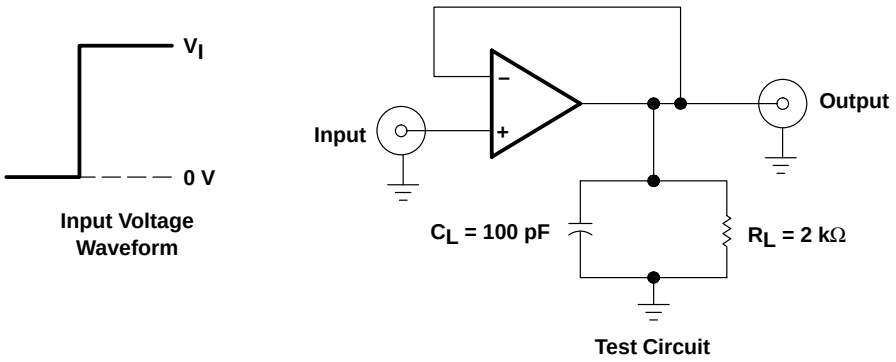


Figure 1. Rise-Time, Overshoot, and Slew-Rate Waveform and Test Circuit

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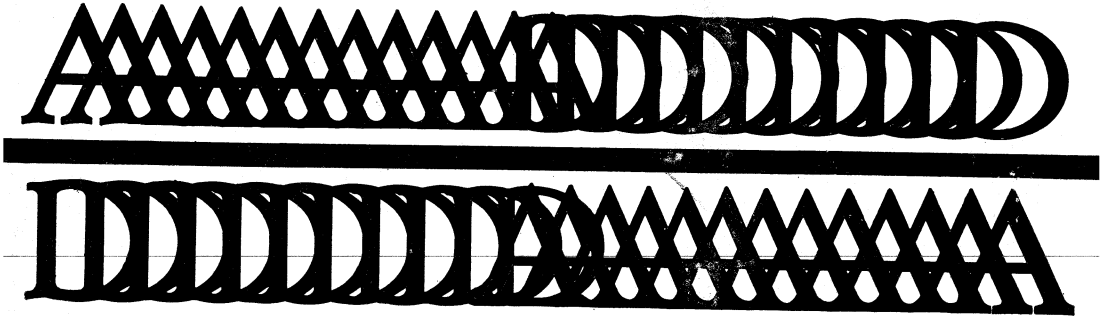
Technical Handbook
VOLUME 10

DATA CONVERTERS



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FERRANTI
DATA CONVERTERS
AND REFERENCES

DATA CONVERTER AND REFERENCES HANDBOOK
- CONTENTS -

ALPHANUMERICAL INDEX

1. Digital-to-Analogue Converters

Contents

PRODUCT SELECTION GUIDE D TO A CONVERTERS

TYPE	USEFUL RESOLUTION (BITS)	SETTLING TIME (μs)	ON-CHIP REFERENCE	INPUT LATCH	TEMPERATURE RANGE (°C)	FEATURES	PAGE
ZN425E SERIES	8 to 6	1	+	–	0 to 70	D to A with on-chip counter	1-13
ZN425J-8	8	1	+	–	-55 to +125	D to A with on-chip counter	1-13
ZN426E SERIES	8 to 6	1	+	–	0 to 70	TTL and CMOS compatible	1-21
ZN426J-8	8	1	+	–	-55 to +125	TTL and CMOS compatible	1-21
ZN428E-8	8	0,8	+	+	0 to 70	Microprocessor, TTL and CMOS compatible	1-27
ZN428J-8	8	0,8	+	+	-55 to +125	Microprocessor, TTL and CMOS compatible	1-27
ZN429E-8	8	1	–	–	0 to 70	Low cost, TTL and CMOS compatible	1-37
ZN429J-8	8	1	–	–	-55 to +125	Low cost, TTL and CMOS compatible	1-37
ZN434E	4	0,3	$V_{CC}/2$	–	0 to 70	Low cost, TTL and CMOS compatible	1-43
ZN435E	8	0,8	+	–	0 to 70	D to A, up/down counter, clock-generator	1-47
ZN435J	8	0,8	+	–	-55 to +125	D to A, up/down counter, clock-generator	1-47
ZN436E	6	1	–	–	0 to 70	Low cost, TTL and CMOS compatible	1-61
ZN436J	6	1	–	–	-55 to +125	Low cost, TTL and CMOS compatible	1-61

1. DIGITAL TO ANALOGUE CONVERTERS

A Digital to Analogue converter (DAC) is a device which converts a digital data input into a corresponding analogue output. This output usually takes the form of a voltage or current.

1.1 Ideal Output Characteristics

If a unipolar voltage output and normal binary input coding are assumed, then the ideal transfer function of a linear DAC may be written as:

$$V_{out} = V_{FS} (B_1.2^{-1} + B_2.2^{-2} + B_3.2^{-3} + \ldots\ldots + B_n.2^{-n})$$

where B_1 is the most significant bit input (MSB) and B_n is the least significant bit input (LSB). Bits 1 to n can each assume a value of '1' or '0'. The number of bit inputs a DAC possesses is known as the RESOLUTION of the converter.

The smallest increment of output voltage is that contributed by the LSB and is equal to $V_{FS}.2^{-n}$.

The terms 'MSB', 'LSB' etc., are frequently used interchangeably to describe either the digital input or the corresponding analogue output.

The maximum output from a DAC is known as full-scale output (V_{FSO}). It occurs when all inputs are '1' and is equal to $V_{FS}\left(\frac{(2^n-1)}{2^n}\right)$. For example the maximum output of a 3-bit DAC is $\frac{7}{8} V_{FS}$.

The transfer function graph of an ideal 3-bit DAC is shown in figure 1. For each of the 8 input codes there exists a discrete analogue output

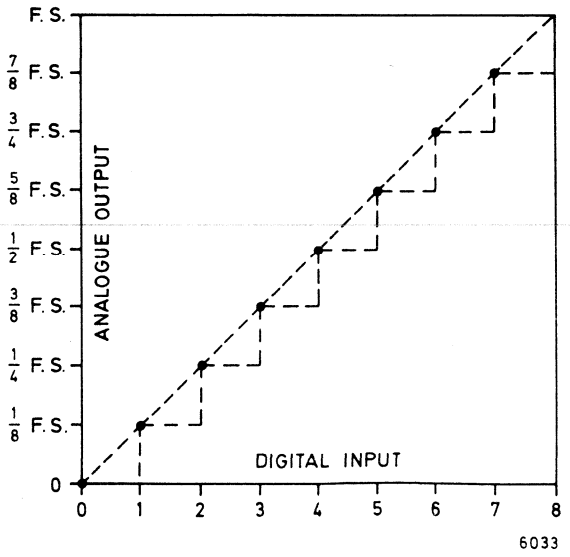


Fig. 1. Transfer Characteristic of Ideal 3-bit DAC

level, represented by a point on the graph. It should be emphasised that the transfer characteristic is not a continuous function and it is, therefore, not strictly correct to join the points with a continuous line, since this would imply that non-integral input codes and corresponding levels existed. However, a straight line is often drawn between zero and full scale to represent the 'ideal' transfer function on which all the points should lie.

Similarly, if the input code of a DAC is incremented using, say, a binary counter and clock generator, then the analogue output will be a staircase waveform. DAC transfer functions are frequently drawn as a staircase, since this is a convenient way of illustrating various errors that may occur in a DAC. However, such a graph is, strictly speaking, a plot of analogue output v. time rather than output v. input code.

1.2 Practical DAC Circuits

Figure 2 shows an example of a 3-bit DAC circuit based on a voltage-switching R-2R ladder network, a technique widely used in Ferranti converters.

Each 2R element is connected either to 0 volts or V_{FS} (V_{REF}) by transistor switches. Binary weighted voltages are produced at the output of the R-2R ladder, the value being proportional to the digital input number.

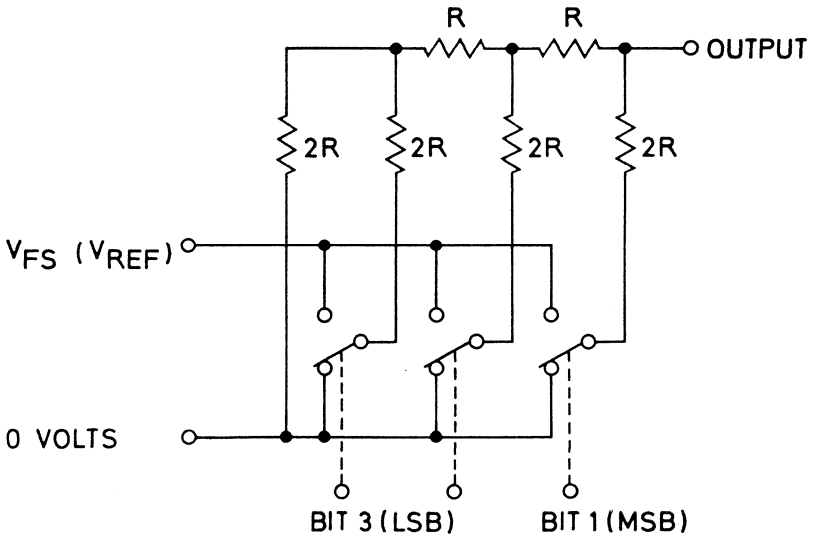


Fig. 2. 3-bit Voltage Switching DAC

For example, it is fairly easy to see that if bit 1 is '1' and bits 2 and 3 are '0' then an output of $V_{FS}/_2$ is produced. This is because the resistance of the ladder looking from the output through the first R is 2R, which forms a 2:1 attenuator with the 2R in series with the MSB switch. Output voltages for other input codes can similarly be calculated, and it can be seen that the ladder may be extended to any number of bits.

The voltage switching ladder technique is used in the ZN426, ZN428 and ZN429 series of D to A converters and also in the ZN425 dual-purpose A to D/D to A converter.

1.3 D to A Parameters and Definitions

1.3.1 Converter Errors

The ideal DAC assumes that all the resistors are perfectly matched and that the switches have zero resistance. In a practical converter this will not be the case and various errors will occur in the output.

1.3.2 Monotonicity

When the input code of a DAC is increased in 1 LSB steps the analogue output of the DAC should also increase, staircase fashion. If the output always increases in this manner then the DAC is said to be monotonic, i.e. the output is a single-valued function of the input. If, due to errors in the bit weighting, the output of the DAC decreases at any step, as shown in figure 3, then the DAC is said to be non-monotonic.

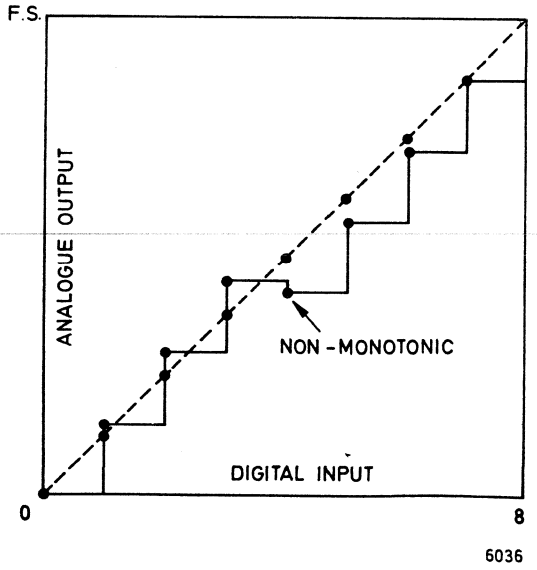


Fig. 3. Non-monotonic DAC

1.3.3 Offset (Zero Error)

Assuming unipolar operation and normal binary coding, when the input code is zero then the DAC output should also be zero. However, due to package lead resistances and offset voltages in the switches this will not be the case, and a small output offset may exist. This has the effect of shifting the transfer function so that it no longer passes through zero, as shown in figure 4.

1.3.4 Gain Error

If the reference voltage of a DAC is exactly the nominal value then the transfer characteristics of the converter should follow the ideal straight line. However, due to imperfections in the converter the transfer function may diverge from this line, as shown in figure 4. This error is known as gain error and is the difference between the slope of the actual transfer characteristic and the slope of the ideal transfer characteristic.

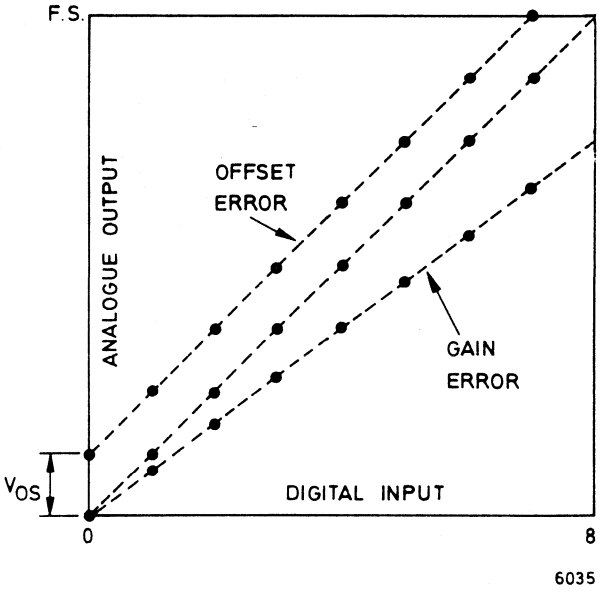


Fig. 4. Illustrating Offset and Gain Errors

1.3.5 Linearity Errors

Offset and gain errors may be trimmed out so that the end points of the transfer characteristic lie at zero and V_{FSO}. However, even when this has been done, some or all of the intermediate points may not lie on the 'ideal' line. These errors, which cannot be trimmed out, are known as linearity errors.

1.3.6 Non-Linearity (Linearity Error)

This is the maximum amount, given either as a percentage of full scale or a fraction of an LSB, by which any point on the transfer characteristic deviates from the ideal straight line passing through zero and V_{FSO}. Non-linearity is illustrated in figure 5. A linearity error within the range $\pm\frac{1}{2}$ LSB assures monotonic operation. Note however that the converse is not true and a DAC may still be monotonic with large linearity errors, which is also shown by figure 5.

1.3.7 Differential Non-linearity

This is the maximum difference, specified as a fraction of an LSB, between the actual and ideal size of any one LSB analogue increment. This can be seen as an error in the step height of a DAC staircase. A positive value of differential non-linearity means that the step height is larger than nominal, whilst a negative value means that it is smaller than nominal. If it is more negative than –1 LSB then the DAC is non-monotonic. However, positive differential non-linearity may assume any value and a DAC can still be monotonic, as shown in figure 5.

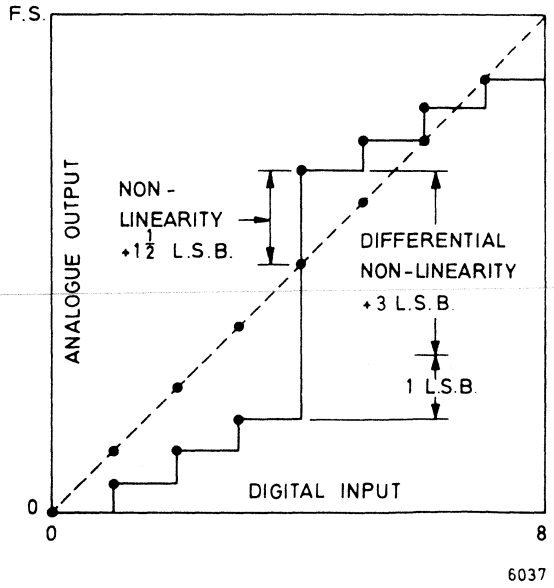


Fig. 5. Illustrating Linearity Errors

D to A Converters

1.3.8 Resolution

As stated earlier, the resolution of a DAC is simply the number of bit inputs that a DAC possesses, which indicates the smallest analogue increment that the converter can produce as a fraction of V_{FS}, e.g. 8 bits = 1 part in 2^8 (256). Resolution implies nothing about the accuracy of a DAC, which is defined by linearity and other errors.

1.3.9 Useful Resolution

If an n bit DAC has a differential non-linearity of say –1.5 LSB then it is non-monotonic. However, if the LSB input is made permanently '0' then the DAC becomes an n – 1 bit device with an LSB equal to twice the original LSB. The differential non-linearity error thus becomes –0.75 (new) LSB and the device is monotonic at a resolution of n – 1 bits. This is illustrated in figure 6, which shows the transfer characteristic of a 3-bit DAC that has a useful resolution of 2 bits.

Due to manufacturing tolerances a proportion of n-bit converters will have only n – 1 or n – 2 bit useful resolution. In applications not requiring n –bit useful resolution these reduced resolution versions offer a significant price advantage. The useful resolution of Ferranti DACs is guaranteed over their full operating temperature range.

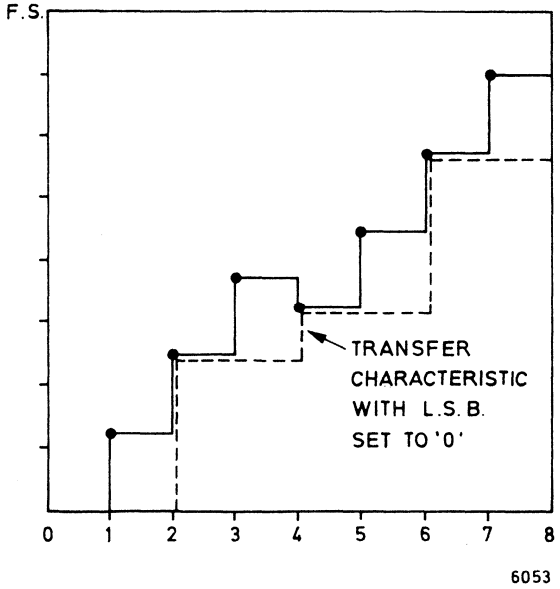


Fig. 6. Non-monotonic 3-bit DAC With a Useful Resolution of 2 bits

1.3.10 Settling Time is the time taken after a transition of the input code for the output of a DAC to settle to within $\pm\frac{1}{2}$ LSB of its final value. This varies depending on which bits are being changed. It may be specified for a change of 1 LSB which generally gives the most optimistic (fastest) figure. More conservative figures are given by the most major transition (where the MSB changes in one direction and all other bits change in the opposite direction, e.g. 01111111 to 10000000 or vice versa) or by a change from all bits off to all bits on (00000000 to 11111111) or vice versa.

1.4 Bipolar Operation

The discussion so far has been concerned only with DACs producing a single polarity (usually positive) output voltage. In some applications a bipolar (both positive and negative) output range may be required. This can be achieved by adding a negative offset of $\frac{V_{REF}}{2}$ to the analogue output, as shown in figure 7. For all input codes where the MSB is '0' the output voltage is then negative, and for output codes where the MSB is '1' the output voltage is positive. Where the input coding is normally binary but the output voltage is offset by $\frac{-V_{REF}}{2}$ then the input code is referred to as offset binary.

The transfer function of a 3-bit DAC with offset binary coding is shown in figure 8.

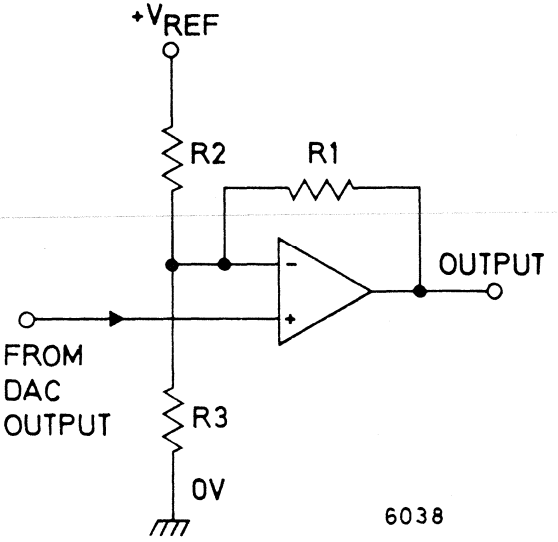


Fig. 7. Bipolar Operation of a DAC

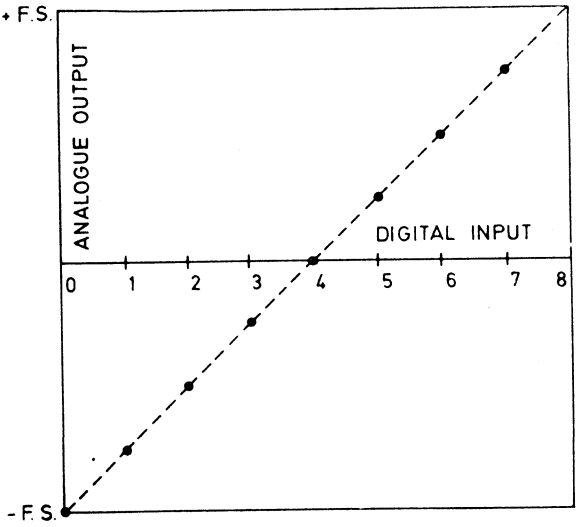


Fig. 8. Bipolar Operation of a 3-bit DAC

FERRANTI semiconductors

ZN425 Series

8 Bit Monolithic D to A/A to D Converter

FEATURES

- 8, 7 and 6 bit Accuracy
- 0°C to +70°C (ZN425E Series)
- –55°C to +125°C (ZN425J-8)
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time (D to A) 1 μsec Typical
- Conversion Time (A to D) 1 msec typical, using ramp and compare.
- Extra Components Required
  - D-A : Reference capacitor (direct voltage output through 10 kΩ typ.)
  - A-D : Comparator, gate, clock and reference capacitor

DESCRIPTION

The ZN425 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply merely by clocking the counter.

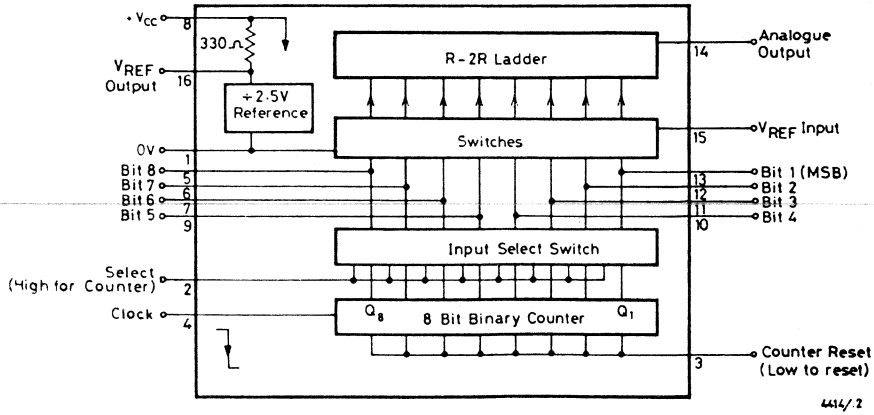


Fig. 1 – System Diagram

ZN425 Series

INTRODUCTION

The ZN425 is an 8-bit dual mode digital to analogue/analogue to digital converter. It contains an 8-bit D to A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including on the chip an 8-bit binary counter, analogue to digital conversion can be obtained simply by adding an external comparator (ZN424P) and clock inhibit gating (ZN7400E).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

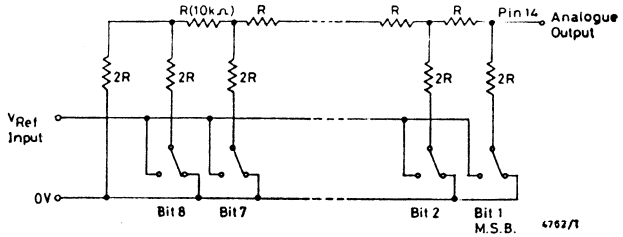


Fig. 2 – The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

ORDERING INFORMATION

Operating Temperature	8-bit Accuracy	7-bit Accuracy	6-bit Accuracy	Package
0°C to +70°C	ZN425E-8	ZN425E-7	ZN425E-6	Plastic
–55°C to +125°C	ZN425J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7·0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5·5 volts *See note 3*
Operating temperature range .. .. .. 0°C to +70°C (ZN425E Series)
–55°C to +125°C (ZN425J-8)
Storage temperature range .. .. –55°C to +125°C

CHARACTERISTICS (at T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified).

Internal voltage reference

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage	V_{REF}	2·4	2·55	2·7	volts	I = 7·5 mA (internal)
Slope resistance	R_s	—	2	4	ohms	I = 7·5 mA (internal)
V_{REF} Temperature coefficient		—	40	—	ppm/°C	I = 7·5 mA (internal)

Note: The internal reference requires a 0·22 μF stabilising capacitor between pins 1 and 16.

8-Bit D to A Converter and Counter

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN425J-8		8	—	—	bits	V_{REF} Input = 2 to 3V
ZN425E-8		8	—	—	bits	
ZN425E-7		7	—	—	bits	
ZN425E-6		6	—	—	bits	
Non-linearity		—	—	±0·5	L.S.B.	*See Note 3*
Differential non-linearity		—	±0·5	—	L.S.B.	*See Note 6*
Settling time		—	1·0	—	μs	1 L.S.B. step
Settling time to 0·5 L.S.B.		—	1·5	2·5	μs	All bits ON toOFF or OFF to ON
Offset voltage ZN425J-8	V_{OS}	—	8	12	mV	All bits OFF *See Note 3*
ZN425E-8, ZN425E-6, ZN425E-7		—	3	8	mV	
Full scale output		2·545	2·550	2·555	volts	All bits ON Ext. V_{REF}=2·56V
Full scale temperature coeff.		—	3	—	ppm/°C	Ext. V_{REF}=2·56V
Non-linearity error temp. coeff.		—	7·5	—	ppm/°C	Relative to F.S.R.
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3·0	volts	
Supply voltage	V_{CC}	4·5	—	5·5	volts	*See Note 3*
Supply current	I_s	—	25	35	mA	
High level input voltage	V_{IH}	2·0	—	—	volts	*See Notes 1 and 2*
Low level input voltage	V_{IL}	—	—	0·7	volts	

CHARACTERISTICS *(continued)*.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max. V_I = 2·4V
		—	—	100	μA	V_{CC} = max. V_I = 5·5V
Low level input current, bit inputs	I_{IL}	—	—	–0·68	mA	V_{CC} = max. V_I = 0·3V
Low level input current, clock reset and input select	I_L	—	—	–0·18	mA	
High level output current	I_{OH}	—	—	–40	μA	
Low level output current	I_{OL}	—	—	1·6	mA	
High level output voltage	V_{OH}	2·4	—	—	volts	V_{CC} = min. Q = 1 I_{load} = –40 μA
Low level output voltage	V_{OL}	—	—	0·4	volts	V_{CC} = min. Q = 0 I_{load} = 1·6 mA
Maximum counter clock frequency	f_c	3	5	—	MHz	*See Note 5*
Reset pulse width	t_R	200	—	—	ns	*See Note 4*

Notes:

1. The Input Select pin (2) must be held low when the bit pins (5, 6, 7, 9, 10, 11, 12 and 13) are driven externally.
2. To obtain counter outputs on bit pins the Input Select pin (2) should be taken to $+V_{CC}$ via a 1 kΩ resistor.
3. The ZN425J differs from the ZN425E in the following respects:
   (a) For the ZN425J, the maximum linearity error may increase to ±1 LSB over the temperature ranges –55°C to 0°C and +70°C to +125°C.
   (b) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.
   (c) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
4. The device may be reset by gating from its own counter.
5. F_{max} in A/D mode is 300 kHz, see page 1–18
6. Monotonic over full operating temperature range at resolution appropriate to accuracy.

If Pin 2 is high then the output equals the Q output of the corresponding counter.

If Pin 2 is low then the output transistor, Tr1 is held off.

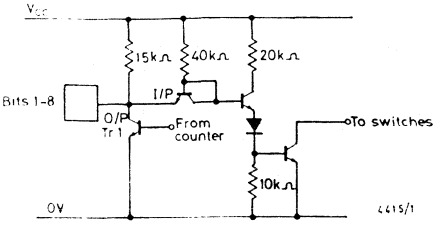


Fig. 3 – Bit Inputs/Outputs

APPLICATIONS

1. 8-bit D to A Converter

The ZN425 gives an analogue voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0·004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $\geqslant 650\ k\Omega$.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 4 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until $V_{out} = 0{\cdot}000V$.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading – 1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3·840 volts – 1 L.S.B.

= 3·825 volts

$$(1\ \text{L.S.B.} = \frac{3{\cdot}84}{256} = 15{\cdot}0\ \text{millivolts.})$$

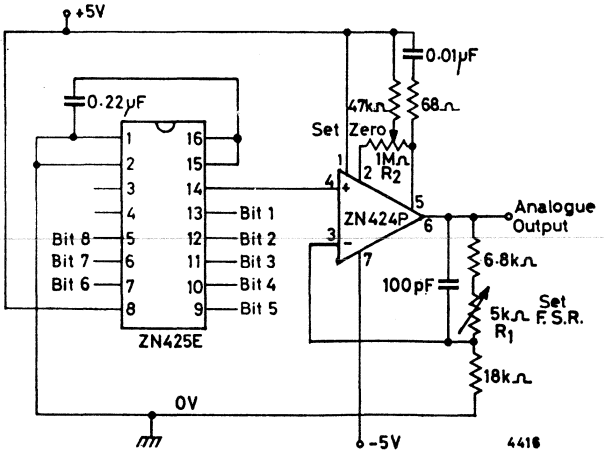


Fig. 4 – 8-bit Digital to Analogue Converter

2. 8-bit Analogue to Digital Converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig. 5. On the negative edge of the CONVERT COMMAND pulse (15 μs minimum) the counter is set to zero and the STATUS latch to logical 1. On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width to the ZN425 is 100 ns. The analogue output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS latch to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8 bit digital output is a valid representation of the analogue input voltage.

A small capacitor of 47 pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20–30 pF) and they form a time constant with the ZN425 output resistance (10 kΩ). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300 kHz. Using the ZN424P as a comparator the clock frequency should be restricted to 100 kHz. The conversion time varies with the input, being a maximum for full scale input.

$$\text{Maximum conversion time} = \frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$

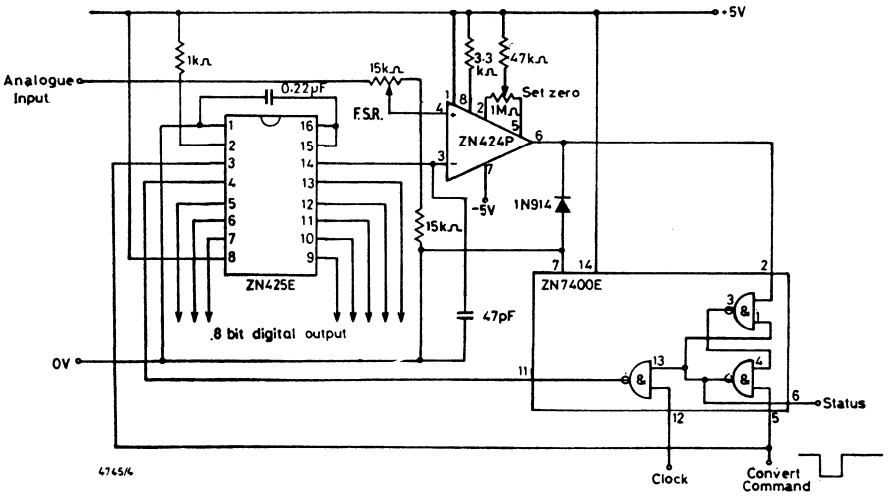


Fig. 5 – 8-bit Analogue to Digital Converter

3. Precision Ramp Generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 6 uses the same buffer stages as the D to A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.

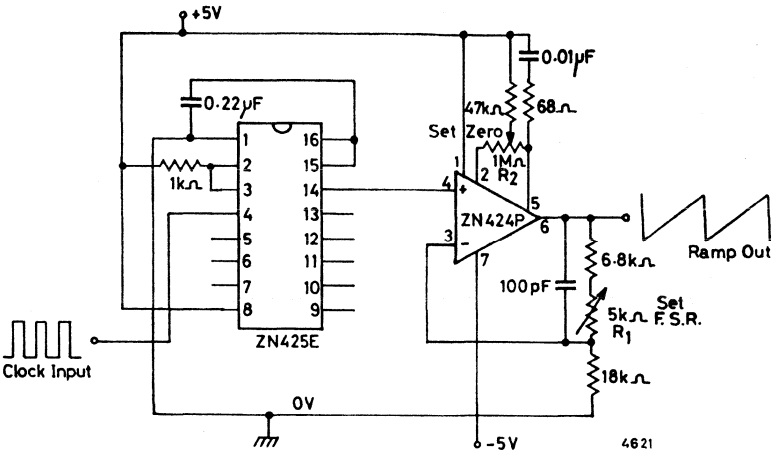


Fig. 6 – Precision Ramp Generator

4. Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer for both the 8-bit Digital to Analogue Converter (Fig. 4) and the Precision Ramp Generator (Fig. 6).

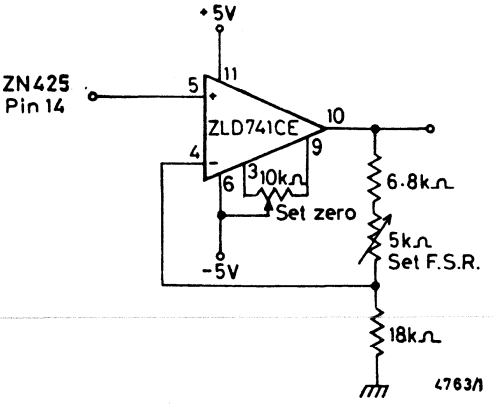


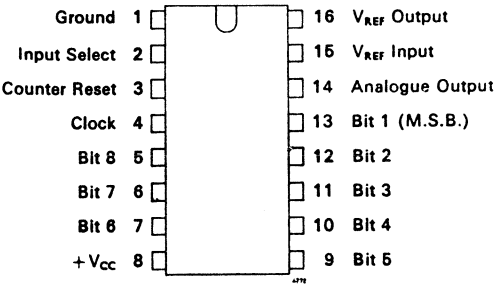
Fig. 7 – The ZLD741 as Output Buffer

5. Further Applications

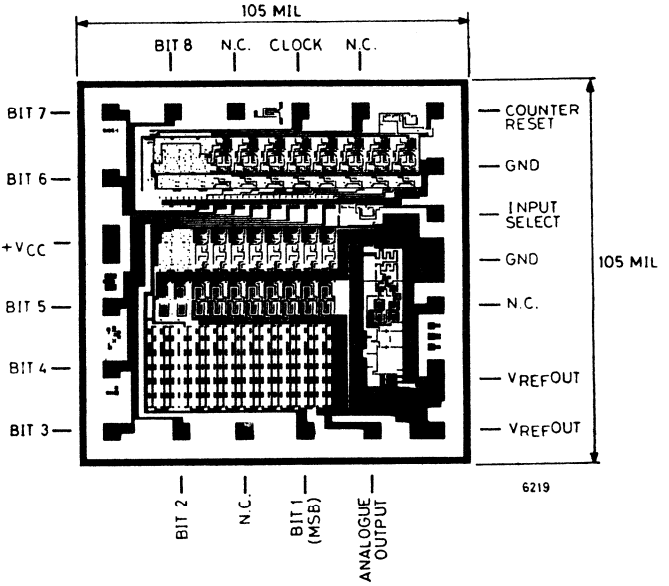
Details of a wide range of additional applications, described in the Ferranti publication 'Application Report–ZN425 8-bit A-D/D-A Converter', are also available.

ZN425 Series

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

D-A CONVERTER

ZN426 Series

8 Bit Monolithic D to A Converter

FEATURES

- 8, 7 and 6-bit Accuracy
- ZN426E Series Commercial Temp. Range 0°C to +70°C
- ZN426J-8 Military Temp. Range −55°C to +125°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 μsec. Typical
- Only Reference Capacitor and Resistor required

DESCRIPTION

The ZN426 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches and a 2.5V precision voltage reference.

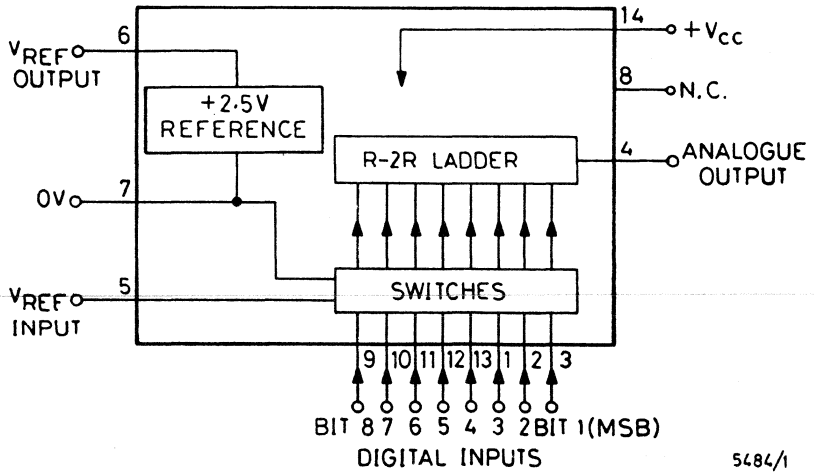


Fig. 1. System Diagram

ZN426 Series

INTRODUCTION

The ZN426 is an 8-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches plus a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. In this case there is no need to supply power to the internal reference so R_{REF} and C_{REF} can be omitted.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

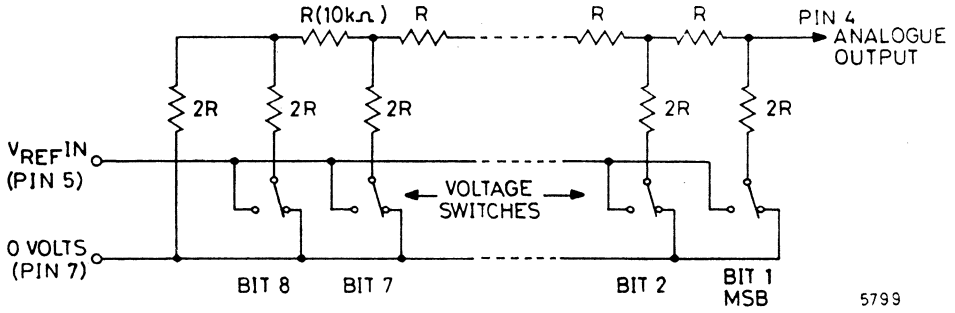


Fig. 2. The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder. the value depending on the digital number applied to the bit inputs.

ORDERING INFORMATION

Operating Temperature	8-bit accuracy	7-bit accuracy	6-bit accuracy	Package
0 to +70°C	ZN426E-8	ZN426E-7	ZN426E-6	Plastic
−55 to +125°C	ZN426J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts
Storage temperature range .. .. −55 to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 volts, T_{amb} = 25°C unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN426J-8, ZN426E-8		8	—	—	bits	V_{REF} input = 2.0 to 3.0 volts
ZN426E-7		7	—	—	bits	
ZN426E-6		6	—	—	bits	
Non-linearity		—	—	±0.5	L.S.B.	*Note 1*
Differential non-linearity		—	±0.5	—	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		—	1.0	—	μs	1 L.S.B. step
Settling time to 0.5 L.S.B.		—	2.0	—	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN426J-8	V_{OS}	—	5.0	8.0	mV	All bits OFF *Note 1*
ZN426E-8, ZN426E-7		—	3.0	5.0	mV	
ZN426E-6						
V_{OS} temperature coefficient		—	5	—	μV/°C	
Full scale output		2.545	2.550	2.555	volts	All bits ON Ext. V_{REF} = 2.560V
Full scale temp. coefficient		—	3	—	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		—	7.5	—	ppm/°C	Relative to F.S.R.

Notes:

1. The ZN426J-8 differs from the ZN426E-8 in the following respects:
   (a) For the ZN426J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1 LSB over the temperature ranges −55°C to 0°C and +70°C to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range at resolution appropriate to accuracy.

ELECTRICAL CHARACTERISTICS *(continued)*

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3.0	volts	
Supply voltage	V_{CC}	4.5	—	5.5	Volts	
Supply current	I_s	—	5	9	mA	
High level input voltage	V_{IH}	2.0	—	—	volts	
Low level input voltage	V_{IL}	—	—	0.7	volts	
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max., V_I = 2.4V
		—	—	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	—	—	−0.18	mA	V_{CC} = max., V_I = 0.3V
Internal Voltage Reference Output voltage	V_{REF}	2.475	2.55	2.625	volts	*Note** R_{REF} = 390Ω
Slope resistance	R_s	—	1	2	ohms	R_{REF} = 390Ω
V_{REF} temperature coefficient		—	40	—	ppm/°C	R_{REF} = 390Ω

*Note** The internal reference requires a 1 μF stabilising capacitor between pins 7 and 6 (C_{REF}) and a 390Ω resistor between pins 14 and 6 (R_{REF}).

APPLICATIONS

1. 8-bit D to A Converter

The ZN426 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0.004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $\geqslant$650 kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading −1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3·840 volts − 1 L.S.B. = 3·825 volts

$$(1 \text{ L.S.B.} = \frac{3 \cdot 84}{256} = 15.0 \text{ millivolts.})$$

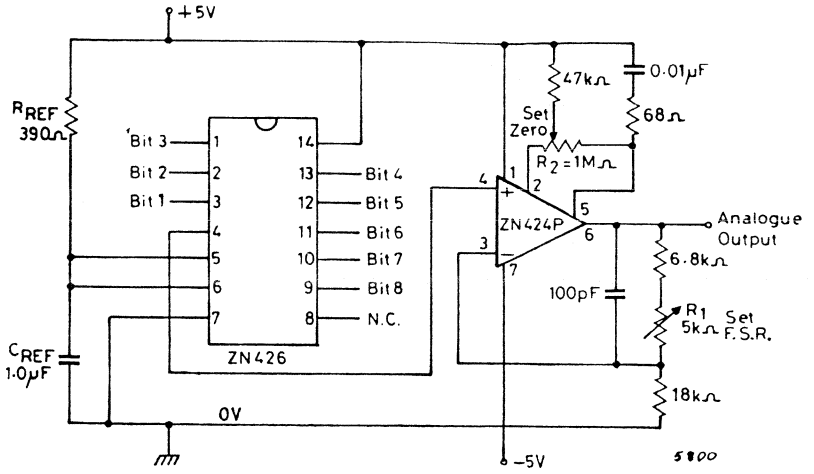


Fig. 3. 8-bit Digital to Analogue Converter

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).

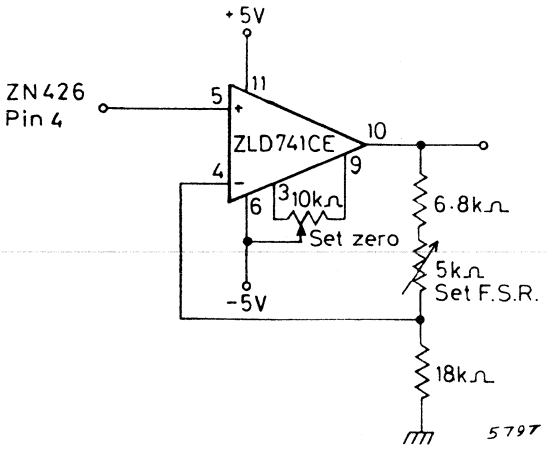
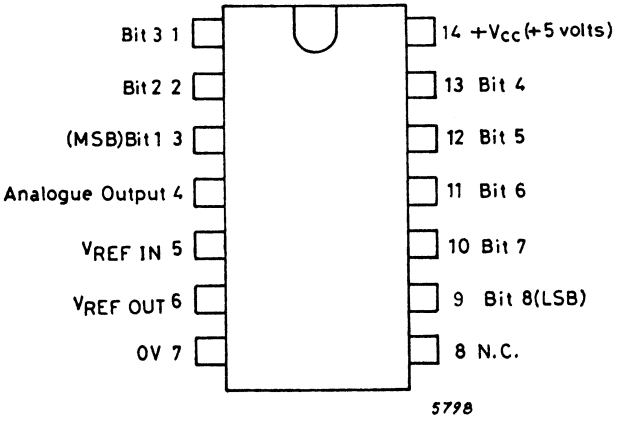
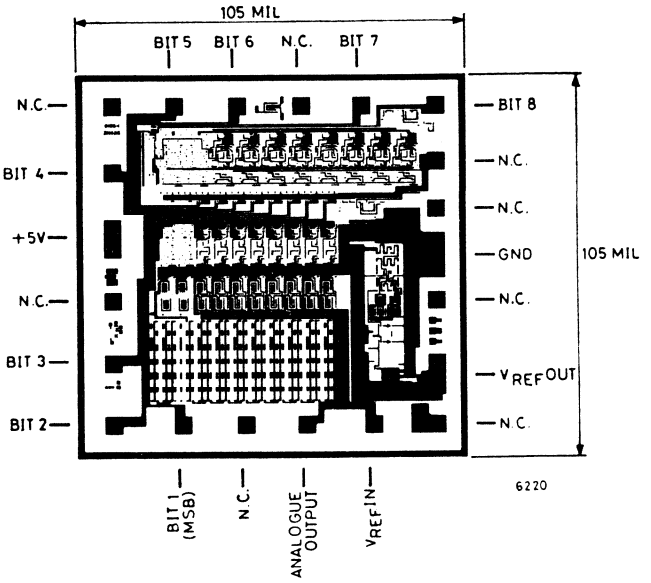


Fig. 4. The ZLD741 as Output Buffer

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

D to A CONVERTER

ZN428E-8
ZN428J-8

8 Bit Latched Input Monolithic D to A Converter

FEATURES

- Contains DAC with data latch and on-chip reference.
- Guaranteed monotonic over the full operating temperature range
- Single +5V supply
- Microprocessor compatible
- TTL and 5V CMOS compatible
- 800 ns settling time
- Complementary to ZN427 A to D Series
- ZN428E-8 Commercial temperature range 0°C to +70°C
- ZN428J-8 Military temperature range −55°C to +125°C

GENERAL DESCRIPTION

The ZN428 is a Monolithic 8 bit D to A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{Enable}}$ is LOW and the data is held when $\overline{\text{Enable}}$ is taken HIGH. The ZN428 also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

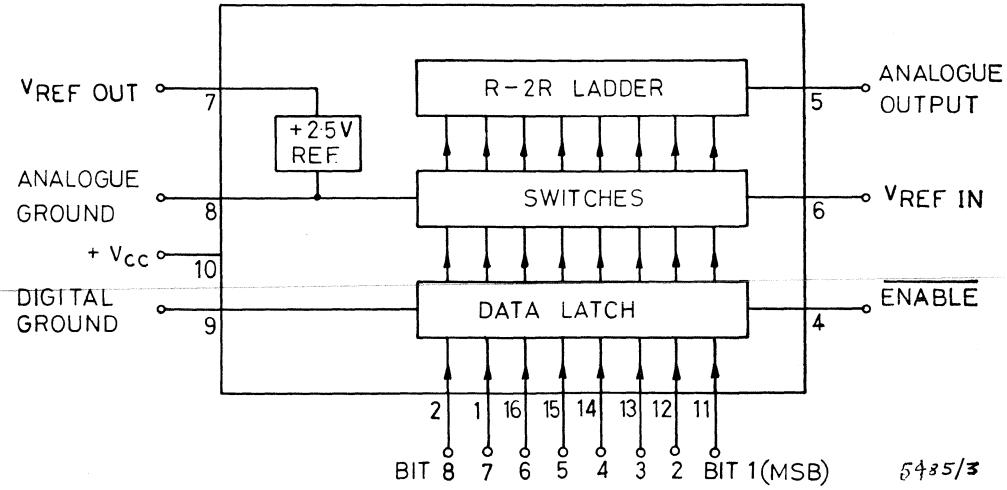


Fig. 1 SYSTEM DIAGRAM

ZN428E-8/J-8

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} input .. .. $+V_{CC}$
Operating temperature range .. .. 0°C to +70°C (ZN428E-8)
−55°C to +125°C (ZN428J-8)
Storage temperature range .. .. −55°C to +125°C
Analogue Ground to Digital Ground .. .. ±200 mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 volts, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output voltage	2.475	2.550	2.625	volts	R_{REF} = 390Ω, C_{REF} = 1 μF
Slope resistance		0.5	2	Ω	
$V_{REF\ OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D to A Converter					
Linearity error			±0.5	LSB	2.0V ⩽ $V_{REF\ IN}$ ⩽ 3.0V
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage T.C.		±6		μV/°C	
Full scale output	2.545	2.550	2.555		External reference $V_{REF\ IN}$ = 2.560 volts, all bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	volts	
Settling time to 0.5 LSB		800		ns	1 LSB Major Transition (Note 2)
		1.25		μs	All bits ON to OFF or OFF to ON (Note 2)
Operating temperature range:					
ZN428E-8	0		70	C	
ZN428J-8	−55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	volts	

Note 1 See REFERENCE
Note 2 R_L = 10 MΩ, C_L = 10 pF.

ELECTRICAL CHARACTERISTICS *(continued)*

	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range) High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	μA	V_{IN} = 5.5V V_{CC} = Max.
			20	μA	V_{IN} = 2.4V V_{CC} = Max.
Low level input current			−5	μA	V_{IN} = 0.4V V_{CC} = Max.
Input Clamp Diode Voltage		−1.5		V	I_{IN} = −8 mA
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH (V_{IH} = 3.5 volts).

Note 4 Set up time before $\overline{\text{Enable}}$ goes high.

Note 5 Hold time after $\overline{\text{Enable}}$ goes high.

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

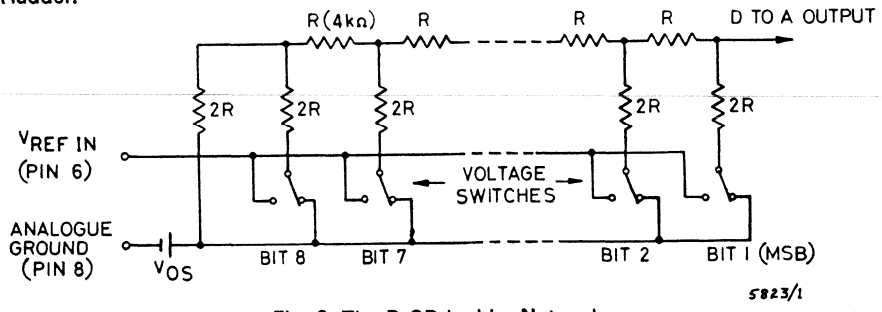


Fig. 2. The R-2R Ladder Network

$$\text{Analogue Output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the data latch.

V_{OS} is a small offset voltage produced by the D to A switch currents flowing through the package lead resistance. The value of V_{OS} is tyically 1 mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ($\pm 6\ \mu V/°C$) the effect on accuracy is negligible.

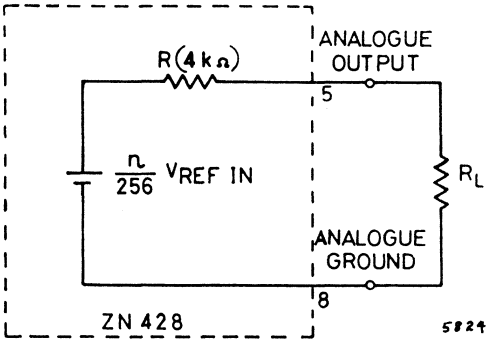


Fig. 3. Analogue Output Equivalent Circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

RL should be chosen to be as large as possible to make the gain drift small. As an example if R_L = 400 kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier (see APPLICATIONS section).

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5 volt Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of (5.0–2.5)/0.39 = 6.4 mA. A stabilising/decoupling capacitor, C_{REF} = 1 μF is required between pins 7 and 8 for internal reference operation, $V_{REF\ OUT}$ (pin 7) being connected to $V_{REF\ IN}$ (pin 6).

Up to five ZN428s may be driven from one internal reference (there is no need to reduce R_{REF}) This useful feature saves power and gives excellent gain tracking between the converters.

(b) External Reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5}{n}$ Ω, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3 volts for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2 volts.

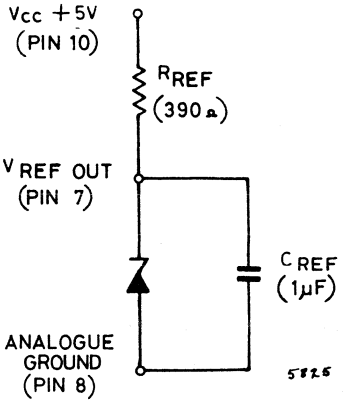


Fig. 4. Internal Voltage Reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the Enable input is low the data inputs drive the D to A directly. When Enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 5.

The ZN428 is provided with separate analogue and digital ground connections. The circuit will operate correctly with as much as ±200 mV between the two grounds.

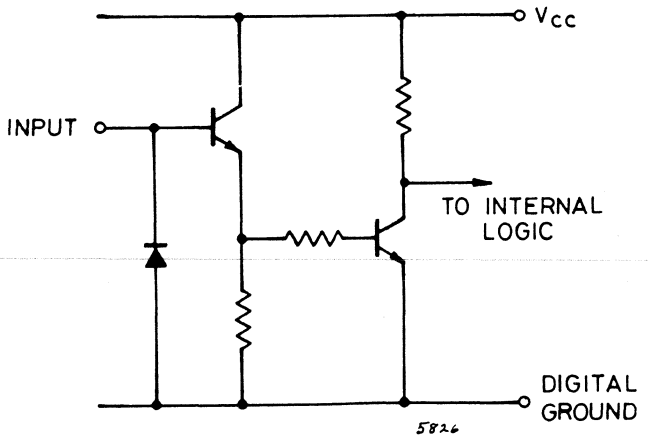


Fig. 5. Equivalent Circuit of All Inputs

APPLICATIONS

(1) Unipolar D to A Converter

The nominal output range of the ZN428 is 0 to $V_{REF\ IN}$ through a 4 kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5 μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.\ V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4 kΩ). The required nominal values of R1 and R2 are given by R1 = 4G kΩ and $R_2 = 4G/(G-1)$ kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Output Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5V and +10V output ranges are given in Fig. 7. Settling time for a major transition is 1.5 μs typical.

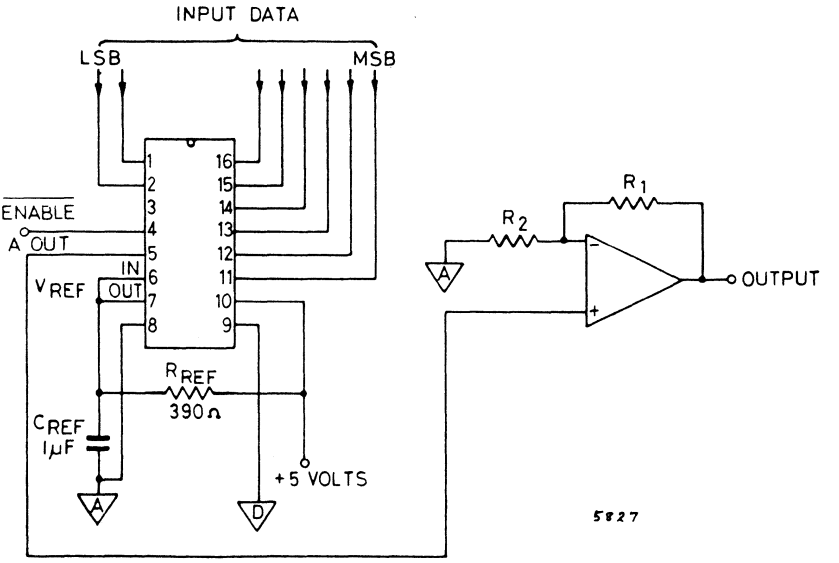


Fig. 6. Unipolar operation – Basic Circuit

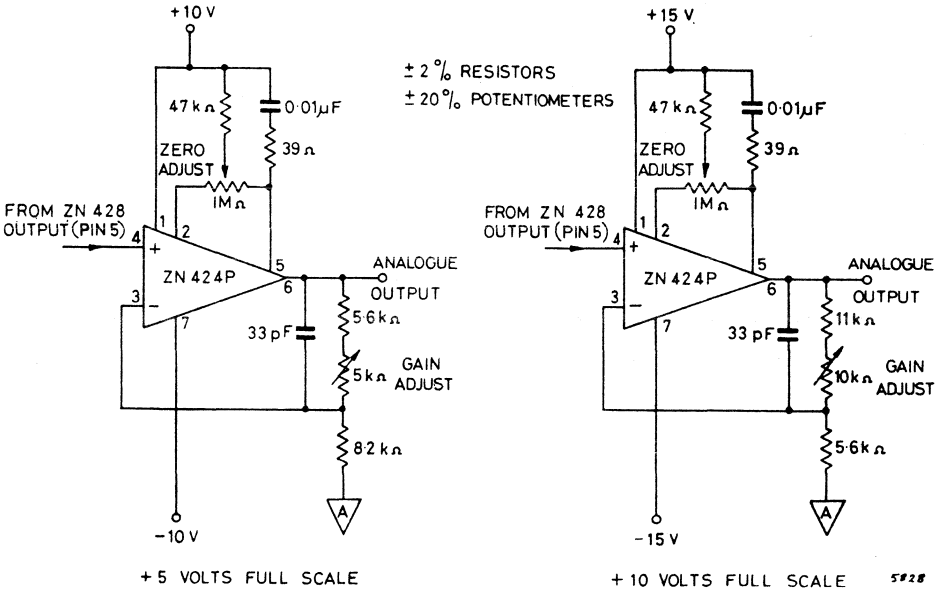


Fig. 7. Unipolar Operation – Component Values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.

(ii) Set all bits ON (high) and adjust gain until V_{OUT} = FS –1 LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS – 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1 mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analogue Output (Nominal value)
11111111	FS – 1LSB
11111110	FS – 2LSB
11000000	$\frac{3}{4}$ FS
10000001	$\frac{1}{2}$ FS + 1LSB
10000000	$\frac{1}{2}$ FS
01111111	$\frac{1}{2}$ FS – 1LSB
01000000	$\frac{1}{4}$ FS
00000001	1LSB
00000000	0

(2) **Bipolar D to A Converter**

For bipolar operation the output from the ZN428 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

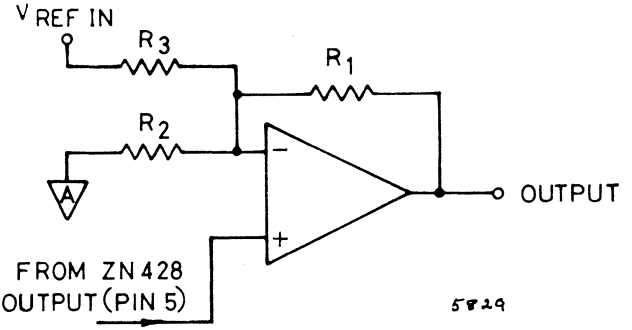


Fig. 8. Bipolar Operation – Basic Circuit

When the digital input to the ZN428 is zero the analogue output is zero and the amplifier output should be –Full scale. An input of all ones to the D to A will give a ZN428 output of $V_{REF\ IN}$ and the amplifier output required is + Full scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4 kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$$R_1 = 8G\ k\Omega,\ R_2 = 8G/(G-1)\ k\Omega \text{ and } R_3 = 8\ k\Omega$$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8\ k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for ±5V and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
±5V	2	16 kΩ	16 kΩ	8 kΩ
±10V	4	32 kΩ	10.66 kΩ	8 kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 9. Note that in the ±5V case R_3 has been chosen as 7.5 kΩ (instead of 8.2 kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5 μs typical.

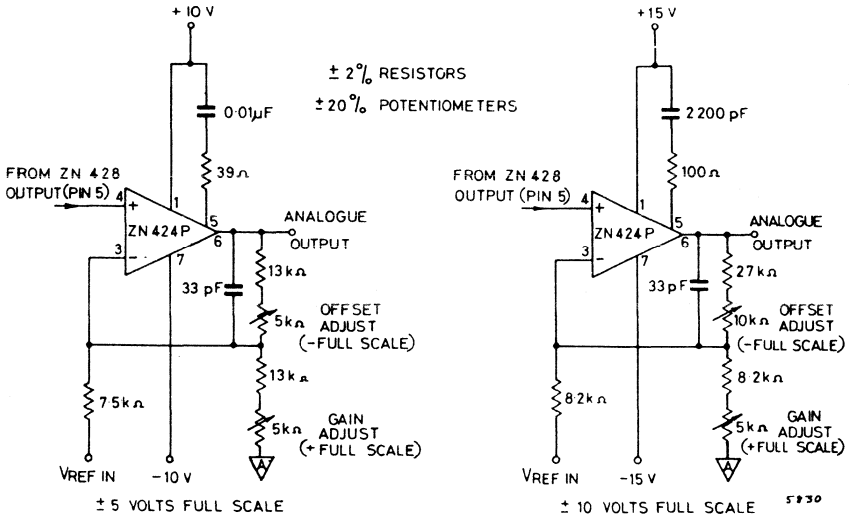


Fig. 9. Bipolar Operation – Component Values

Bipolar Adjustment Procedure

(1) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust offset until the amplifier output reads –Full Scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads +(Full Scale – 1LSB).

BIPOLAR SETTING UP POINTS

Input Range, ±FS	LSB	–FS	+(FS–1LSB)
±5V	39.1 mV	–5.0000V	+4.9609V
±10V	78.1 mV	–10.0000V	+9.9219V

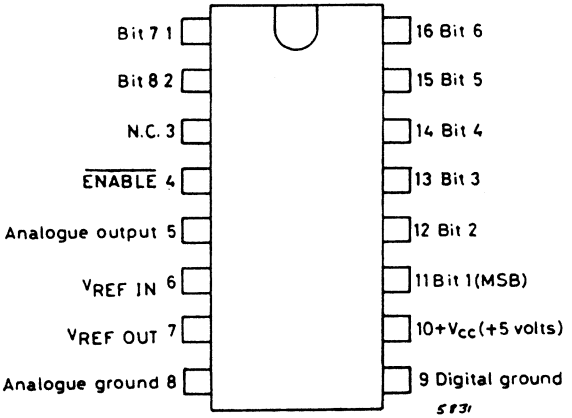
$$1\text{LSB} = \frac{2\text{FS}}{256}$$

BIPOLAR LOGIC CODING

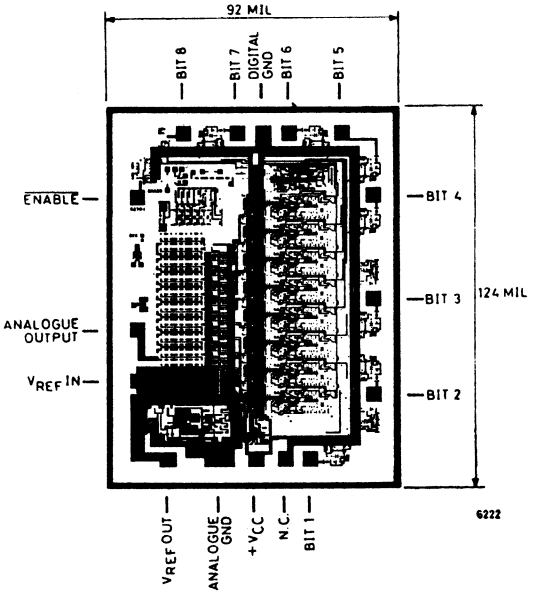
Input Code (Offset Binary)	Analogue Output (Nominal Value)
11111111	+(FS – 1LSB)
11111110	+(FS – 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	–1LSB
01000000	–½FS
00000001	–(FS – 1LSB)
00000000	–FS

ZN428E-8/J-8

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

D-A CONVERTER

ZN429 Series

Low Cost 8 Bit Monolithic D to A Converter

FEATURES

- 8, 7 and 6-bit Accuracy
- ZN429E Series Commercial Temp. Range 0°C to +70°C
- ZN429J-8 Military Temp. Range −55°C to +125°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 μsec. Typical
- Designed for low-cost applications

DESCRIPTION

The ZN429 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

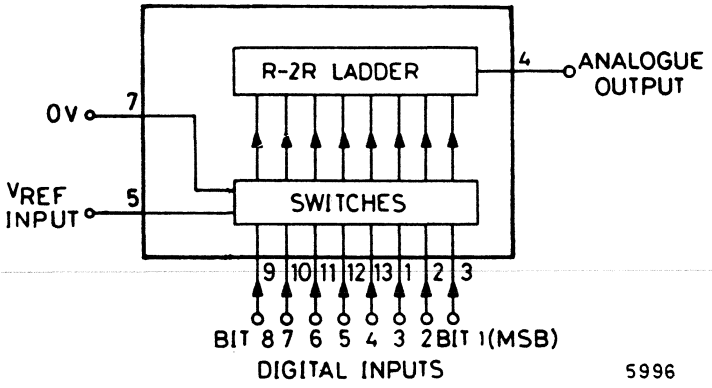


Fig. 1. System Diagram

ZN429 Series

INTRODUCTION

The ZN429 is an 8-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

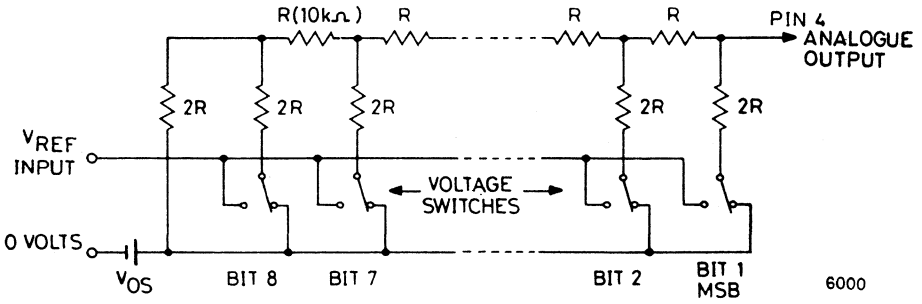


Fig. 2. The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2 ohms.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

ORDERING INFORMATION

Operating Temperature	8-bit accuracy	7-bit accuracy	6-bit accuracy	Package
0 to +70°C	ZN429E-8	ZN429E-7	ZN429E-6	Plastic
–55 to +125°C	ZN429J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts
Storage temperature range .. .. –55 to +125°C

CHARACTERISTICS (at T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN429J-8, ZN429E-8		8	—	—	bits	V_{REF} input = 2.0 to 3.0 volts
ZN429E-7		7	—	—	bits	
ZN429E-6		6	—	—	bits	
Non-linearity		—	—	±0.5	L.S.B.	*Note 1*
Differential non-linearity		—	±0.5	—	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		—	1.0	—	μs	1 L.S.B. step
Settling time to 0.5 L.S.B.		—	2.0	—	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN429J-8, ZN429E-8	V_{OS}	—	5.0	8.0	mV	All bits OFF *Note 1*
ZN429E-7, ZN429E-6		—	3.0	5.0	mV	
V_{OS} temperature coefficient		—	5	—	μV/°C	
Full scale output		2.545	2.550	2.555	volts	All bits ON Ext. V_{REF} = 2.560V
Full scale temp. coefficient		—	3	—	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		—	7.5	—	ppm/°C	Relative to F.S.R.

Notes:

1. The ZN429J-8 differs from the ZN429E-8 in the following respects:
   (a) For the ZN429J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1 LSB over the temperature ranges −55°C to 0°C and +70°C to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range at resolution appropriate to accuracy.

CHARACTERISTICS (*continued*)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3.0	volts	
Supply voltage	V_{CC}	4.5	—	5.5	volts	
Supply current	I_s	—	5	9	mA	
High level input voltage	V_{IH}	2.0	—	—	volts	
Low level input voltage	V_{IL}	—	—	0.7	volts	
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max., V_I = 2.4V
		—	—	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	—	—	–0.18	mA	V_{CC} = max., V_I = 0.3V

APPLICATIONS

1. 8-bit D to A Converter

The ZN429 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0.004% per °C (or 1 L.S.B./ 100°C) if R_L is chosen to be $\geqslant$650 kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading –1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3.840 volts – 1 L.S.B.
= 3.825 volts

$$(1 \text{ L.S.B.} = \frac{3.84}{256} = 15.0 \text{ millivolts})$$

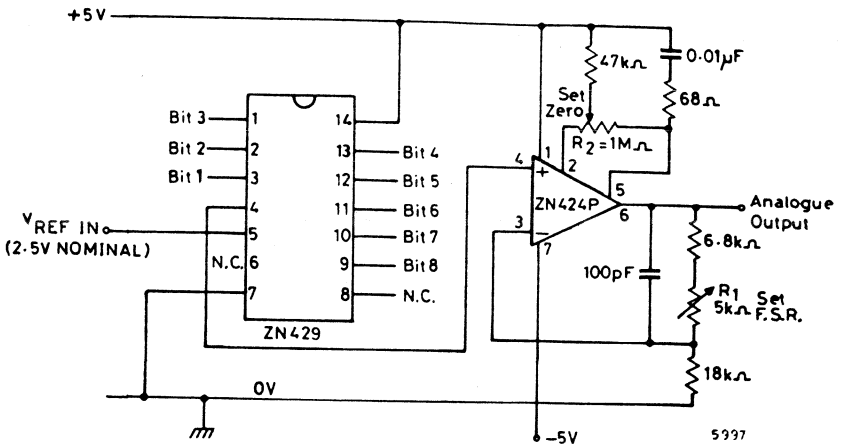


Fig. 3. 8-bit Digital to Analogue Converter

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).

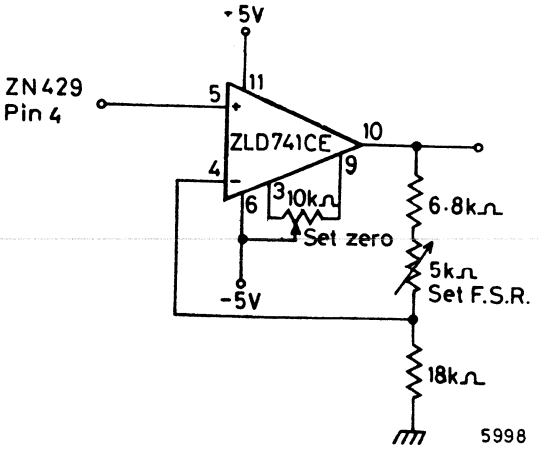
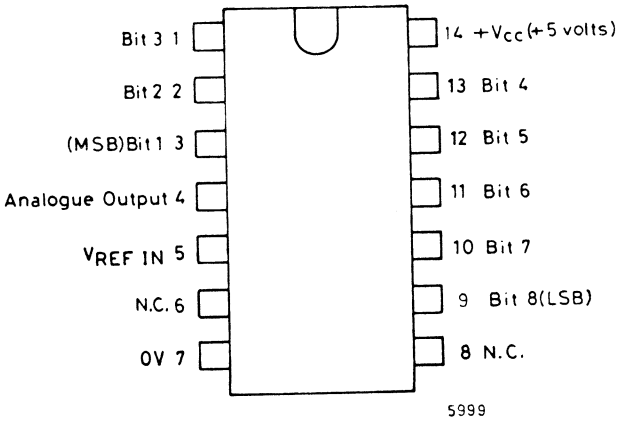


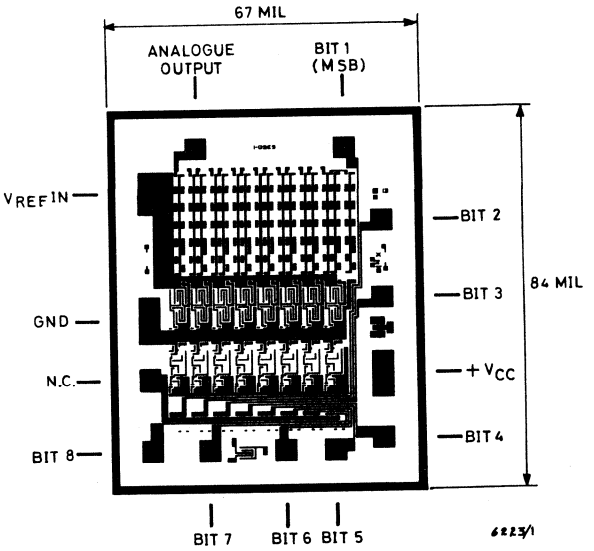
Fig. 4. The ZLD741 as Output Buffer

ZN429 Series

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

D-A CONVERTER

ZN434

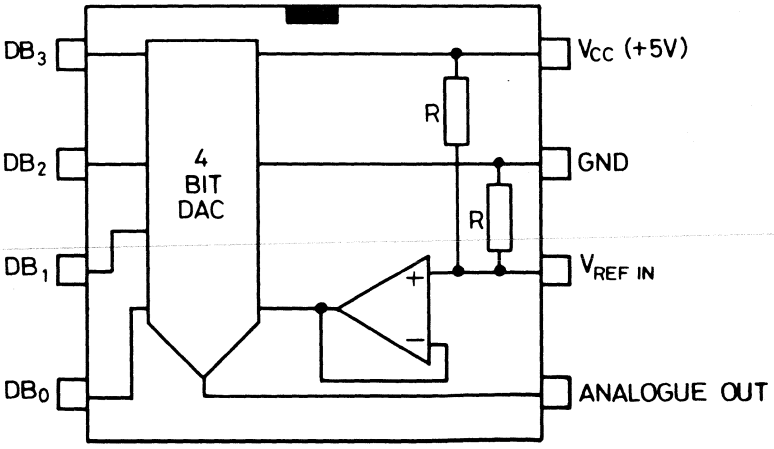
Low Cost 4 Bit D to A Converter

FEATURES

- 4 bit resolution
- ¼ LSB linearity
- Voltage output
- 300ns settling time
- TTL and CMOS compatible
- Single + 5V supply
- On-chip $\frac{V_{CC}}{2}$ reference
- 0°C to +70°C or −40°C to +85°C temperature range.

DESCRIPTION

The ZN 434 is a 4-bit DAC containing an R-2R ladder network of diffused resistors and precision bipolar switches. An on-chip reference amplifier and attenuator provide a reference voltage of $\frac{V_{CC}}{2}$, allowing the IC to function with no external components.



ZN 434 SYSTEM DIAGRAM

ZN434

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .. .. +7.0 volts
Logic and V_{REF} inputs .. .. 0 to V_{CC}

	Min	Max
Operating Temperature (ZN 434E)	0°C	+70°C
(ZN 434BE)	−40°C	+85°C
Storage Temperature	−55°C	+125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise stated)

Parameter	Min.	Typ.	Max.	Units	Conditions
D to A Converter Resolution	4	—	—	Bits	
Linearity error	—	—	±0.25	LSB	1.5V<$V_{REF\ in}$ < 3V
Differential Linearity error	—	—	±0.25	LSB	
Linearity error tempco	—	±3	—	ppm/°C	
Differential linearity error tempco	—	±6	—	ppm/°C	
Zero error	—	3.0	5.0	mV	
Zero error tempco	—	+6	—	µV/°C	
Full-scale output (V_{CC} as reference)	2.235	2.345	2.456	volts	
Full-scale output (External reference)	0.922	0.938	0.954	V_{ref} in	1.5V<$V_{REF\ in}$ < 3V
Full scale tempco	—	±3	—	ppm/°C	
Analogue output resistance	1.75	2.5	3.25	k	
Analogue output capacitance	—	15	—	pF	
Settling time to 0.5 LSB	—	200	300	ns	Code transition 0000 or 1111 1111 0000
	—	100	150	ns	1 LSB step
Supply voltage	+4.5	+5	+5.5	V	
Supply current	—	10	15	mA	

Parameter	Min.	Typ.	Max.	Units	Conditions
On chip reference amplifier					
Output voltage	$\frac{V_{CC} \times 0.97}{2}$	$\frac{V_{CC}}{2}$	$\frac{V_{CC} \times 1.03}{2}$		
Input current	—	1	—	μA	
Offset voltage		±10		mV	
Input resistance	9	18	27	k	
Logic Inputs					
High level input voltage V_{IH}	2.0	—	—	V	
Low level input voltage V_{IL}	—	—	0.8	V	
High level input current I_{IH}	—	—	10	μA	$V_{CC}=5.5V, V_I=2.4V$
	—	—	100	μA	$V_{CC}=V_I=5.5V$
Low level input current I_{IL}	—	—	180	μA	$V_{CC}=5.5V, V_I=0.3V$

CIRCUIT DESCRIPTION

D to A Converter

The ZN 434 is a 4 bit DAC consisting of an R-2R ladder of diffused resistors and precision bipolar switches designed for low offset voltage.

The ladder operates in the voltage switching mode and produces an output voltage $V_{out}=\frac{n}{16}(V_{REF\ IN}-V_{OS})+V_{OS}$, where n is the digital code set at the bit inputs and V_{OS} is a small offset voltage caused by the supply current flowing through the lead resistance of the ground pin.

On-chip Reference Amplifier

The ZN 434 contains a reference amplifier and attenuator that provide a reference voltage of nominally $\frac{V_{CC}}{2}$ without any external components. Taking into account the attenuator error, input current and offset voltage of the amplifier and gain error of the DAC the full-scale output will be within ± ½ LSB of the nominal value of $0.369 \times V_{CC}$.

By maintaining an accurate and stable supply voltage the ZN 434 may thus be used without an external reference. Where several ZN 434s are used in a system the V_{REF} inputs may be joined together to improve V_{REF} matching.

If a reference voltage other than $\frac{V_{CC}}{2}$ is required then the on-chip attenuator may be overridden, either by connecting a lower resistance attenuator in parallel or by using an active reference such as a bandgap reference source.

FERRANTI semiconductors

DATA CONVERTER

ZN435 E/J

8-Bit Multifunction Data Converter

ADVANCE PRODUCT INFORMATION

FEATURES

- Multimode device operates as:
  - —DAC
  - —ADC
  - —Tracking ADC
  - —Voltage to Frequency Converter
  - —Ramp and Sawtooth Generator
  - —Nonlinear Waveform Generator
  - —Voltage—Controlled Oscillator
  - —Track-and-Hold Circuit
- 8-bit Accuracy
- 800ns DAC Settling Time
- On-chip Up/down Counter
- On-chip Clock
- On-chip Voltage Reference
- Single + 5V supply
- Commercial or Military Temperature Range.

DESCRIPTION

The ZN435 is a versatile, multifunction 8-bit data conversion system. A voltage-output DAC, 8 bit up/down counter, stable 2.5v bandgap reference and clock generator are contained on a single chip.

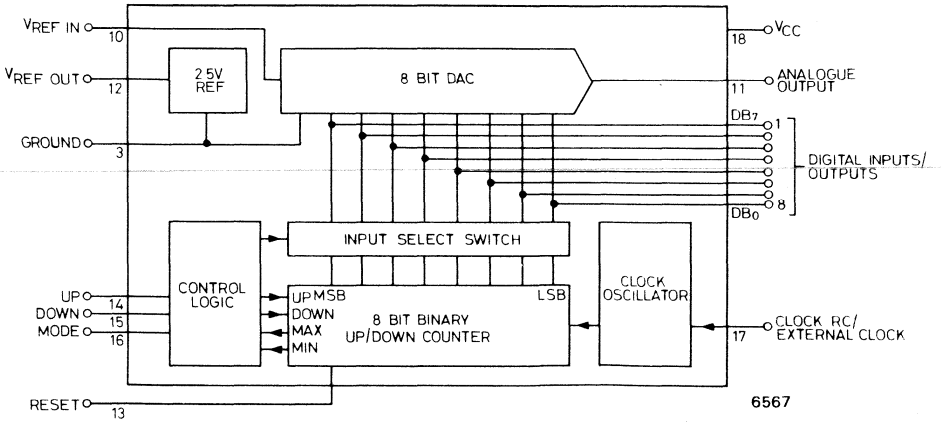


Fig. 1 SYSTEM DIAGRAM

ZN435

ABSOLUTE MAXIMUM RATINGS

Supply Votage, V_{CC} .. .. +7.0 volts
Max. Voltage, Logic and V_{REF} inputs .. .. V_{CC}

Operating Temperature Range

TYPE	T_{min}(°C)	T_{max}(°C)
ZN435E	0	+70
ZN435J	−55	+125

Storage Temperature Range .. −55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{REF} = 1.5−3.0V T_{amb} = +25°C unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
D TO A CONVERTER					
Resolution	8	—	—	bits	
Linearity Error	—	±0.25	±0.5	L.S.B.	T_{min} T_{amb} T_{max}
Differential Linearity Error	—	±0.25	±1	L.S.B.	
Zero Error	—	3.0	5.0	mV	ZN435E All bits OFF
	—	5.0	10.0	mV	ZN435J
Settling time to 0.5LSB	—	500	—	ns	All bits OFF to ON or
	—	800	—	ns	vice versa
Full-scale output	2.545	2.550	2.555	V	All bits ON, V_{REF} = 2.56V
Output Resistance	—	4	—	k	
Full-scale Temperature Coefficient	—	4	—	ppm/°C	Ext V_{REF} = 2.56V
Reference Voltage	0	—	3	V	

Parameter	Min.	Typ.	Max.	Units	Conditions
On-chip Voltage Reference					
Output Voltage	2.4	2.59	2.7	V	$R_{REF}=390\ \Omega$
Slope Resistance	—	2	4	Ω	$C_{REF}=220n$
Temperature Coefficient of V_{REF}	—	50	—	ppm/°C	
Reference Current	4	—	15	mA	
Counter (with external clock)					
High Level Threshold Voltage V_{T+}	—	—	2.3	V	
Low Level Threshold Voltage V_{T-}	1.7	—	—	V	
Maximum Clock Frequency	1	1.5	—	MHz	
On-chip Clock					
Maximum Frequency	500	—	—	KHz	
Clock Frequency Tempco	—	100	—	ppm/°C	
Clock Frequency Spread	—	—	1	%	Device to Device using same R&C
Clock Resistor	3	—	100	k	
Clock Capacitor	100	—	—	pF	
High Level Threshold Voltage V_{T+}	—	4.6	—	V	
Low Level Threshold Voltage V_{T-}	—	1.5	—	V	
Supply Rejection	—	0.8	—	%/V	
Logic Circuits					
BIT INPUTS					
High Level Input Voltage V_{IH}	2.0	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	—	−100	µA	$V_{IN}=2.4V$
Low Level Input Current I_{IL}	—	—	−220	µA	$V_{IN}=0.4V$
BIT OUTPUTS					
High Level Output Voltage V_{OH}	—	5.0	—		No Load
Low Level Output Voltage V_{OL}	—	0.1	—		
High Level Output Current I_{OH}	125	—	—	µA	$V_{OUT}=2.4V$
Low Level Output Current I_{OL}	−3.0	—	—	mA	$V_{OUT}=0.4V$

Parameter	Min.	Typ.	Max.	Units	Conditions
CONTROL INPUTS					
High Level Input Voltage V_{IH}	2	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	—	−25	μA	$V_{IN}=2.4V$
Low Level Input Current I_{IL}	—	—	−95	μA	$V_{IN}=0.4V$
Reset Pulse Width	200	—	ns		
Power Supply					
Supply Voltage	4.5	5	5.5	V	
Supply Current	—	35	45	mA	$V_{CC}=5.5V$

GENERAL CIRCUIT OPERATION

The ZN435 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN435 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

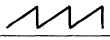
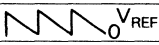
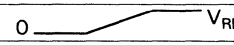
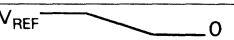
An on-chip oscillator is provided to drive the clock input of the up-down counter. The on-chip clock may be overriden by an external clock signal.

UP/DOWN COUNTER AND CONTROL LOGIC

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory. the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN435. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continuously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs are accessible from the I/o port.

A truth table for the control inputs is given in Table 1.

RESET	MODE	DOWN	UP	DIGITAL FUNCTION	ANALOGUE WAVEFORM
1	1	1	1	Counter Stopped.	
1	1	1	0	Count up continuously.	
1	1	0	1	Count down continuously.	
1	1	0	0	Count up, reverse at F.S., count down, reverse at zero.	
1	0	1	1	Counter Stopped.	
1	0	1	0	Count up, Stop at F.S.	
1	0	0	1	Count down, Stop at zero.	
X	0	0	0	DAC MODE, Counter output disabled. Counter can still be reset by taking reset input low.	
0	X	X	X	Counter reset. Does not affect analogue output in DAC MODE.	

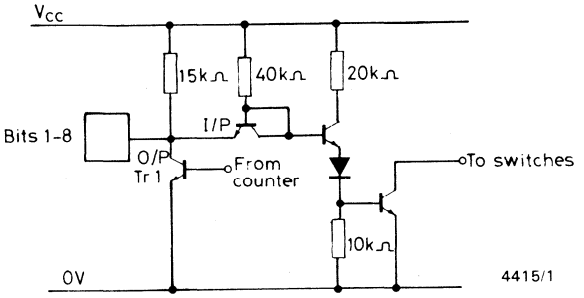


Fig. 2—BIT INPUTS/OUTPUTS

DATA PORT

One bit of the data port is shown in figure 2. The input/output pin is the junction of the counter output buffer and the DAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families.

CLOCK CIRCUIT

The on-chip clock circuit of the ZN435 is shown in figure 3.

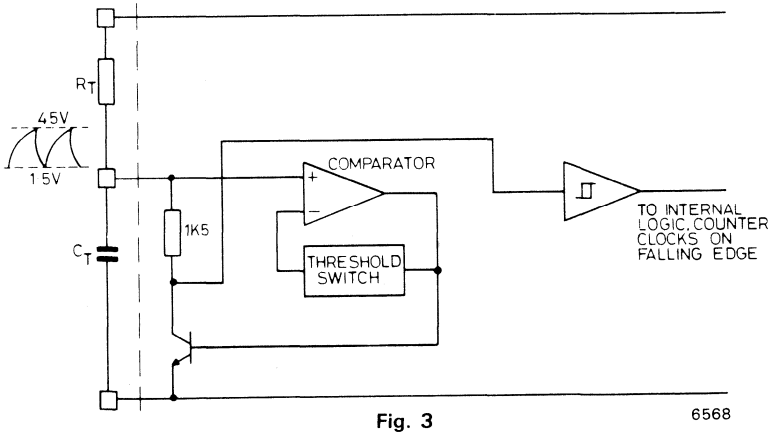


Fig. 3

The frequency of the clock is given by $f_{CLK} = \frac{1}{4R_TC_C}$ (Hz, ~, F)

Graphs of oscillator frequency versus resistor and capacitor values are given in figure 4.

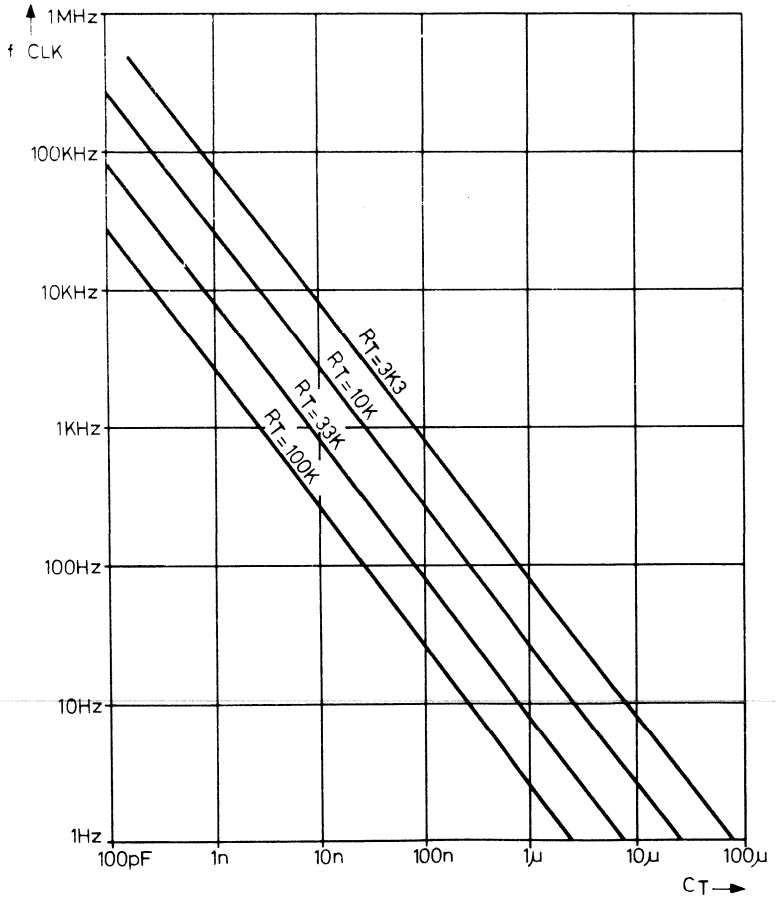


Fig. 4

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The external capacitor C_T is charged via the external resistor R_T to the upper threshold of the comparator (about +4.5v with V_{CC} = +5V). The comparator turns on the discharge transistor to discharge C_T and switches its threshold to the lower value of about 1.5V. When the voltage on C_T has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven direct from a TTL totem-pole output, as shown in figure 5a. If open collector or CMOS gates are used then their V_{OH} must be attenuated to below 4.5V, as shown in figures 5b and 5c. these thresholds the Schmitt trigger delivers clock pulses to the internal logic.

This slightly complicated arrangement has the advantage that the clock can be overdriven without turning on the discharge transistor, provided the drive voltage V_{OH} level does not exceed 4.5V.

The clock can be overdriven direct from a TTL totem-pole output, as shown in figure 5a. If open collector or CMOS gates are used then their V_{OH} must be attenuated to below 4.5V, as shown in figures 5b and 5c.

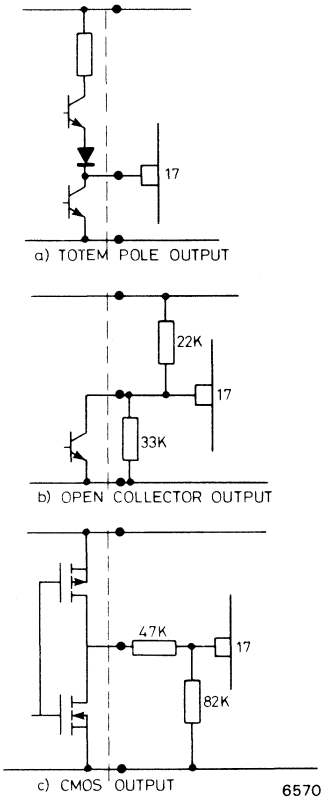


Fig. 5. OVERDRIVING THE CLOCK INPUT

ANALOGUE CIRCUITS

D TO A CONVERTER

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in figure 6.

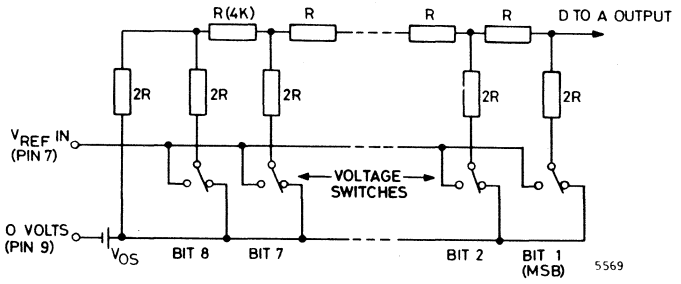


Fig. 6 R2-R LADDER NETWORK

Each 2R element is connected to either OV or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 3mV for the ZN435E and 5mV for the ZN435J. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0 volts to $V_{REF\ IN}$ with an output resistance R (4kΩ).

REFERENCE

ON-CHIP REFERENCE

The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig. 7).

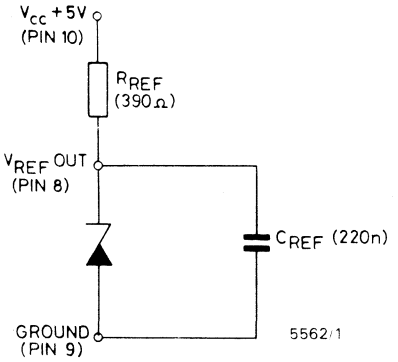


Fig. 7 INTERNAL VOLTAGE REFERENCE

An external resistor (R_{REF}) should be connected between pins 10 and 17 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor (C_{REF}) is required between pins 8 and 9.

To use the internal reference $V_{REF\ OUT}$ (Pin 12) is connected to $V_{REF\ IN}$ (Pin 10).

The recommended reference resistor of 390Ω will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN435s. Where several ZN435s are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

APPLICATIONS

The applications of the ZN435 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated.

WAVEFORM GENERATOR

The circuit of a low-frequency waveform generator is illustrated in figure 8.

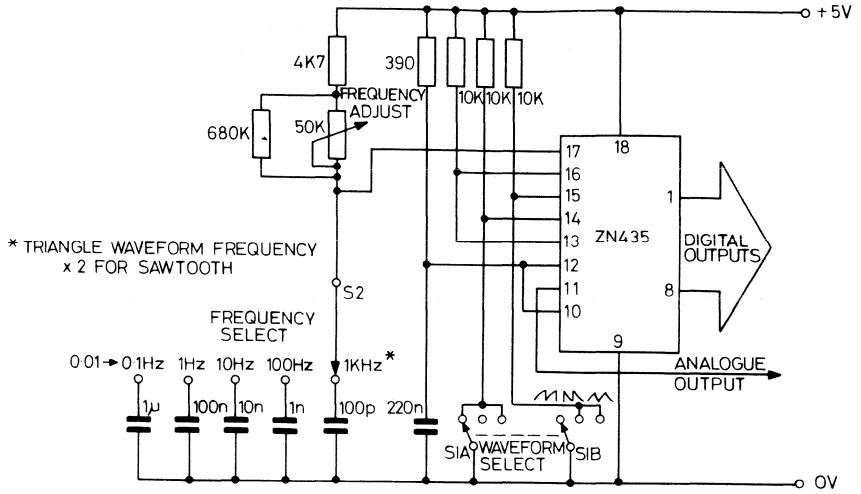


Fig. 8 WAVEFORM GENERATOR 6571

This will produce stable, linear, sawtooth and triangle waveforms.

RAMP AND COMPARE A TO D CONVERTER

A simple ramp and compare A to D converter can be constructed using the ZN435 and an external comparator, as shown in figure 9.

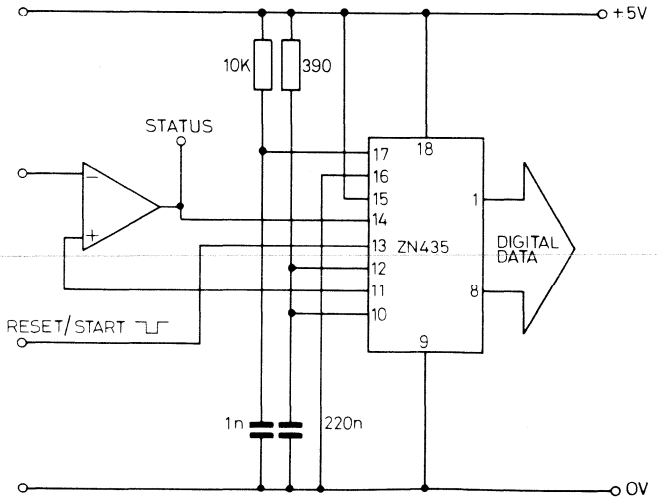


Fig. 9 RAMP AND COMPARE ADC 6572

The counter is set to count up from zero, producing a positive-going ramp at the analogue output. When the ramp voltage exceeds the analogue input the comparator output will go high, inhibiting the clock and stopping the counter. The converter can be reset and re-started by applying a low-going pulse to the reset input.

The basic analogue input range is $0-V_{REF}$, but other ranges can be accommodated by adding an attenuator to the comparator input. The comparator offset adjustment can be used for zero adjustment. Note that in this circuit the mode input is tied low to make the counter stop at full-scale. This prevents the counter cycling in the event of an overrange input.

TRACKING A TO D CONVERTER

The on-chip up-down counter allows the ZN435 to be configured very simply as a tracking A to D converter using an external comparator, as shown in figure 10.

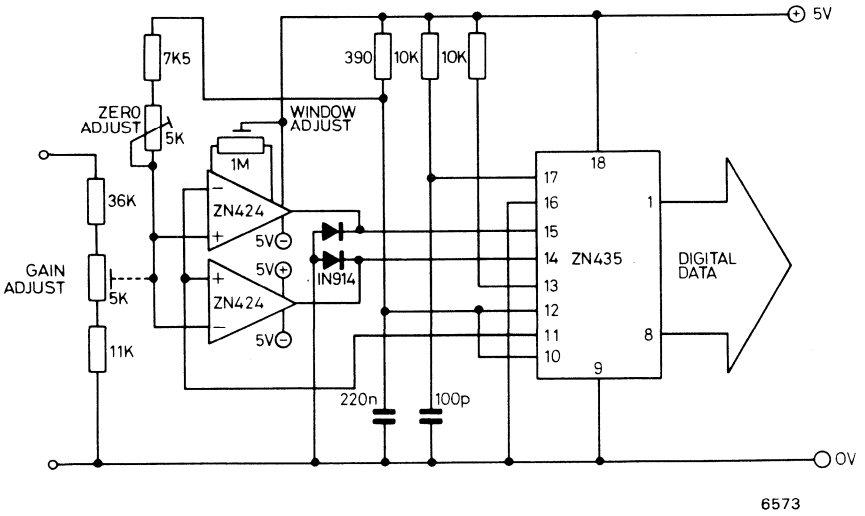


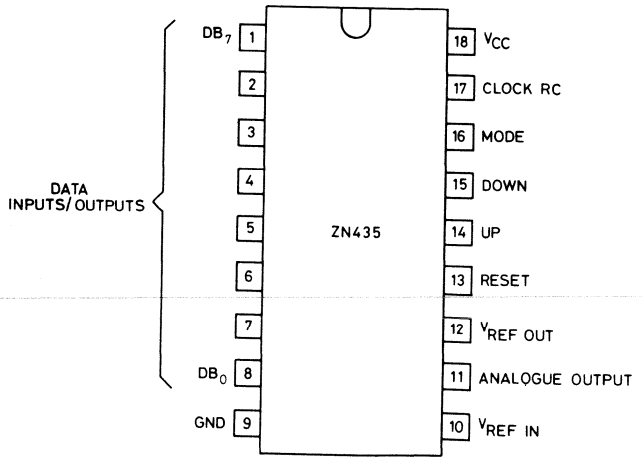
Fig. 10 TRACKING ADC

In this circuit two ZN424 op amps are used to make a window comparator. This has a deadband equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2.

Whenever the analogue voltage is above the threshold of A1 the counter will count up so that the DAC output increases to follow the analogue voltage. Whenever the analogue voltage is below the threshold of A2 the counter will count down to make the DAC follow the analogue voltage. When the analogue voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped.
The circuit here has an analogue input range of $\pm$10V. Other ranges may be accommodated by suitable choice of input resistors.

Note that in this circuit the mode input is tied low. This causes the counter to stop when full-scale or zero is reached, i.e. when the analogue input exceeds plus or minus full-scale. Without this feature the counter would simply cycle continuously.

PIN CONNECTIONS



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FERRANTI semiconductors

D-A CONVERTER

ZN436E/J

Low Cost 6 Bit Monolithic D to A Converter

FEATURES

- 6-bit Accuracy
- ZN436E Commercial Temp. Range 0°C to +70°C
- ZN436J Military Temp. Range −55°C to +125°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 μsec. Typical
- Designed for low-cost applications

DESCRIPTION

The ZN436 is a monolithic 6-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

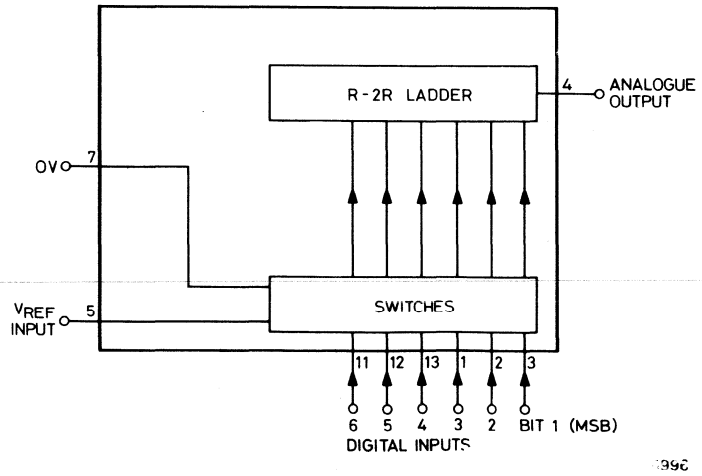


Fig. 1. SYSTEM DIAGRAM

ZN436E/J

INTRODUCTION

The ZN436 is a 6-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 6-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

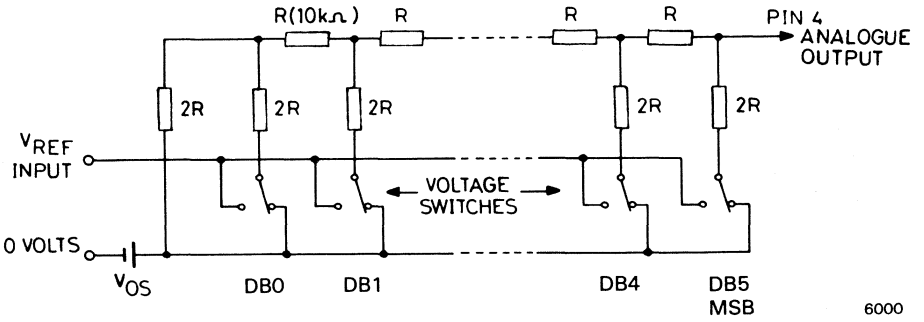


Fig. 2 THE R-2R LADDER NETWORK

Each 2R element is connected either to OV or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2 ohms.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN436 circuits and this is increased to ten for the ZN458 range.

ORDERING INFORMATION

Operating Temperature	6-bit accuracy			Package
0 to +70°C	ZN436E			Plastic
−55 to +125°C	ZN436J			Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts
Storage temperature range .. .. .. −55 to +125°C

CHARACTERISTICS (at T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution			–	–	bits	
Accuracy (useful resolution) ZN436J		6	–	–	bits	V_{REF} input = 2.0 to 3.0 volts
ZN436E		6	–	–	bits	
Non-linearity		–	–	±0.5	L.S.B.	*Note 1*
Differential non-linearity		–	±0.5	–	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		–	1.0	–	µs	1 L.S.B. step
Settling time ot 0.5 L.S.B.		–	2.0	–	µs	All bits ON to OFF or OFF to ON
Offset voltage ZN436J	V_{OS}	–	5.0	8.0	mV	All bits OFF *Note 1*
ZN436E		–	3.0	5.0	mV	
V_{OS} temperature coefficient		–	5	–	µV/°C	
Full scale output		2.510	2.520	2.530	volts	All bits ON Ext V_{REF} = 2.560V
Full scale temp. coefficient		–	3	–	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		–	7.5	–	ppm/°C	Relative to F.S.R.

CHARACTERISTICS (*continued*)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_O	–	10	–	kΩ	
External reference voltage		0	–	3.0	volts	
Supply voltage	V_{CC}	4.5	–	5.5	volts	
Supply current	I_S	–	5	9	mA	
High level input voltage	V_{IH}	2.0	–	–	volts	
Low level input voltage	V_{IL}	–	–	0.7	volts	
High level input current	V_{IH}	–	–	10	μA	V_{CC} = max., V_I = 2.4V
		–	–	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	–	–	−0.18	mA	V_{CC} = max., V_I = 0.3V

APPLICATIONS

1. 6-bit D to A Converter

The ZN436 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_O, will be less than 0.004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $>$ 650kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading −1 L.S.B.

iii. Repeat *i.* and *ii.*

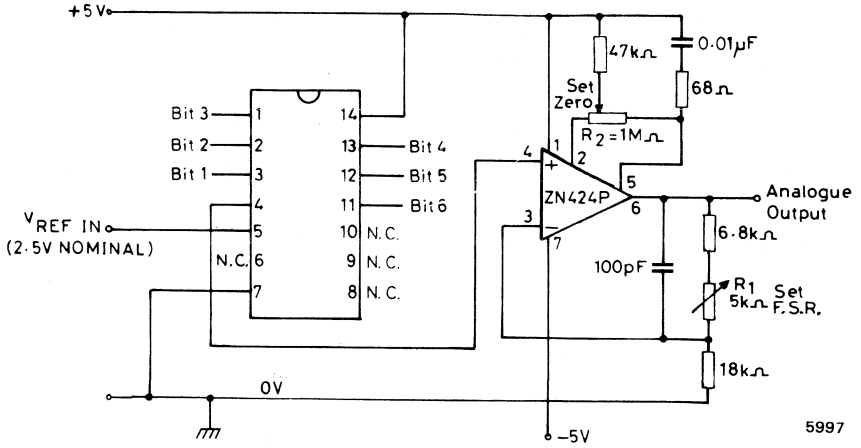


Fig. 3 6-BIT DIGITAL TO ANALOGUE CONVERTER

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).

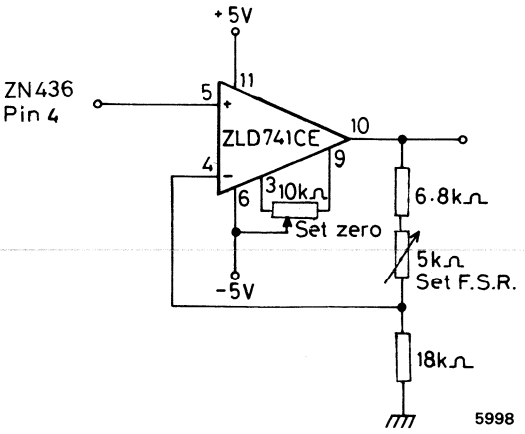
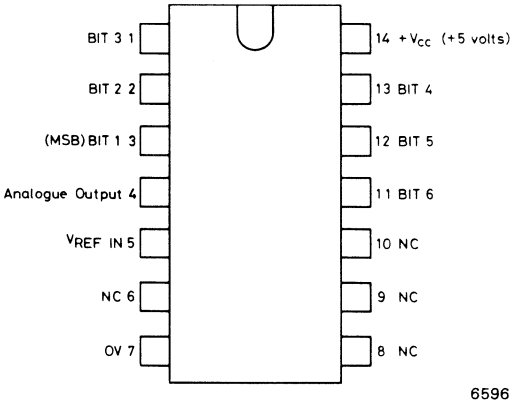


Fig. 4 THE ZLD741 AS OUTPUT BUFFER

PIN CONNECTIONS



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2. Analogue-to-Digital Converters

Contents

PRODUCT SELECTION GUIDE A TO D CONVERTERS

TYPE	USEFUL RESOLUTION (BITS)	CONVERSION TIME (μs)	CONVERSION METHOD	ON-CHIP REFERENCE	TEMPERATURE RANGE (°C)	FEATURES	PAGE
ZN425E Series	8-6	1000	Ramp and compare	+	0 to 70	Low cost dual purpose A/D-D/A converter	1-13
ZN425J	8	1000	Ramp and compare	+	-55 to +125	Low cost dual purpose A/D-D/A converter	1-13
ZN427E-8	8	10	Succ. Approx.	+	0 to 70	Microprocessor, TTL and CMOS compatible	2-17
ZN427-J8	8	10	Succ. Approx.	+	-55 to +125	Microprocessor, TTL and CMOS compatible	2-17
ZN432CJ Series	10-8	15	Succ. Approx.	+	0 to 70	Parallel/serial Output, TTL and CMOS compatible	2-35
ZN432J Series	10-8	15	Succ. Approx.	+	-55 to +125	Parallel/serial Output, TTL and CMOS compatible	2-35
ZN433CJ Series	10-8	1(ΔU_{in}=1LSB)	Tracking	+	0 to 70	Parallel/serial Output, TTL and CMOS compatible	2-53
ZN433J Series	10-8	1(ΔU_{in}=1LSB)	Tracking	+	-55 to +125	Parallel/serial Output, TTL and CMOS compatible	2-53
ZN435E	8	800	Ramp and compare	+	0 to 70	Dual purpose A/D-D/A converter (up/down counter)	1-47
ZN435J	8	800	Ramp and compare	+	-55 to +125	Dual purpose A/D-D/A converter (up/down counter)	1-47
ZN440J	6	0.06	Parallel (Flash)	-	0 to 70	Ultra fast monolithic Video A/D converter	2-63
ZN447-449E Series	8-6	9	Succ. Approx.	+	0 to 70	Clock generator, Microproc. TTL and CMOS compatible	2-75
ZN447-449J Series	8-6	9	Succ. Approx.	+	-55 to +125	Clock generator, Microproc. TTL and CMOS compatible	2-75
ZN450E, CJ	3 ½ Digit BCD	250ms	Charge balancing	+	0 to 70	Single chip DVM for direct LCD drive	2-97
ZNA116E,J	3 ½ Digit BCD	160ms	Dual Slope	-	0 to 70	DVM logic subsystem for LED MPX display	2-121
ZNA216,J	3 ¾ Digit BCD	160ms	Dual Slope	-	0 to 70	DVM logic subsystem for LED MPX display	2-135

2. ANALOGUE TO DIGITAL CONVERTERS

An analogue to digital Converter (ADC) is a device which converts an analogue input into a corresponding digital output code.

2.1 Ideal Output Characteristics

Assuming a unipolar input voltage and binary coded output, the transfer function of an ideal n-bit ADC is given by:

$$V_{FS}\ (B_1.2^{-1} + B_2.2^{-2} + \ldots . + B_n.2^{-n}) = V_{in} \pm \tfrac{1}{2}LSB$$

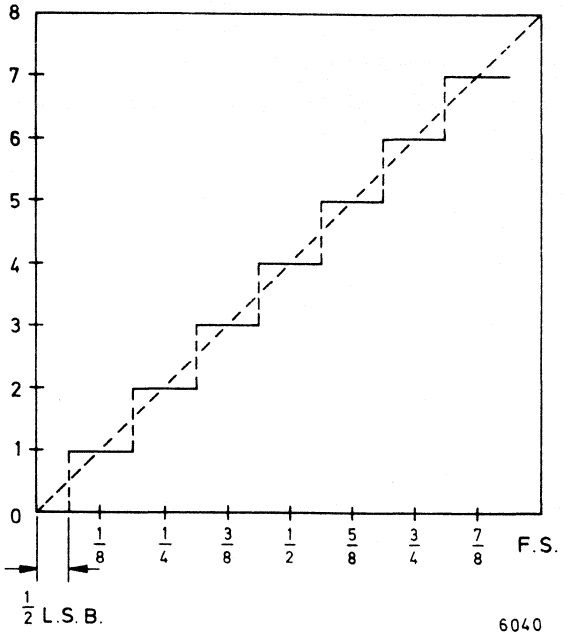


Fig. 9. Ideal 3-bit ADC Transfer Characteristic

The transfer function of an ideal 3-bit ADC is shown in figure 9. In this case there are 8 digital output codes corresponding to the 8 input codes of a DAC. However, unlike the analogue output of a DAC, the analogue input of an ADC can vary continuously, which means that each digital output code, with the exception of 0 and 7, exists over an analogue increment of 1 LSB. The zero of an ADC is usually trimmed so that the transitions between codes occur $\frac{1}{2}$ LSB on either side of the nominal analogue input for a particular code. For example, the nominal input for output code 2 is $\frac{1}{4}$ V_{FS}. The transition from 1 to 2 occurs at $\frac{3}{16}$ V_{FS} and the transition from 2 to 3 occurs at $\frac{5}{16}$ V_{FS}.

As with a DAC, an 'ideal' straight line may be drawn through the transfer characteristic of an ADC.

2.2 Practical A to D Conversion Methods

There are many methods of performing an analogue to digital conversion. Although not all of these methods are used in the current range of Ferranti A-D converters, they are all, nonetheless, mentioned for the sake of completeness.

2.2.1 Parallel (Flash) Conversion

In an n-bit parallel converter (Fig. 10) a resistor ladder is used to generate $2^n - 1$ voltage levels from 1 LSB to $(2^n - 1) \times$ LSB which are fed to the reference inputs of $2^n - 1$ voltage comparators. The analogue input signal is fed to the second input of each comparator, and is thus compared simultaneously with each of the $2^n - 1$ voltage levels. At the point in the comparator chain where the reference voltage exceeds the input voltage the comparator outputs will change over from low to high. The comparator outputs are encoded into whatever digital output coding is required.

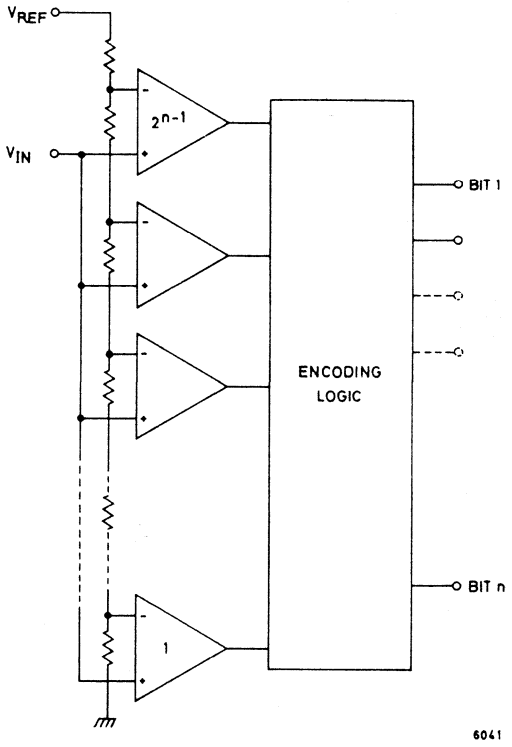


Fig. 10. Parallel A-D Converter

Since the only delays involved in the conversion are the propagation delay of one comparator plus the logic propagation delays, parallel converters are very fast and may perform in excess of 10 million conversions per second. However, due to the large number of comparators required (63 for a 6-bit converter, 255 for an 8-bit converter) they are expensive to produce. Applications include digital video systems, digital storage oscilloscopes and radar data processing.

2.2.2 Staircase and Comparator

In this type of ADC the input code of a DAC is incremented by a binary counter to give a staircase waveform, as shown in figure 11. This is compared with the analogue input and when the staircase exceeds the analogue voltage the comparator output changes state and stops the clock. The count reached by the binary counter is thus the ADC output code. This method of A to D conversion is relatively simple and cheap, but is also relatively slow, requiring $2^n - 1$ clock pulses for a full scale conversion, where n is the number of bits. This conversion method is used in the ZN425 series of dual-purpose D-A/A-D converters.

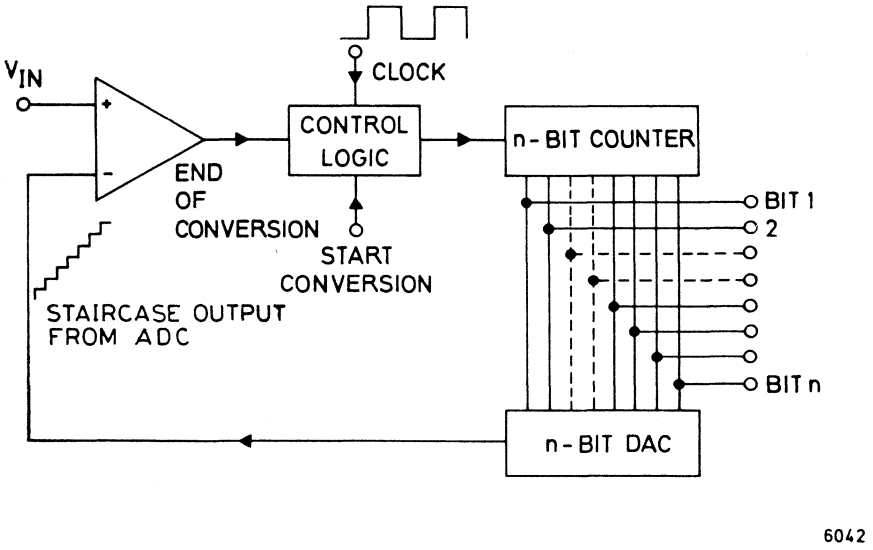


Fig. 11. Staircase (Ramp) and Compare ADC

A to D Converters

2.2.3 Tracking Converters

As its name implies, a tracking converter can follow changing analogue inputs. The principle operation is similar to that of the staircase and compare type of converter, but it uses an up/down counter and a window comparator, as shown in figure 12. When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input $\pm\frac{1}{2}$ LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in figure 13. A tracking converter has speed advantages over a staircase and compare type, since the counter of the latter type can only count up, and must therefore be reset between conversions. In the case of a tracking converter, once it has performed an initial conversion starting from zero, any subsequent conversions require only that number of clock pulses necessary to track any increase or decrease in input voltage.

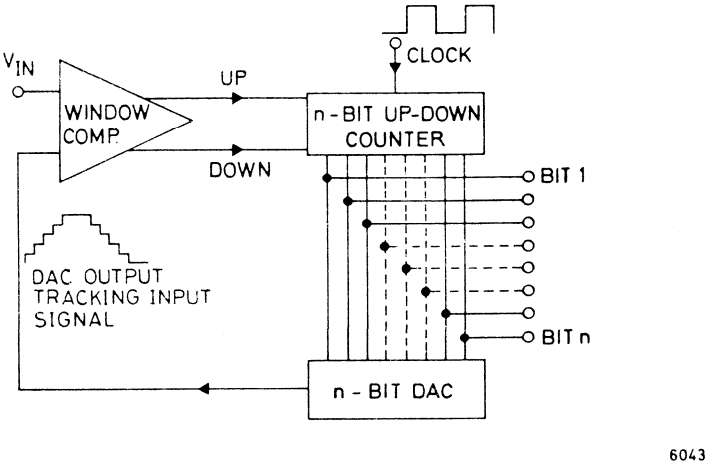


Fig. 12. Tracking ADC

As an extreme example consider an analogue input that changes from V_{FSO} to (V_{FSO} –1 LSB). The staircase and compare converter will require 2^n –1 clock pulses for the first conversion and 2^n –2 clock pulses for the second conversion. The tracking converter on the other hand, will require 2^n –1 clock pulses for the first conversion but only one clock pulse for the second conversion. This is illustrated in figure 14.

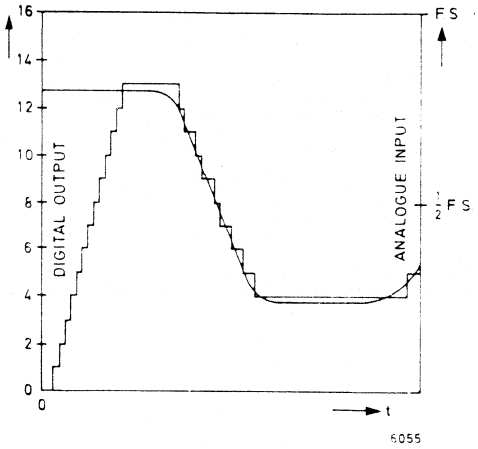


Fig. 13. Operation of Tracking ADC

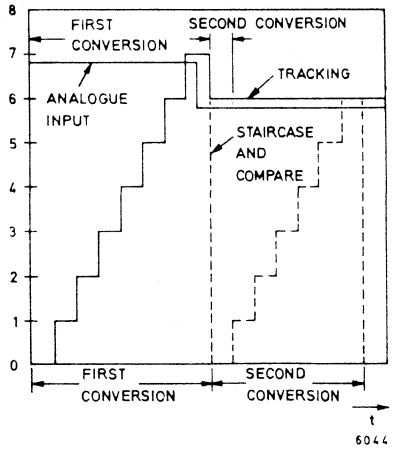


Fig. 14. Comparison of ramp and compare and tracking ADCs

In general it can be said that a tracking converter will follow signals whose rate of change is less than ± 1 LSB $\times$ clock frequency. If this condition is met there is no need to use a sample-and-hold circuit on the analogue input.

A tracking technique is used in the ZN433 series of converters.

2.2.4 Successive Approximation Converters

The operation of a staircase and compare ADC is analogous to weighing, say an 11 gramme weight, on a balance by adding one gramme weights until the scale tips, which is clearly a very slow method. A faster procedure, known as successive approximation, uses weights of 16, 8, 4, 2 and 1 grammes. The 16 gramme weight is tried first and is discarded because it tips the scale. The 8 gramme weight is tried next, and is left on the pan. Next the 4 gramme weight is tried and discarded, and the 2 and 1 gramme weights are tried and retained. The final result is the sum of the weights remaining on the scale pan, and the operation has taken 5 'cycles' as opposed to 11 'cycles' for the staircase and compare method.

The principle of a successive approximation ADC is identical. The MSB of a DAC is first set to '1' and the output is compared to the analogue input. If it is greater than the input the MSB is reset to '0', otherwise it is left at '1'. The next bit is then set to '1' and the DAC output is again compared to the analogue input. Again it is either reset or left at '1' depending on the result of the comparison. This procedure is repeated for every bit down to the LSB, and the final input code to the DAC is the output code of the ADC. A successive approximation cycle is illustrated in figure 15.

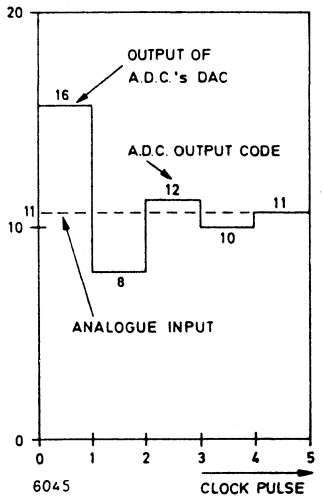


Fig. 15. Operation of a Successive Approximation ADC

Successive approximation is used in the ZN427 and ZN432 series of converters.

2.2.5 Dual Slope Converters

Dual slope integration is one of the slowest methods of A to D conversion, but it offers high resolution at a modest cost.

A block diagram of a dual-slope converter is shown in figure 16. It operates in the following manner: Switch S1 is closed by the control logic, S4 is opened and the input voltage is integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time the integrator output voltage, V_O, is $\frac{-V_{in}\, n\, T_c}{RC}$ where T_c is the clock period. This is shown in figure 17.

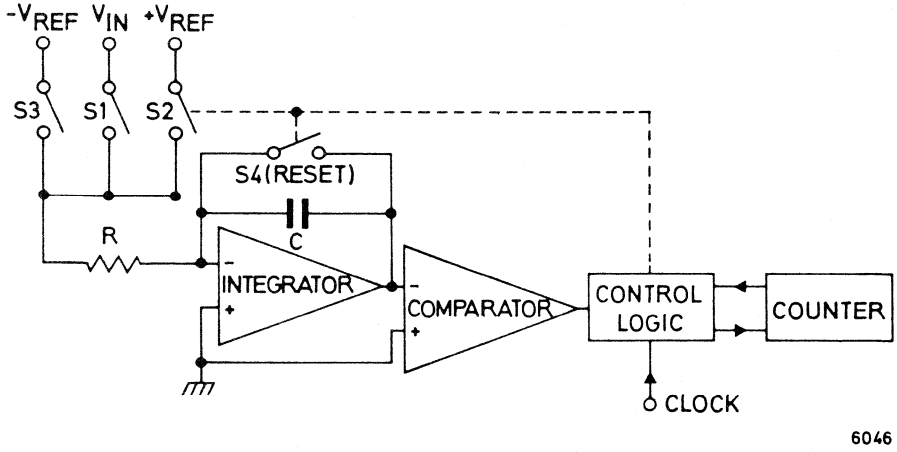


Fig. 16. Dual-Slope ADC

During this period the polarity of the input signal is detected by the comparator. At the end of the integration period S1 is opened and, depending on the polarity of V_{in}, either S2 or S3 is closed to connect the integrator to a reference voltage of opposite polarity to V_{in}. The counter is now allowed to count from zero until the integrator output reaches 0 volts, when the comparator output changes state and the counter is stopped. Since the integration is over the same voltage range (V_O), $V_O = \frac{-V_{REF} \times T_c}{RC}$, where x is the count

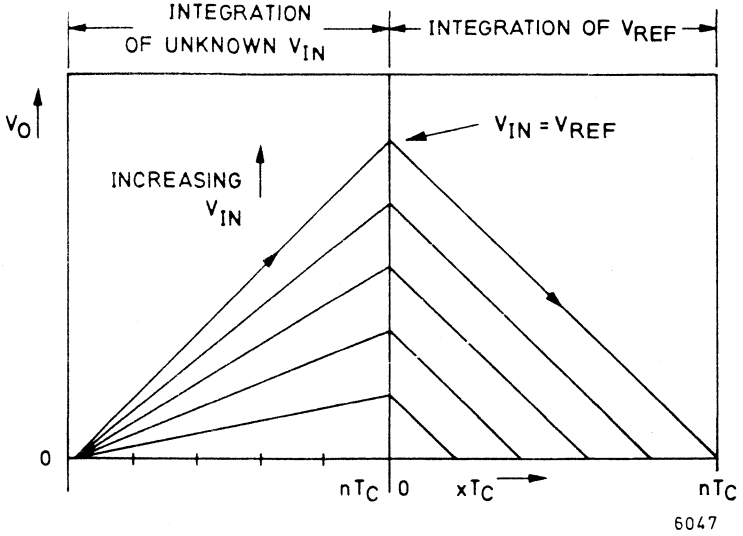


Fig. 17. Operation of Dual-Slope ADC

reached by the time the integrator output crosses zero. Thus

$$\frac{V_{in}.n\,T_c}{RC} = \frac{V_{REF}\,x\,T_c}{RC}$$

$$\text{or } x = \frac{V_{in}.n}{V_{REF}}$$

Since n and V_{REF} are both fixed the output count is proportional to the input voltage. Since both the first and second integrations occur under identical conditions the converter is unaffected by any long-term variations in T_c, R or C, as demonstrated by the disappearance of these terms from the final equation. The only factors affecting the accuracy of the converter are (1) the stability of V_{REF} (2) the stability of the 'on' resistance of S1 to S3 and (3) drift in the integrator and comparator op-amps. These effects can be minimised by careful design.

Dual slope converters are generally used where high resolution and low cost are more important than speed, for example in digital voltmeters.

The ZNA116 and ZNA216 are DVM logic subsystems containing the clock, counter and all control logic necessary for dual slope converter or DVM.

2.3 A to D Parameters and Definitions

2.3.1 A to D Converter Errors

Like DACs, practical ADCs are subject to a number of error sources, and since most ADCs contain a reference DAC, many of these error sources are the same for both types of converter.

2.3.2 Quantising Error (Uncertainty)

Quantising error is an ADC specification that has no counterpart in DAC specifications. For each input code of a DAC there is a unique analogue output level, but for any ADC output code there is a 1 LSB range of analogue input levels. It is thus not possible to tell from the output code the precise value of the analogue input level, there being a quantising error or uncertainty of $\pm\frac{1}{2}$ LSB. Since all ADCs have this inherent quantising error the parameter is frequently not quoted in specifications.

2.3.3 Missing Codes

Missing codes are perhaps best explained by considering the operation of a staircase and compare type 3-bit ADC which has a non-monotonic DAC, as shown in figure 18. The reference DAC exhibits non-monotonicity at input code 4, i.e. step 4 of the staircase decreases. There is thus no way in which the counter can be stopped at this code. If the analogue input is less than the DAC output for code 3 then the comparator will stop the counter before 4 is reached. If the analogue input is greater than output 3 it must also be greater than output 4, so the comparator will not change state at code 4.

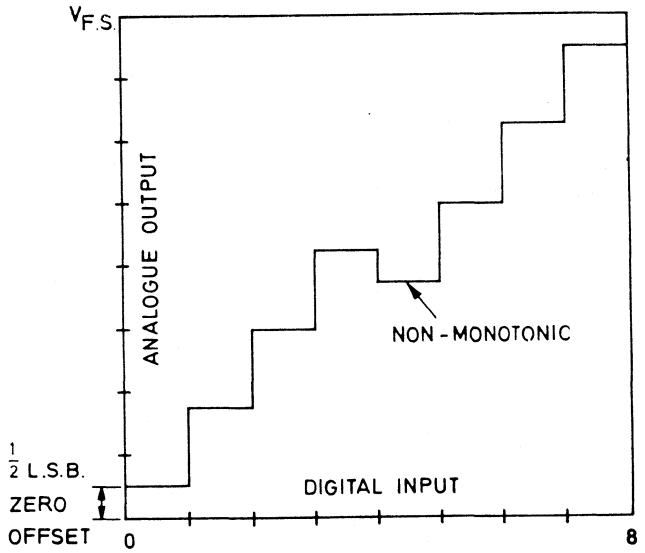


Fig. 18. Non-monotonic DAC used in an ADC

Output code 4 will thus never appear and is known as a 'missing' code. The transfer function of an ADC with a missing code is shown in figure 19.

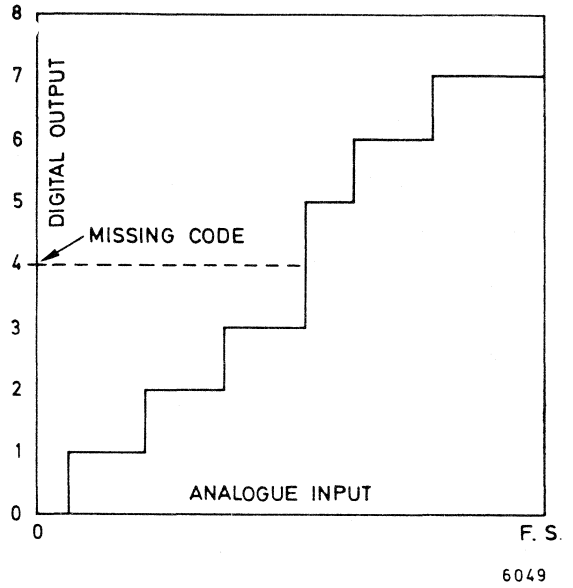


Fig. 19. ADC With Missing Code

2.3.4 Zero Transition

As explained earlier, the zero of an ADC is usually trimmed so that the output transition from 0 to 1 occurs at an input level corresponding to $\frac{1}{2}$ LSB, i.e. $\frac{1}{2}\frac{V_{FS}}{2^n}$. However, as supplied the reference DAC of an ADC I.C. will not have the $\frac{1}{2}$ LSB offset necessary to achieve this. The zero transition will thus occur at 1 LSB plus the DAC zero error, plus the comparator offset voltage. These three parameters are frequently lumped together as the (untrimmed) zero transition of the ADC.

2.3.5 Gain Error

This is the difference between the slope of a line drawn between the actual zero and full scale transition points and that of a line drawn through the ideal transition points.

2.3.6 Non-linearity (Linearity Error)

Non-linearity is the maximum amount by which any actual transition points deviates from the corresponding ideal transition point. It is specified as a percentage of full-scale or a fraction of an LSB. A linearity error of less than $\pm\frac{1}{2}$ LSB assures no missing codes.

2.3.7 Differential Non-linearity

This is the maximum difference between any 1 LSB increment of the analogue input and the ideal size of an LSB increment $\frac{V_{FS}}{2^n}$. Differential non-linearity of less than 1 LSB guarantees no missing codes.

2.3.8 Resolution

The resolution of an ADC is simply the number of bit outputs that the converter possesses. As with a DAC, resolution implies nothing about the accuracy of a device.

2.3.9 Useful Resolution

Useful resolution is the resolution (number of bits) at which an ADC has no missing codes, which for Ferranti ADCs is guaranteed over the operating temperature range. As with DACs, an n-bit ADC may have a useful resolution less than n bits, for reasons previously explained.

2.3.10 Conversion Time

The time taken for an ADC to perform a complete conversion is known as the conversion time. For successive approximation converters conversion time is fixed by the number of bits and the clock frequency. However, for other types, conversion time may vary with input voltage. For example, a ramp and compare ADC requires $2^n - 1$ clock pulses for a full scale conversion but only one clock pulse for a one bit conversion. It is thus important to check exactly what is being specified.

2.4 Bipolar Operation

As with a DAC, an ADC may be used for bipolar operation. Taking the ZN427 as an example the input is offset by $\frac{+V_{REF}}{2}$ so that the input voltage presented to the ADC is always positive, even with negative input voltages down to $\frac{-V_{REF}}{2}$. The principle of offsetting an ADC input is illustrated in figure 20, whilst the transfer function of a 3 bit bipolar ADC is shown in figure 21. In this case the **output** coding is known as offset binary.

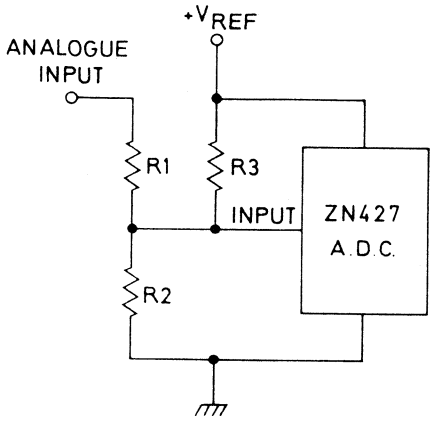


Fig. 20. Bipolar Operation of an ADC

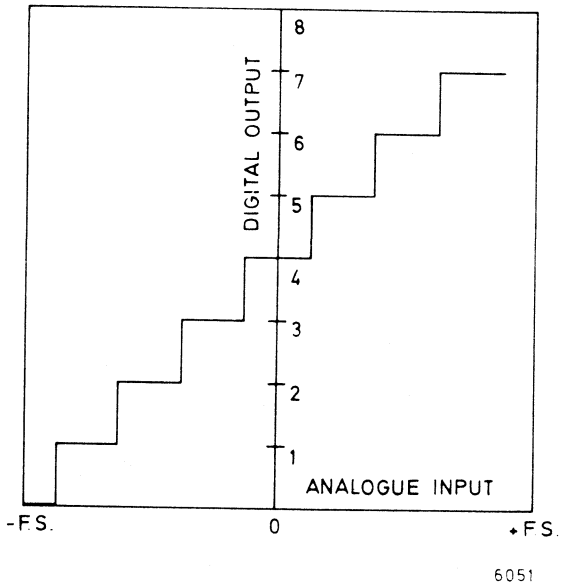


Fig. 21. Bipolar Transfer Characteristic of an ADC

FERRANTI semiconductors

A-D CONVERTER

ZN427E-8
ZN427J-8

Microprocessor Compatible 8 Bit Successive Approximation A - D Converter

FEATURES

- Easy interfacing to microprocessors, or operates as a 'stand-alone' converter
- Fast: 10 μs conversion time guaranteed
- No missing codes over operating temperature range
- Data outputs 3-state TTL compatible, other logic inputs and outputs TTL and CMOS compatible
- Choice of on-chip or external voltage reference
- Ratiometric operation
- Unipolar and bipolar input ranges
- Complementary to ZN428 DAC
- Choice of commercial or military temperature range

DESCRIPTION

The ZN427 is an 8-bit successive approximation converter with 3-state outputs to permit easy interfacing to a common data bus. The IC contains a voltage switching DAC, a fast comparator, successive approximation logic and a 2.56 volt precision band-gap reference, the use of which is pin-optional to retain flexibility. An external fixed or varying reference may therefore be substituted, thus allowing ratiometric operation.

Only passive external components are required for operation of the converter.

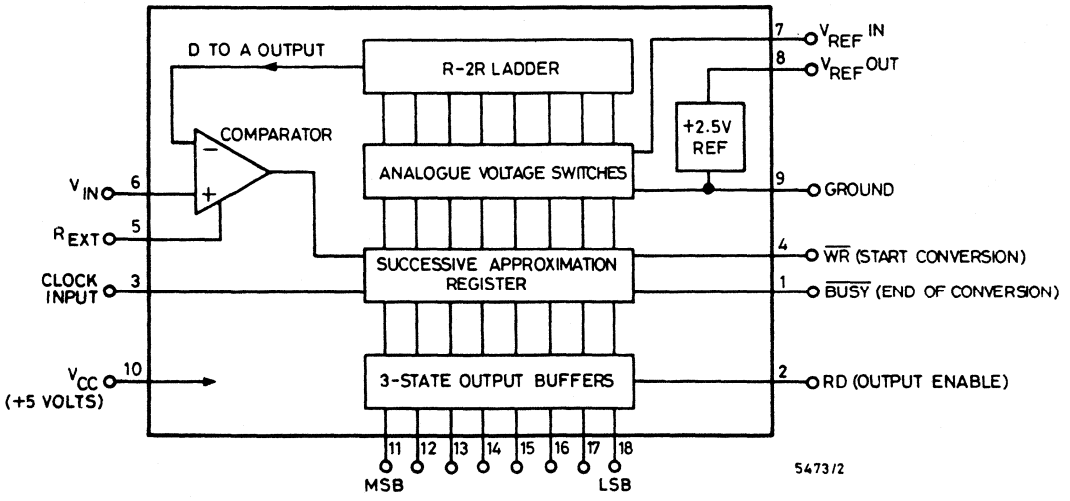


Fig. 1 – System Diagram

ZN427E-8/J-8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7.0 volts
Max. Voltage, Logic and V_{REF} inputs .. .. V_{CC}
Operating temperature range .. .. 0°C to +70°C (ZN427E-8)
–55°C to +125°C (ZN427J-8)
Storage temperature range .. .. –55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
CONVERTER					
Resolution	8	—	—	Bits	
Linearity Error	—	—	±0.5	LSB	
Differential Non-Linearity	—	±0.5	—	LSB	
Linearity Error T.C.	—	±3	—	ppm/°C	
Differential Non-Linearity T.C.	—	±6	—	ppm/°C	
Full Scale (Gain) T.C.	—	±2.5	—	ppm/°C	External Ref. 2.5V
Zero T.C.	—	±8	—	µV/°C	
Zero Transition 00000000 to 00000001	12	15	18	mV	$V_{REF\,IN}$ = 2.560V
F.S. Transition 11111110 to 11111111	2.545	2.550	2.555	V	$V_{REF\,IN}$ = 2.560V
Conversion Time	—	—	10	µs	See Note 1
External Reference Voltage	1.5	—	3.0	V	
Supply Voltage (V_{CC})	4.5	—	5.5	V	
Supply Current	—	25	40	mA	
Power Consumption	—	125	—	mW	
COMPARATOR					
Input Current	—	1	—	µA	V_{IN} = 3V, R_{EXT} = 82kΩ
Input Resistance	—	100	—	kΩ	V_- = –5V
Tail Current, I_{EXT}	25	—	150	µA	
Negative Supply, V–	–3.0	—	–30.0	V	See COMPARATOR
Input Voltage	–0.5	—	3.5	V	
INTERNAL VOLTAGE REFERENCE					
Output Voltage	2.475	2.560	2.625	V	R_{REF} = 390Ω C_{REF} = 4 µ7
Slope Resistance	—	0.5	2	Ω	
V_{REF} Temperature Coefficient	—	50	—	ppm/°C	
Reference Current	4	—	15	mA	See REFERENCE

ELECTRICAL CHARACTERISTICS (continued)

	Min.	Typ.	Max.	Units	Conditions
LOGIC					
(over operating temp.)					
High Level Input Voltage V_{IH}	2	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current,	—	—	50	μA	V_{IN} = 5.5V, V_{CC} = max.
$\overline{WR}$ and RD inputs I_{IH}	—	—	15	μA	V_{IN} = 2.4V, V_{CC} = max.
High Level Input Current,	—	—	100	μA	V_{IN} = 5.5V, V_{CC} = max.
Clock Input I_{IH}	—	—	30	μA	V_{IN} = 2.4V, V_{CC} = max.
Low Level Input Current I_{IL}	—	—	−5	μA	V_{IN} = 0.4V, V_{CC} = max.
High Level Output Current I_{OL}	—	—	−100	μA	
Low Level Output Current I_{OL}	—	—	1.6	mA	
High Level Output Voltage V_{OH}	2.4	—	—	V	I_{OH} = max., V_{CC} = min.
Low Level Output Voltage V_{OL}	—	—	0.4	V	I_{OL} = max., V_{CC} = min.
Disabled Output Leakage	—	—	2	μA	V_O = 2.4V
Input Clamp Diode Voltage	—	—	−1.5	V	
Read Input to Data Output	—	—	250	ns	See Fig. 8
Enable/Disable Delay Time t_{RD}	—	180	250	ns	
Start Pulse Width t_{WR}	250	160	—	ns	See Fig. 8
$\overline{WR}$ to $\overline{BUSY}$ Propagation	—	—	250	ns	
Delay t_{BD}	—	—	—		
Clock Pulse Width	500	—	—	ns	
Maximum Clock Frequency	900	1000	—	kHz	See Note 1

Note 1 : A 900 kHz clock gives a conversion time of 10μs (9 clock periods).

GENERAL CIRCUIT OPERATION

The ZN427 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF}/2$ from the DAC. This is compared to the input voltage V_{IN} ; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the ninth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held low to keep the 3-state buffers in their high impedance state. Data can be read out by taking RD high, thus enabling the 3-state outputs. Readout is non-destructive. The $\overline{BUSY}$ output may be tied to the RD input to automatically enable the outputs when the data is valid.

For reliable operation of the converter the start pulse applied to the $\overline{WR}$ input must meet certain timing criteria with respect to the converter clock. These are detailed in the timing diagram of figure 2.

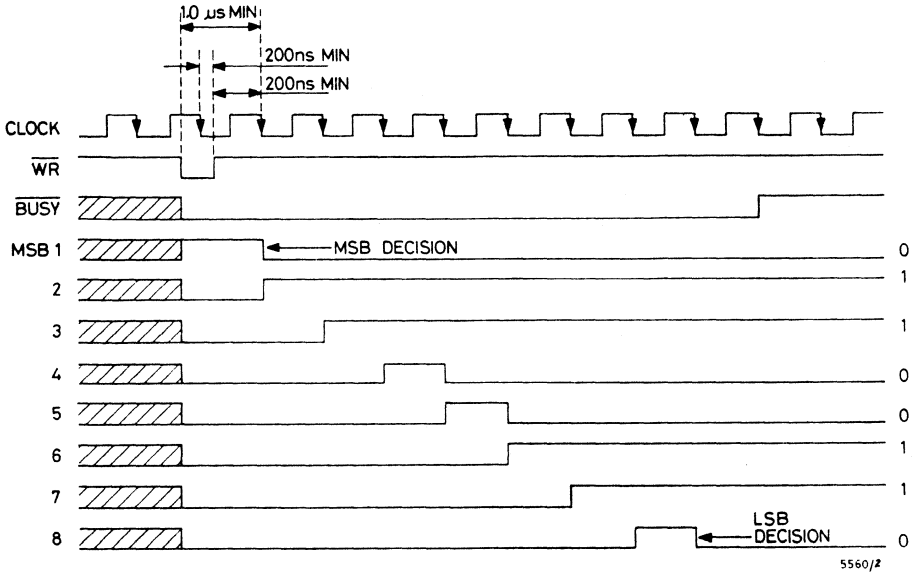


Fig. 2 Timing Diagram

NOTES ON TIMING DIAGRAM

1. A conversion sequence is shown for the digital word 01100110. For clarity the 3-state outputs are shown as being enabled during the conversion, but normal practice would be to disable them until the conversion was complete.

2. The $\overline{BUSY}$ output goes low during a conversion. When $\overline{BUSY}$ goes high at the end of a conversion the output data is valid. In a microprocessor system the $\overline{BUSY}$ output can be used to generate an interrupt request when the conversion is complete.

3. In the timing diagram cross hatching indicates a 'don't care' condition.

4. The start pulse operates as an asynchronous (independent of clock) reset that sets the MSB output to 1 and sets all other outputs and the end of conversion flag to 0. This resetting occurs on the low-going edge of the start pulse and as long as $\overline{WR}$ is low the converter is inhibited. Conversion commences on the first active (negative going) clock edge after the $\overline{WR}$ input has gone high again, when the MSB decision is made. A number of timing constraints thus apply to the start pulse.

(a) The minimum duration of the start pulse is 250ns, to allow reliable resetting of the converter logic circuits.

(b) There is no limit to the maximum duration of the start pulse.

(c) To allow the MSB to settle at least 1.5μs must elapse between the negative going edge of the start pulse and the first active clock edge that initiates the MSB desicion.

(d) To ensure reliable clocking the positive-going edge of the start pulse should not occur within 200 ns of an active (negative-going) clock edge. The ideal place for the positive-going edge of the start pulse is coincident with a positive-going clock edge. As a special case of the above conditions the start pulse may be synchronous with a negative-going clock pulse.

PRACTICAL CLOCK AND SYNCHRONISING CIRCUITS

The actual method of generating the clock signal and synchronising it to the start conversion pulse (or vice versa) will depend on the system in which the ZN427 is incorporated.

When used with a microprocessor the ZN427 can be treated as RAM and can be assigned a memory address using an address decoder. If the μP clock is used to drive the ZN427 and the μP write pulse meets the ZN427 timing criteria with respect to the μP clock then generating the start pulse is simply a matter of gating the decoded address with the microprocessor write pulse. Whilst the conversion is being performed the microprocessor can perform other instructions or No operation (NOP). When the conversion is complete the outputs can be enabled onto the data bus by gating the decoded address with the read pulse. A timing diagram for this sequence of operations is given in figure 3.

An advantage of using the microprocessor clock is that the conversion time is known precisely in terms of machine cycles. The data outputs may therefore be read after a fixed delay of at least nine clock cycles after the end of the $\overline{WR}$ pulse, when the conversion will be complete.

Alternatively the read operation may be initiated by using the $\overline{BUSY}$ output to generate an interrupt request.

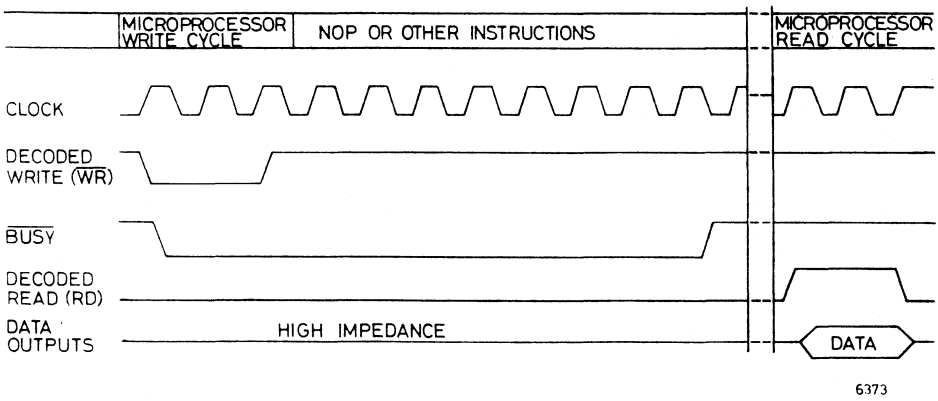


Fig. 3 Typical Timing Diagram Using μP clock and Write Pulse

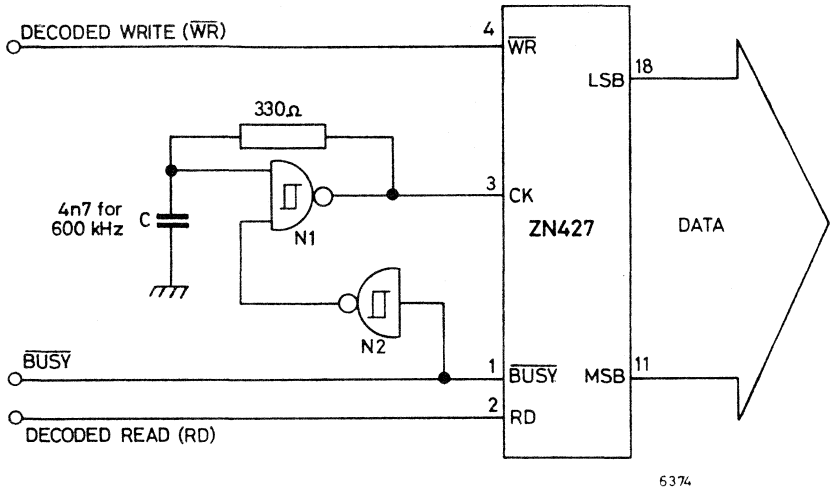
In some systems, for example single-chip microcomputers such as the 8048, this simple method may not be feasible for one or more of the following reasons:

(a) The MPU clock is not available externally.

(b) The clock frequency is too high.

(c) The write pulse timing criteria make it unsuitable for direct use as a start conversion pulse.

If any of these conditions apply then the self-synchronising clock circuit of figure 4a is recommended.



N1 N2 = ZN7413 or ½ 74132 Schmitt Trigger

$$f_{CK} = \frac{1}{360.C} \text{ (Hz, F)}$$

Fig. 4a. Self-Synchronising Clock Circuit

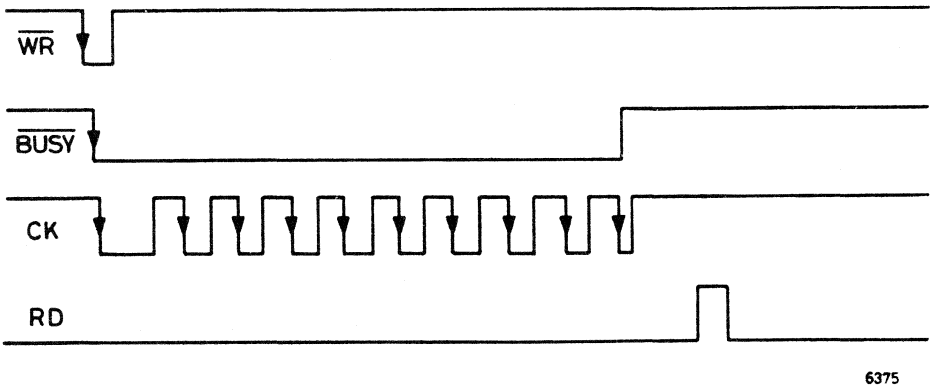


Fig 4b. Timing Diagram For Circuit of Figure 4a.

N1 is connected as an astable multivibrator which, when the $\overline{BUSY}$ output is high, is inhibited by the output of N2 holding one of its inputs low. The start conversion pulse resets the $\overline{BUSY}$ flag and N1 begins to oscillate. When the conversion is completed $\overline{BUSY}$ goes high and the clock is inhibited.

Since the start pulse starts the clock it may occur at any time. The only constraints on the start pulse are that it must be longer than 250 ns but at least 200 ns shorter than the first clock pulse. The first clock pulse is in fact longer than the rest since C1 starts from a fully charged condition whereas on subsequent cycles it charges between the upper and lower thresholds (V_{T+} and V_{T-}) of the Schmitt trigger.

LOGIC INPUTS AND OUTPUTS

The logic inputs of the ZN427 utilise the emitter-follower configuration shown in fig. 5. This gives extremely low input currents for CMOS as well as TTL compatibility.

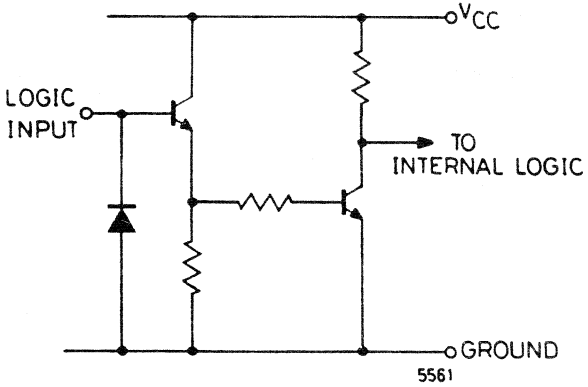
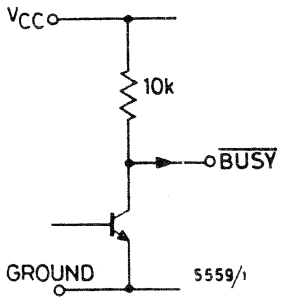


Fig. 5. Equivalent Circuit of all Inputs

The $\overline{BUSY}$ output, shown in figure 6, utilises a passive pullup for CMOS/TTL compatibility



The data outputs have 3-state buffers, an equivalent circuit of which is shown in figure 7. Whilst the RD input is low both output transistors are turned off and the output is in a high impedance state. When RD is high the data output will assume the appropriate logic state (0 or 1).

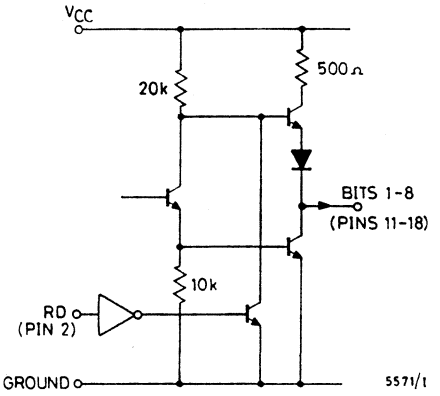


Fig. 7. Equivalent Circuit of Data Outputs

A test circuit and timing diagram for the output enable/disable delays are given in figure 8.

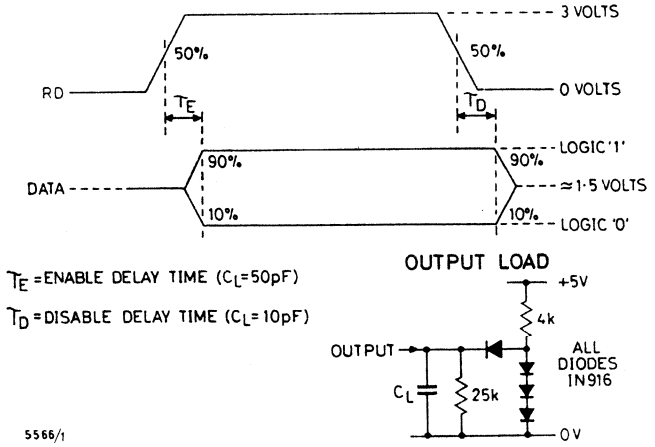


Fig. 8. Output Enable/Disable Waveforms

ANALOGUE CIRCUITS

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in figure 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D to A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 2 mV for the ZN427E-8 (4 mV, ZN427J-8). This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8 μV/°C) the effect on accuracy will be negligible.

The D to A output range can be considered to be 0-$V_{REF\ IN}$ through an output resistance R (4kΩ)

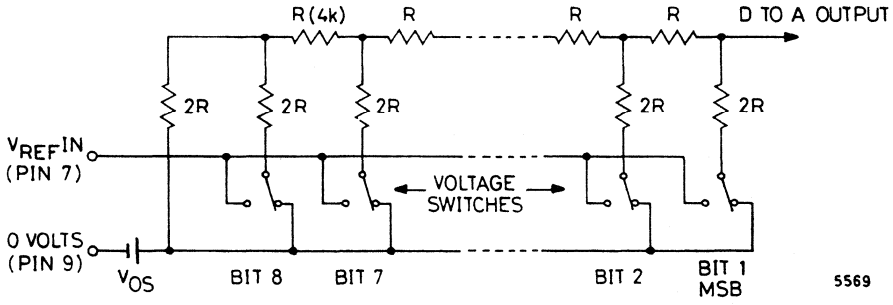


Fig. 9. R2-R Ladder Network

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 10). A resistor (R_{REF}) should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0 -2.5) /0.39 = 6.4mA. A stabilising/decoupling capacitor, C_{REF} (4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (Pin 8) is connected to $V_{REF\ IN}$ (Pin 7).

Up to five ZN427's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

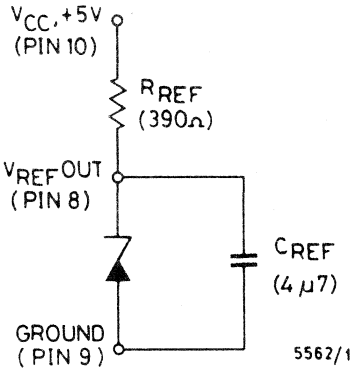


Fig. 10 Internal Voltage Reference

(b) External Reference

If required an external reference voltage in the range +1.5 to +3.0 volts may be connected to $V_{REF\,IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$ where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 volts to +3.0 volts. The ZN427 will operate if $V_{REF\,IN}$ is less than +1.5 volts but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 11.

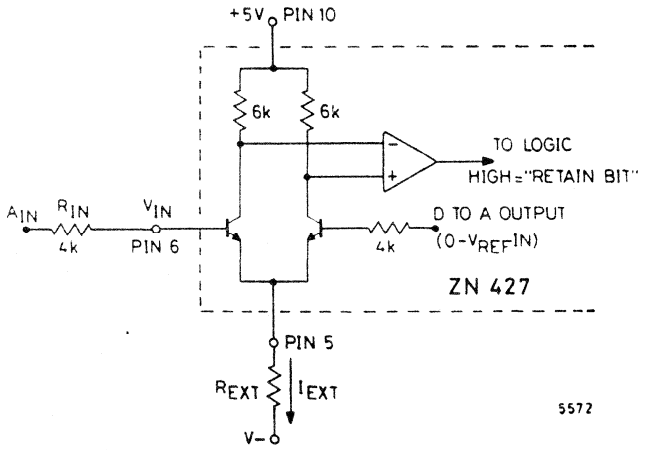


Fig. 11 Comparator Equivalent Circuit

The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V–.

This arrangement allows the ZN427 to work with any negative supply in the range –3 to –30 volts. The ZN427 is designed to be insensitive to changes in I_{EXT} from 25μA to 150μA. The suggested nominal value of I_{EXT} is 65μA and a suitable value for R_{EXT} is given by $R_{EXT} = |V-|15k\Omega$.

V– (Volts)	R_{EXT} (±10%)
–3	47kΩ
–5	82kΩ
–10	150kΩ
–12	180kΩ
–15	220kΩ
–20	330kΩ
–25	390kΩ
–30	470kΩ

The output from the D to A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analogue input to be converted could be connected directly to the other comparator input (V_{IN}, Pin 6) but for optimum stability with temperature the analogue input should be applied through a source resistance (R_{IN} = 4kΩ) to match the ladder resistance.

ANALOGUE INPUT RANGES

The basic connection of the ZN427 shown in fig. 12 has an analogue input range 0 to $V_{REF\,IN}$, which, in some applications, may be made available from previous signal conditioning/scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by offsetting the analogue input range so that the comparator always sees a positive input voltage.

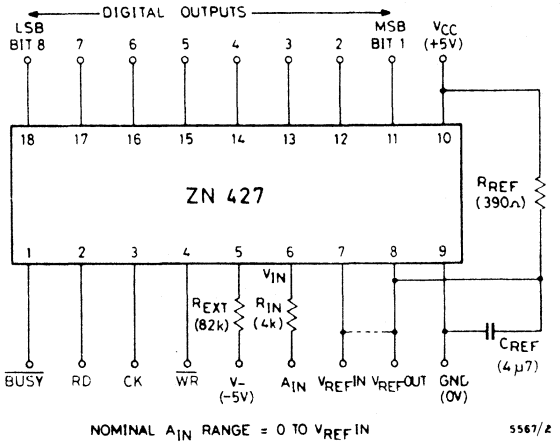


Fig. 12. External Components for Basic Operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in figure 13.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input(A_{IN}) is at full scale. The resulting full scale range is given by:

$$A_{IN}\ FS = (1+\frac{R1}{R2}),\ V_{REF\ IN} = G.\ V_{REF\ IN}.$$

To match the ladder resistance R1//R2 ($\approx R_{IN}$) = 4kΩ.

The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ kΩ, $R_2 = \frac{4G}{G-1}$ kΩ.

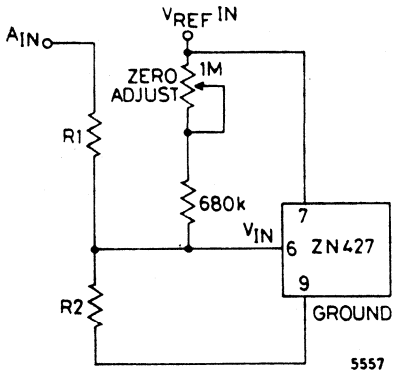


Fig. 13 Unipolar Operation - General Connection

Using these relationhips a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Input Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

ZERO ADJUSTMENTS

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to +1½ LSB with a 2.56 volt reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of $+\frac{1}{2}$ LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than $1\frac{1}{2}$ times $V_{REF\,IN}$.

Practical circuit values for +5V and +10V input ranges are given in fig. 14, which incorporate both zero and gain adjustments.

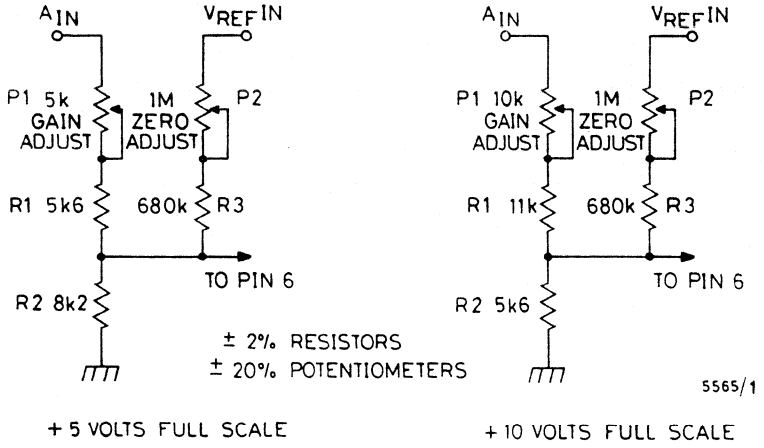


Fig. 14. Unipolar Operation - Component Values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full scale minus $1\frac{1}{2}$ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply $\frac{1}{2}$ LSB to A_{IN} and adjust zero until Bit 8 just flickers between 0 and 1 with all other bits at 0.

UNIPOLAR SETTING-UP POINTS

Input Range, +FS	$\frac{1}{2}$ LSB	FS $-1\frac{1}{2}$ LSB
+5V	9.8 mV	4.9707 volts
+10V	19.5 mV	9.9414 volts

$$1\ \text{LSB} = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Binary)
FS –1 LSB	11111111
FS –2 LSB	11111110
$\frac{3}{4}$ FS	11000000
$\frac{1}{2}$ FS + 1 LSB	10000001
$\frac{1}{2}$ FS	10000000
$\frac{1}{2}$ FS – 1 LSB	01111111
$\frac{1}{4}$ FS	01000000
1 LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN427 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 15).

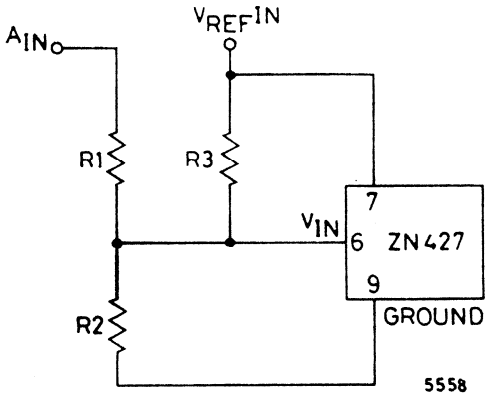


Fig. 15. Bipolar Operation - General Connection

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance $R_1/R_2/R_3$ $(=R_{IN}) = 4k\Omega$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8\ Gk\Omega$, $R_2 = 8G/(G - 1)k\Omega$, $R_3 = 8k\Omega$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for $\pm 5V$ and $\pm 10V$ input ranges are given in the following table.

Input Range	G	R_1	R_2	R_3
±5V	2	16 kΩ	16 kΩ	8 kΩ
±10V	4	32 kΩ	10.66 kΩ	8 kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 16.

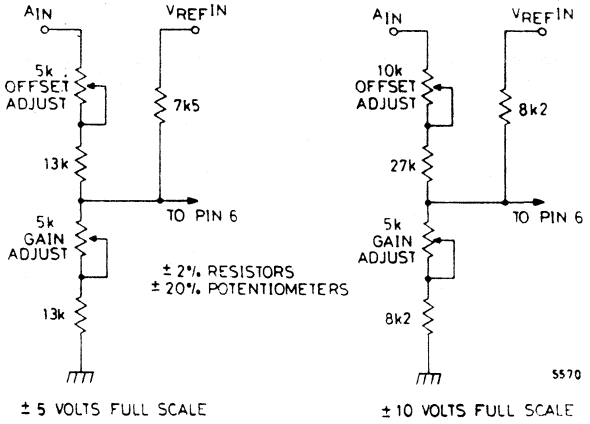


Fig. 16 Bipolar Operation - Component Values

Note that in the ±5V case R_3 has been chosen as 7.5 kΩ (instead of 8.2 kΩ) to obtain a more symmetrical range of adjustment using standard potentometers.

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply $-(FS - \frac{1}{2}\ LSB)$ to A_{IN} and adjust offset until the Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply $+(FS - 1\frac{1}{2}\ LSB)$ to A_{IN} and adjust gain until Bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

BIPOLAR SETTING-UP POINTS

Input Range, ±FS	$-(FS - \frac{1}{2}\ LSB)$	$+(FS - 1\frac{1}{2}\ LSB)$
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

$$1\ LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Offset Binary)
+(FS – 1 LSB)	11111111
+(FS – 2 LSB)	11111110
+½ FS	11000000
+1 LSB	10000001
0	10000000
–1 LSB	01111111
–½ FS	01000000
–(FS – 1 LSB)	00000001
–FS	00000000

SINGLE 5 VOLT SUPPLY RAIL OPERATION

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig. 17 works with any clock frequency from 10 kHz to 1 MHz and can supply up to five ZN427s.

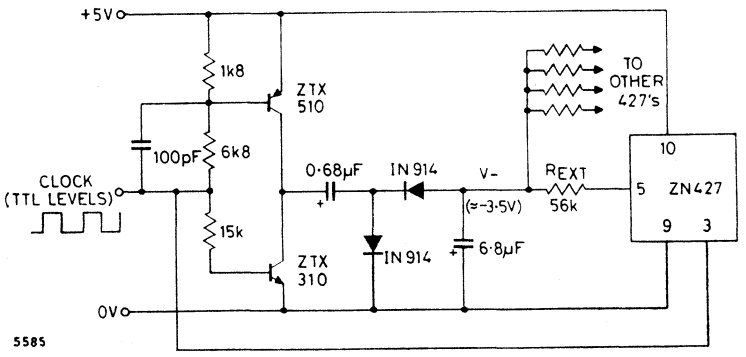
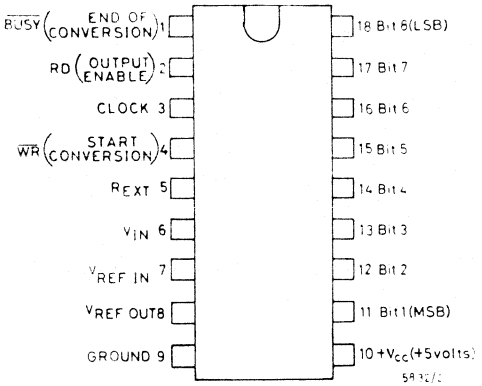
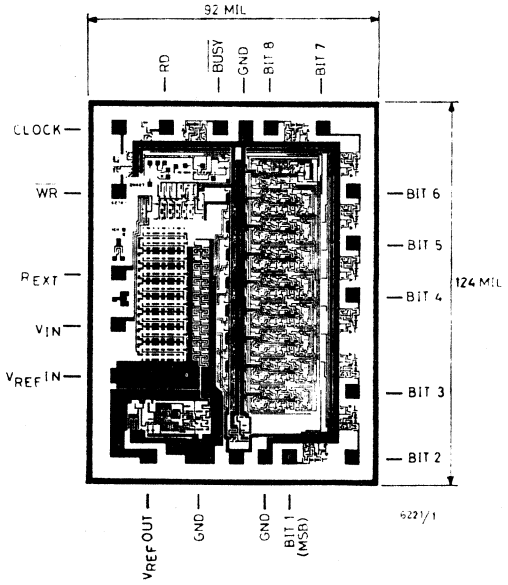


Fig. 17. Single 5 Volt Supply Operation

Pin Connections





Chip Dimensions and Layout

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	OPERATING TEMP. RANGE
ZN427E-8	Plastic	0°C to +70°C
ZN427J-8	Ceramic	−55°C to +125°C

FERRANTI semiconductors

A to D CONVERTER

ZN432 Series

10-Bit Successive Approximation Monolithic A/D Converter

FEATURES

- 10, 9 and 8-Bit Accuracies
- 3 Operating Temperature Ranges
- 20 μs Conversion Time Guaranteed
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction

DESCRIPTION

The ZN432 range of successive approximation analogue to digital converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to provide guaranteed monotonicity over the operating temperature range.

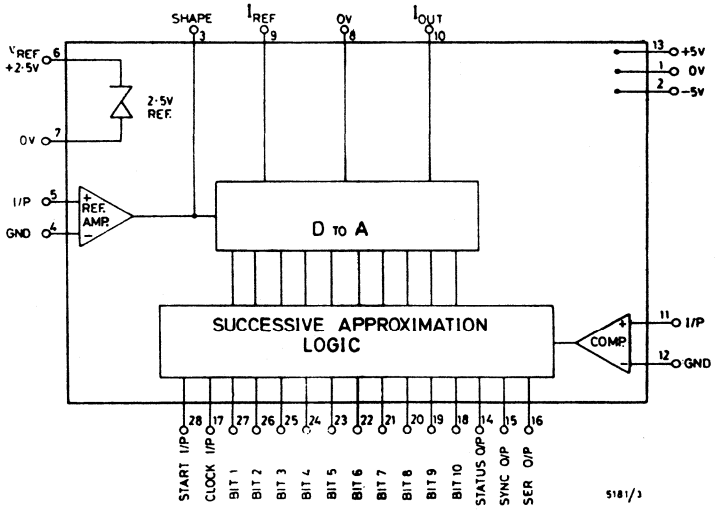


Fig. 1 – INTEGRATED CIRCUIT BLOCK DIAGRAM

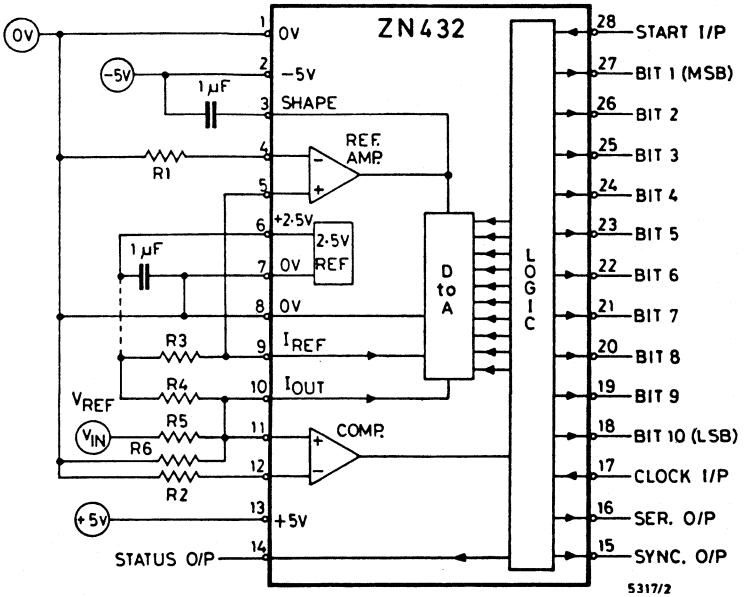


Fig. 2—TYPICAL EXTERNAL COMPONENTS

ORDERING INFORMATION

Operating Temperature	10-bit accuracy	9-bit accuracy	8-bit accuracy	Package
–55 to +125°C	ZN432J-10	ZN432J-9	ZN432J-8	Ceramic
–40 to +85°C	ZN432BJ-10	ZN432BJ-9	ZN432BJ-8	Ceramic
0 to +70°C	ZN432CJ-10	ZN432CJ-9	ZN432CJ-8	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply Voltages .. .. ±7 volts
Logic Input Voltage .. .. .. $+V_{CC}$ and 0V
Storage Temperature Range .. –55°C to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
CONVERTER Accuracy (useful resolution)	ZN432J-10, ZN432BJ-10, ZN432CJ-10	10			10		Bits	Note 1
	ZN432J-9, ZN432BJ-9, ZN432CJ-9	9			9		Bits	
	ZN432J-8, ZN432BJ-8, ZN432CJ-8	8			8		Bits	
Non-linearity	All types			±0.5			LSB	
Differential non-linearity	All types		±0.5				LSB	Note 1
Operating temp. range	ZN432J-10, ZN432J-9, ZN432J-8				–55	+125	°C	
	ZN432BJ-10, ZN432BJ-9, ZN432BJ-8				–40	+85	°C	
	ZN432CJ-10, ZN432CJ-9, ZN432CJ-8				0	+70	°C	
D to A reference current, I_{REF} (pin 9)	All types	0.25		1.0	0.25	1.0	mA	Note 6
Conversion time	All types		15	20		20	µs	Note 2
Nominal analogue input range	All types	–2.5		+2.5			V	Note 3
Supply rejection	All types		0.1				% per V	
Gain error	All types		±0.05				%	Note 4

ZN432 Series

CHARACTERISTICS (*continued*)

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Gain temperature coefficient (Note 4)	ZN432J-10 ZN432BJ-10 ZN432CJ-10		10				ppm/°C	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9 ZN432J-8 ZN432BJ-8 ZN432CJ-8		20				ppm/°C	
Zero temperature coefficient	ZN432J-10 ZN432BJ-10 ZN432CJ-10		7				ppm/°C of FSR	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9 ZN432J-8 ZN432BJ-8 ZN432CJ-8		15				ppm/°C of FSR	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		35				mA	
Power consumption	All types		350				mW	
INTERNAL VOLTAGE REFERENCE Output voltage	All types		2.480				V	
Output voltage tolerance (Note 5)	ZN432J-10 ZN432BJ-10 ZN432CJ-10			±1.5			%	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9			±2.0			%	
	ZN432J-8 ZN432BJ-8 ZN432CJ-8			±5.0			%	
Slope impedance	All types		0.75				Ω	
Maximum Reference load current			±2				mA	

CHARACTERISTICS *(continued)*

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. Range		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
LOGIC	All types							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	$V_S = \pm 5.5V$ $V_I = 2.4V$
			50				μA	$V_S = \pm 5.5V$ $V_I = 5.5V$
Low level input current			1				μA	$V_S = \pm 5.5V$ $V_I = 0.4V$
High level output voltage		2.4			2.4		V	$I_{load} = -40\ \mu A$
Low level output voltage				0.4		0.4	V	$I_{load} = 1.6$ mA

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. This corresponds to a maximum clock rate of 550 kHz based on 11 clock periods per conversion cycle (see timing diagram, page 2–42 This provides an update rate of 45 kHz.

NOTE 3. Single polarity and other input ranges may be provided by different input resistor values. (see page 2–41)

NOTE 4. Excluding reference.

NOTE 5. For typical temperature performance see Fig. 6

NOTE 6. The full scale D to A output current I_{OUT} = 4 times I_{REF}. For optimum performance I_{REF} = 0.5 mA.

TEST CIRCUIT

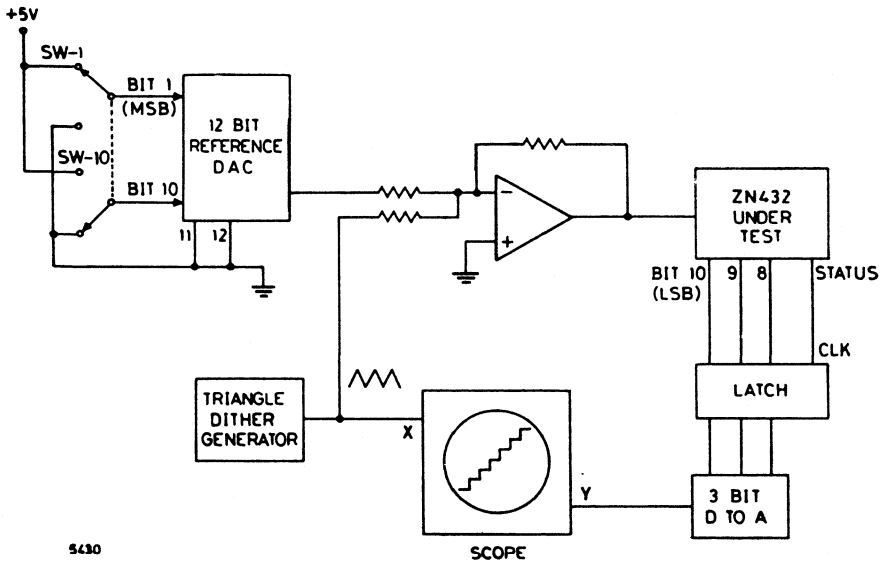


Fig. 3 – DYNAMIC CROSSPLOT ACCURACY TEST

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ L.S.B.) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference D.A.C. in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN432 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit D.A.C. of at least 6-bit accuracy and the analogue output used as the Y deflection for the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator, thus:
   $$R_1 = R_3$$
   And R_2 = parallel combination of R_4, R_5 and R_6.
3. I_{REF} should be 0.5 mA
   Therefore
   $$R_3 = \frac{V_{REF}}{0.5\ mA}$$
   $I_{out\ FS}$ is four times I_{REF}, i.e., 2 mA
4. Analysing the network yields the following:
   $$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$
   $$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$
   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 1.25 kΩ as this determines the D to A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	2.5 kΩ	∞
+2.5	−2.5	5*	10 kΩ	1.25 kΩ	10 kΩ	5 kΩ	2.5 kΩ	5 kΩ
+2.5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	1.25 kΩ	∞
+5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	2.5 kΩ	2.5 kΩ
+4	−2	2.5	5 kΩ	1.25 kΩ	5 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+4	−2	12*	24 kΩ	1.25 kΩ	24 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+10	−10	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	10 kΩ	3.33 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6
*Note 2. External reference

7. For setting up R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

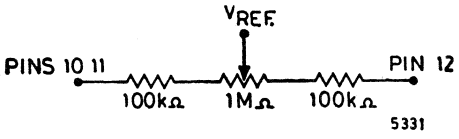


Fig. 4 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION

TIMING DETAILS

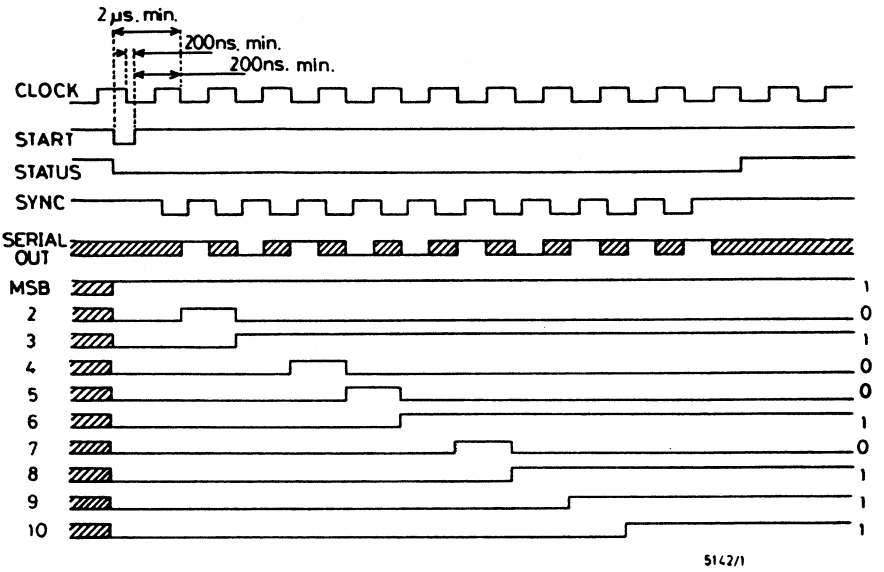


Fig. 5 – TIMING DIAGRAM

NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all the other bits to 0.

2. The first active (negative going) edge of Clock after the trailing edge of the 'START' pulse should not occur until at least 2 µs after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of Clock must not occur within 200 ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.
   Ten SYNC pulses are provided to facilitate data transmission.
   The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the Status Output goes HIGH.

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS –1LSB	1111111111
FS –2LSB	1111111110
¾ FS	1100000000
½ FS +1LSB	1000000001
½ FS	1000000000
½ FS –1LSB	0111111111
¼ FS	0100000000
1LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS –1LSB)	1111111111
+(FS –2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
–(1LSB)	0111111111
–(½ FS)	0100000000
–(FS–1LSB)	0000000001
–FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½ LSB for transition 0000000000 to 0000000001, and of (full scale –1½ LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of –(full scale –½ LSB) for transition 0000000000 to 0000000001, and of (full scale –1½ LSB) for transition 1111111111 to 1111111110.

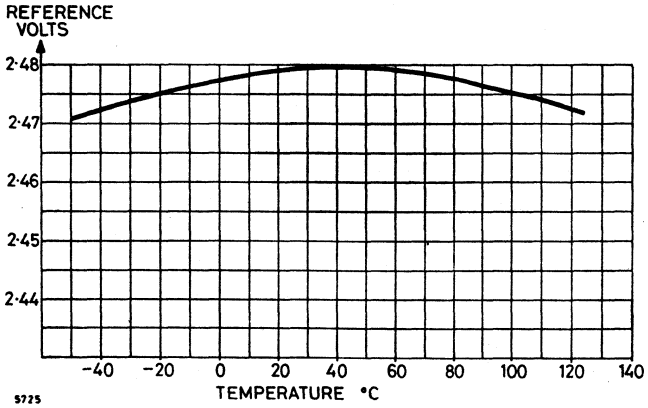
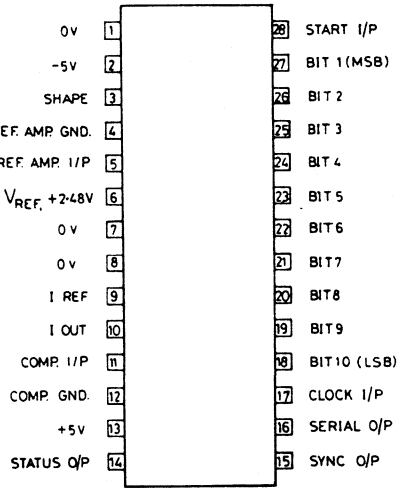


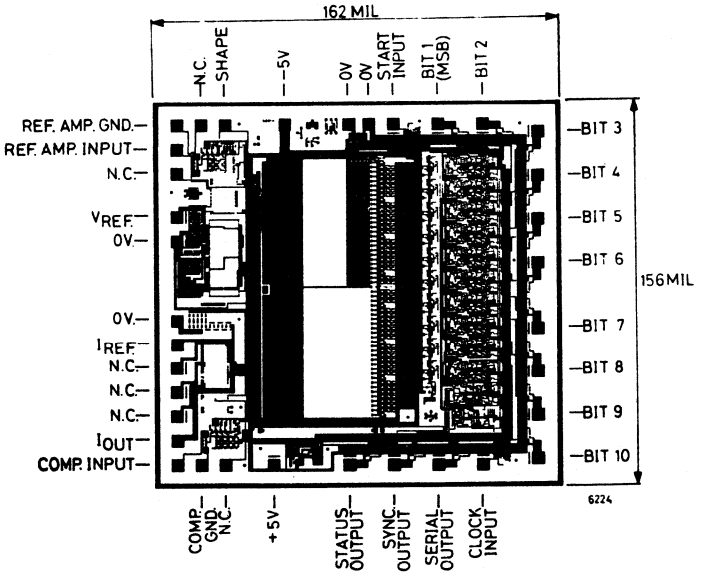
Fig. 6 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE (ALL TYPES)

ZN432 Series

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

A to D CONVERTER

ZN432E

10-Bit Successive Approximation Monolithic A/D Converter

FEATURES

- 10 Bit Resolution
- No Missing Codes
- 20 μs Conversion Time Guaranteed
- Input Range as Desired
- $\pm$ 5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction
- Low Cost Moulded Package

DESCRIPTION

The ZN432E successive approximation analogue to digital converter combines several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to guarantee no missing codes over the operating temperature range.

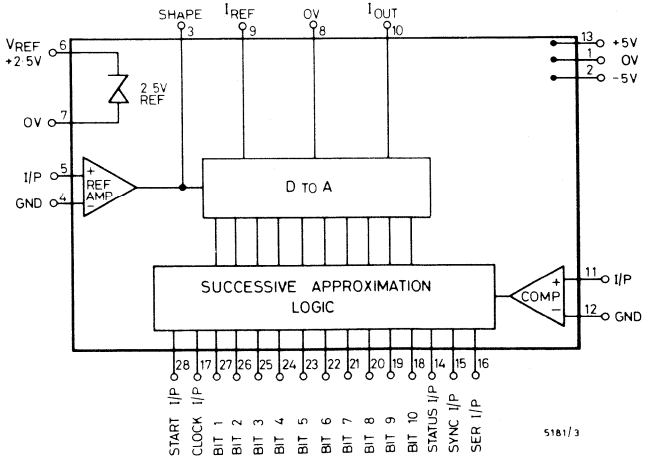


Fig. 1 – INTEGRATED CIRCUIT BLOCK DIAGRAM

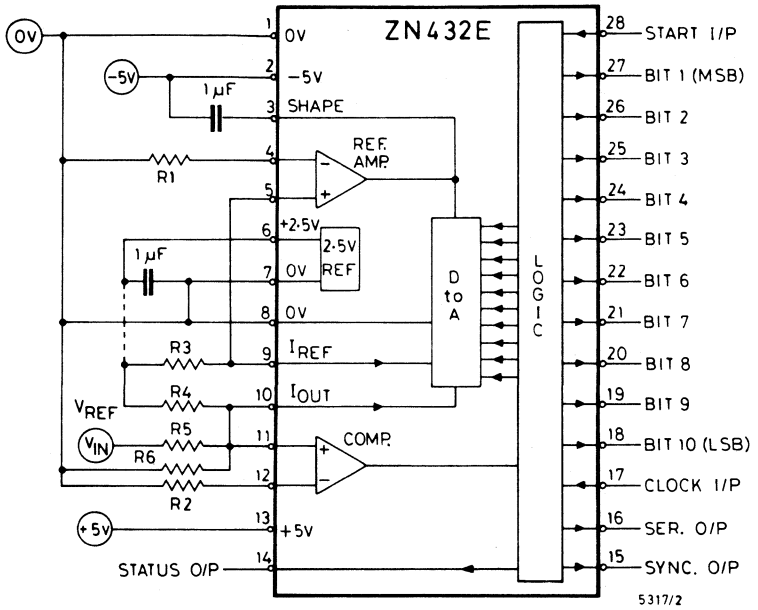


Fig. 2 – TYPICAL EXTERNAL COMPONENTS

ORDERING INFORMATION

TYPE No.	OPERATING TEMPERATURE RANGE	PACKAGE
ZN432E	0 to + 70°C	28 Pin Moulded DIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	± 7 volts	
Logic Input Voltage	+ V_{cc} and OV	
	Min.	Max.
Operating Temperature	0°C	+ 70°C
Storage Temperature	−55°C	+125°C

ELECTRICAL CHARACTERISTICS

(Supply Voltage = ± 5V, Tamb = + 25°C unless otherwise stated)

Parameter	Min.	Typ.	Max.	Units	Conditions
CONVERTER					
Resolution	10	–	–	Bits	
Linearity Error	−1	0	+1	LSB	
Differential Linearity Error	−0.8	0	+1	LSB	Note 1
DAC Reference Current (I_{REF})	0.25	0.5	1	mA	Note 6
Conversion Time	–	15	20	μS	Note 2
Nominal Analogue Input Range	−2.5	–	+2.5	V	Note 3
Supply Rejection		0.1		% per V	
Gain Error		+0.05		%	Note 4
Gain Tempco		20		ppm/°C	
Zero Tempco		15		ppm/°C	
Supply Voltage	± 4.5	± 5	+5.5	V	
Supply Current		35		mA	
Power Consumption		350		mW	
INTERNAL VOLTAGE REFERENCE					
Output Voltage	2.38	2.46	2.54	V	Note 5
Slope Impedance		0.75			
Maximum Load Current		± 2		mA	

ZN432E

CHARACTERISTICS *(continued)*

Parameter	t_{amb} = +25°C			Over Spec. Temp. Range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
LOGIC							
High level input voltage	2.0			2.0		V	
Low level input voltage			0.8		0.8	V	
High level input current		7				μA	V_S = ±5.5V V_I = 2.4V
		50				μA	V_S = ±5.5V V_I = 5.5V
Low level input current		1				μA	V_S = ±5.5V V_I = 0.4V
High level output voltage	2.4			2.4		V	I_{load} = –40 μA
Low level output voltage			0.4		0.4	V	I_{load} = 1.6 mA

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. This corresponds to a maximum clock rate of 550 kHz based on 11 clock periods per conversion cycle (see timing diagram, 2-50). This provides an update rate of 45 kHz.

NOTE 3. Single polarity and other input ranges may be provided by different input resistor values. (See page 2–49)

NOTE 4. Excluding reference.

NOTE 5. For typical temperature performance see Fig. 5

NOTE 6. The full scale D to A output current I_{OUT} = 4 times I_{REF}. For optimum performance I_{REF} = 0.5 mA.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator, thus:

$$R_1 = R_3$$

And R_2 = parallel combination of R_4, R_5, and R_6.

3. I_{REF} should be 0.5mA
   Therefore

$$R_3 = \frac{V_{REF}}{0.5\ mA}$$

   $I_{out\ FS}$ is four times I_{REF}, i.e., 2 mA
4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$

$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$

   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 1.25 k Ω as this determines the D to A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	2.5 kΩ	∞
+2.5	−2.5	5*	10 kΩ	1.25 kΩ	10 kΩ	5 kΩ	2.5 kΩ	5 kΩ
+2.5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	1.25 kΩ	∞
+5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	2.5 kΩ	2.5 kΩ
+4	−2	2.5	5 kΩ	1.25 kΩ	5 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+4	−2	12*	24 kΩ	1.25 kΩ	24 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+10	−10	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	10 kΩ	3.33 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6
Note 2. External reference.

7. For setting up R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

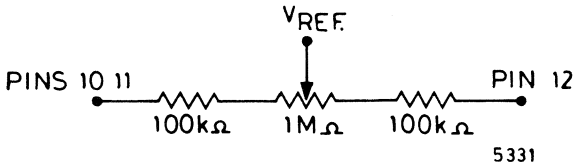


Fig. 3 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION

TIMING DETAILS

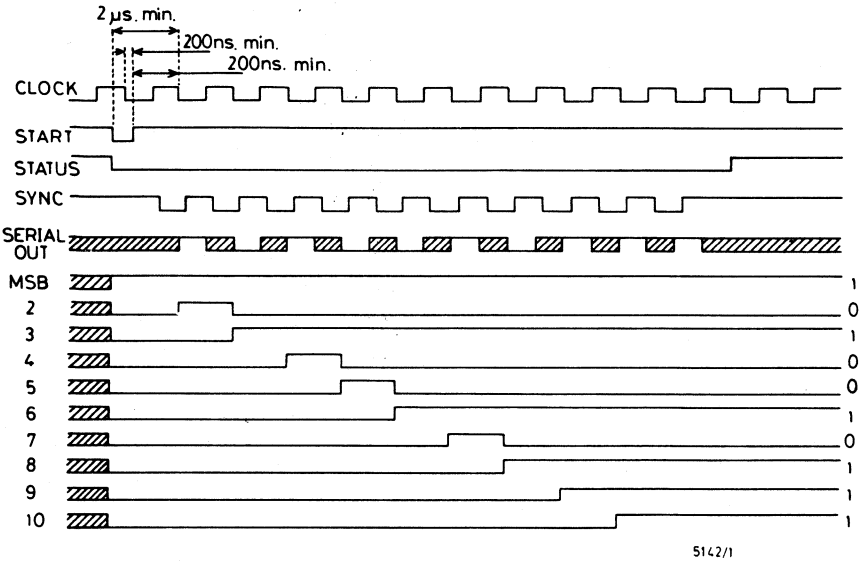


Fig. 4 – TIMING DIAGRAM

NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all the other bits to 0.

2. The first active (negative going) edge of Clock after the trailing edge of the 'START' pulse should not occur until at least 2 μs after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of Clock must not occur within 200 ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.
   Ten SYNC pulses are provided to facilitate data transmission.
   The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the Status Output goes HIGH.

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS −1LSB	1111111111
FS −2LSB	1111111110
¾ FS	1100000000
½ FS +1LSB	1000000001
½ FS	1000000000
½ FS −1LSB	0111111111
¼ FS	0100000000
1 LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS −1LSB)	1111111111
+(FS −2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−(½ FS)	0100000000
−(FS −1LSB)	0000000001
−FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½ LSB for transition 0000000000 to 0000000001, and of (full scale −1½ LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of −(full scale −½LSB) for transition 0000000000 to 0000000001, and of (full scale −1½LSB) for transition 111111111111 to 1111111110.

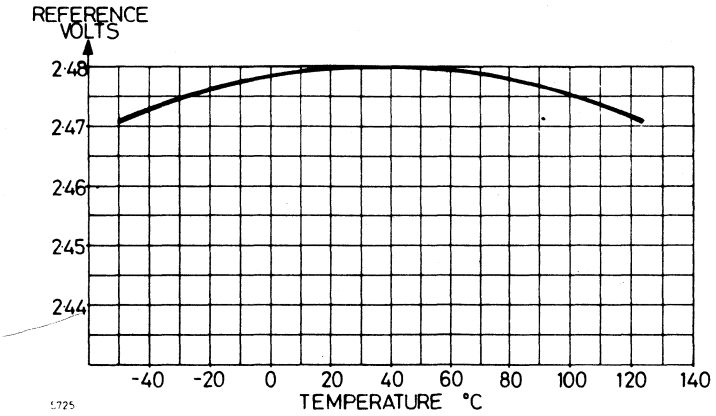


Fig. 5 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE

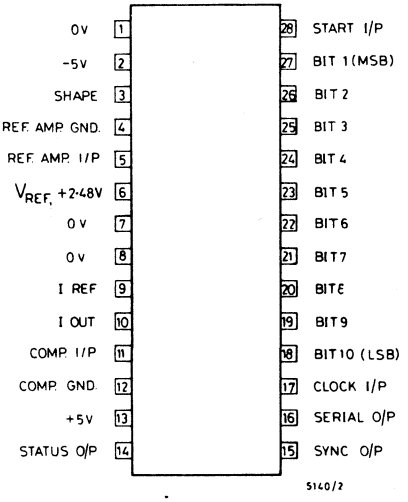


Fig. 6 – PIN CONNECTIONS

FERRANTI semiconductors

A to D CONVERTER

ZN433 Series

10-Bit Tracking Monolithic A/D Converter

FEATURES

- 10, 9 and 8-Bit Accuracies
- 3 Operating Temperature Ranges
- 1μs Conversion Time (Assuming Continuous Tracking)
- Input Range as Desired
- $\pm$5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction

DESCRIPTION

The ZN433 range of tracking analogue to digital converters combines several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), tracking logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast window comparator with good overload recovery. At a resolution appropriate to the accuracy specification, no missing codes are obtained over the full temperature range.

The tracking principle ensures continuous up to date conversion data. This is suitable for single channel conversion, e.g. digital transducers, and often obviates the need for sample and hold.

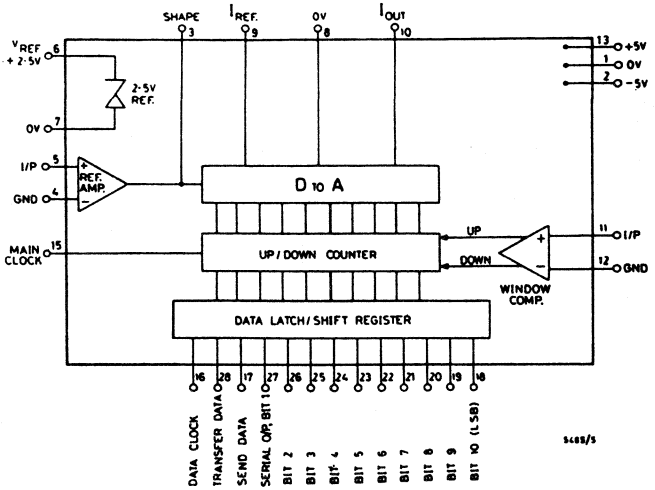


Fig. 1 – SYSTEM DIAGRAM

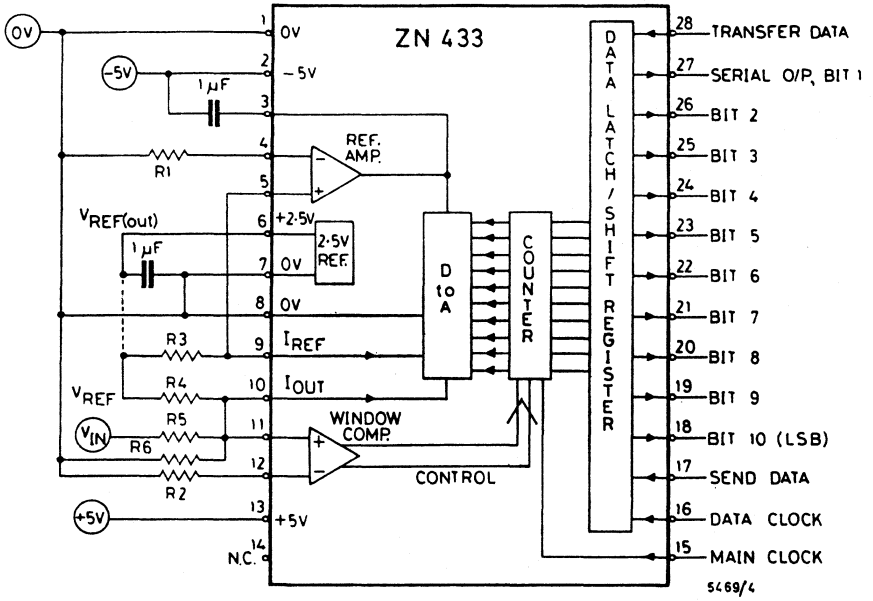


Fig. 2 – TYPICAL EXTERNAL COMPONENTS

See page 93 for calculation of resistor values. When the internal reference is used, $V_{REF(out)}$ (pin 6) is connected to R3 and R4 as shown. An external reference may also be used, which for ratiometric operation can vary by ±20% of nominal.

ORDERING INFORMATION

Operating Temperature	10-bit accuracy	9-bit accuracy	8-bit accuracy	Package
–55 to +125°C	ZN433J-10	ZN433J-9	ZN433J-8	Ceramic
–40 to +85°C	ZN433BJ-10	ZN433BJ-9	ZN433BJ-8	Ceramic
0 to +70°C	ZN433CJ-10	ZN433CJ-9	ZN433CJ-8	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply Voltages .. .. ±7 volts
Logic Input Voltage .. .. .. $+V_{CC}$ and 0V
Storage Temperature Range .. .. –55°C to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	Version	T_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
CONVERTER								
Accuracy (useful resolution)	ZN433J-10 ZN433BJ-10 ZN433CJ-10	10			10		Bits	Note 1
	ZN433J-9 ZN433BJ-9 ZN433CJ-9	9			9		Bits	
	ZN433J-8 ZN433BJ-8 ZN433CJ-8	8			8		Bits	
Non-linearity	All types			±0.5			LSB	
Differential non-linearity	All types		±0.5				LSB	Note 1
Operating temp. range	ZN433J-10 ZN433J-9 ZN433J-8				–55	+125	°C	
	ZN433BJ-10 ZN433BJ-9 ZN433BJ-8				–40	+85	°C	
	ZN433CJ-10 ZN433CJ-9 ZN433CJ-8				0	+70	°C	
D to A reference current, I_{REF} (pin 9)	All types	0.8		1.2	0.8	1.2	mA	Note 2
Max. Clock Rate	All types	1	1.2		1		MHz	Note 3
Nominal analogue input range	All types	–2.5		+2.5			V	Note 4
Supply rejection	All types		0.1				% per V	

ZN433 Series

CHARACTERISTICS *(continued)*

Parameter	Version	T_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Gain temperature coefficient (Note 5)	ZN433J-10 ZN433BJ-10 ZN433CJ-10		10				ppm/°C	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9 ZN433J-8 ZN433BJ-8 ZN433CJ-8		20				ppm/°C	
Zero temperature coefficient	ZN433J-10 ZN433BJ-10 ZN433CJ-10		7				ppm/°C of FSR	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9 ZN433J-8 ZN433BJ-8 ZN433CJ-8		15				ppm/°C of FSR	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		50				mA	
Power consumption	All types		500				mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types		2.480				V	
Output voltage tolerance (Note 6	ZN433J-10 ZN433BJ-10 ZN433CJ-10			±1.5			%	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9			±2.0			%	
	ZN433J-8 ZN433BJ-8 ZN433CJ-8			±5.0			%	
Slope impedance	All types		0.75				Ω	
Maximum reference load current			±4				mA	

CHARACTERISTICS (*continued*)

Parameter	Version	T_{amb} = +25°C			Over Spec. Temp. Range		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
LOGIC	All types							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	V_S = ±5.5V V_I = 2.4V
			50				μA	V_S = ±5.5V V_I = 5.5V
Low level input current			1				μA	V_S = ±5.5V V_I = 0.4V
High level output voltage		2.4			2.4		V	I_{load} = −40 μA
Low level output voltage				0.4		0.4	V	I_{load} = 1.6 mA

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. The full scale D to A output current I_{out} = 4 times I_{REF}. For optimum performance I_{REF} = 1.0 mA.

NOTE 3. For main clock waveform see Fig. 5, 2-60 . Input signals which do not change by more than 1 LSB/μs may be tracked continuously without the need for a sample and hold. This corresponds to a full scale bandwidth of 300 Hz. Higher frequencies may be tracked if the amplitude is reduced, e.g. the half full scale bandwidth is 600 Hz.

NOTE 4. Single polarity and other input ranges may be provided by different input resistor values (see 2-59)

NOTE 5. Excluding reference.

NOTE 6. For typical temperature performance see Fig. 6

TEST CIRCUIT

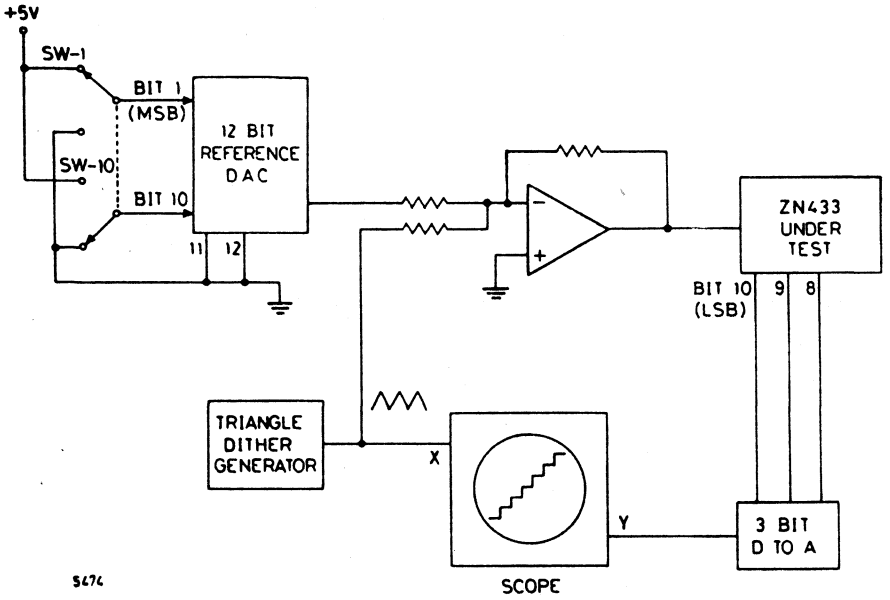


Fig. 3 – DYNAMIC CROSSPLOT ACCURACY TEST

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ L.S.B.) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference D.A.C. in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN433 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3 bit D.A.C. of at least 6 bit accuracy and the analogue output used as the Y deflection for the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator which both operate in a virtual earth mode. Thus: $R_1 = R_3$
   And R_2 = parallel combination of R_4, R_5 and R_6.
3. I_{REF} should be 1.0 mA, though it may be varied from 0.8 mA to 1.2 mA,
   Therefore $$R_3 = \frac{V_{REF}}{1.0\ mA}$$
   $I_{out\ FS}$ is four times I_{REF}, i.e., 4 mA (I_{out} for zero reading is 0 mA).
4. Analysing the network yields the following:
   $$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$
   $$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$
   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 625Ω as this determines the D to A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.25 kΩ	1.25 kΩ	∞
+2.5	−2.5	5*	5 kΩ	625Ω	5 kΩ	2.5 kΩ	1.25 kΩ	2.5 kΩ
+2.5	0	2.5	2.5 kΩ	625Ω	2.5 kΩ	∞	625Ω	∞
+5	0	2.5	2.5 kΩ	625Ω	2.5 kΩ	∞	1.25 kΩ	1.25 kΩ
+4	−2	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.875 kΩ	1.5 kΩ	2.5 kΩ
+4	−2	12*	12 kΩ	625Ω	12 kΩ	1.875 kΩ	1.5 kΩ	2.5 kΩ
+10	−10	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.25 kΩ	5 kΩ	1.67 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6

*Note 2. External reference

7. For setting up: R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

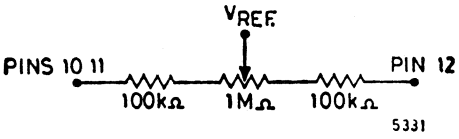


Fig. 4 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION

LOGIC DETAILS

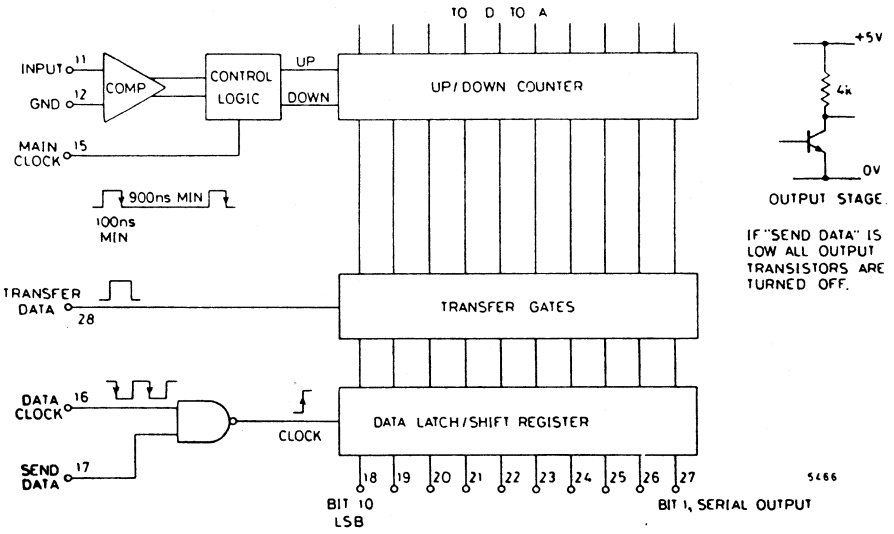


Fig. 5 – LOGIC SYSTEM

NOTES ON LOGIC DIAGRAM

1. The Window Comparator and Control Logic determine whether the Counter will clock up or down or keep the same value on an active (negative going) edge of the Main Clock.

2. Parallel data from the Up/Down Counter will be loaded into the output Data Latch/Shift Register when the TRANSFER DATA input is HIGH. TRANSFER DATA should not be taken HIGH until 150 ns after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge. The minimum TRANSFER DATA pulse width is 50 ns.

   If TRANSFER DATA is held permanently HIGH then the Counter outputs will appear directly at the bit outputs.

3. Serial output data (MSB first) can be obtained from the MSB output (Pin 27) by applying a DATA CLOCK (Pin 16, 1 MHz maximum, 100 ns minimum pulse width).

4. A LOW on SEND DATA (Pin 17) disables the DATA CLOCK and turns off all the output transistors so that all the bit outputs are HIGH (see diagram of output).

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS –1LSB	1111111111
FS –2LSB	1111111110
¾ FS	1100000000
½ FS +1LSB	1000000001
½ FS	1000000000
½ FS –1LSB	0111111111
¼ FS	0100000000
1LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS –1LSB)	1111111111
+(FS –2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
–(1LSB)	0111111111
–(½ FS)	0100000000
–(FS –1LSB)	0000000001
–FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full scale –1½LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of –(full scale –½LSB) for transition 0000000000 to 0000000001, and of (full scale –1½LSB) for transition 1111111111 to 1111111110.

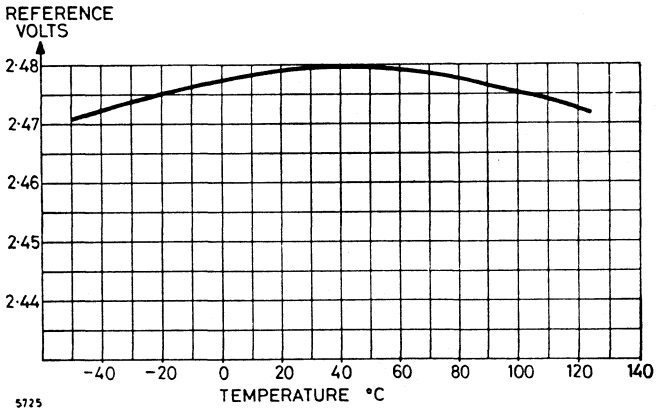
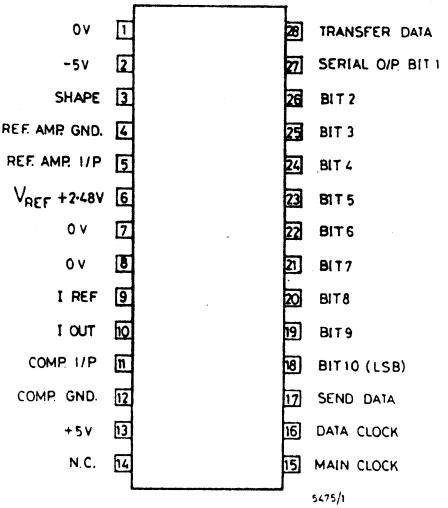


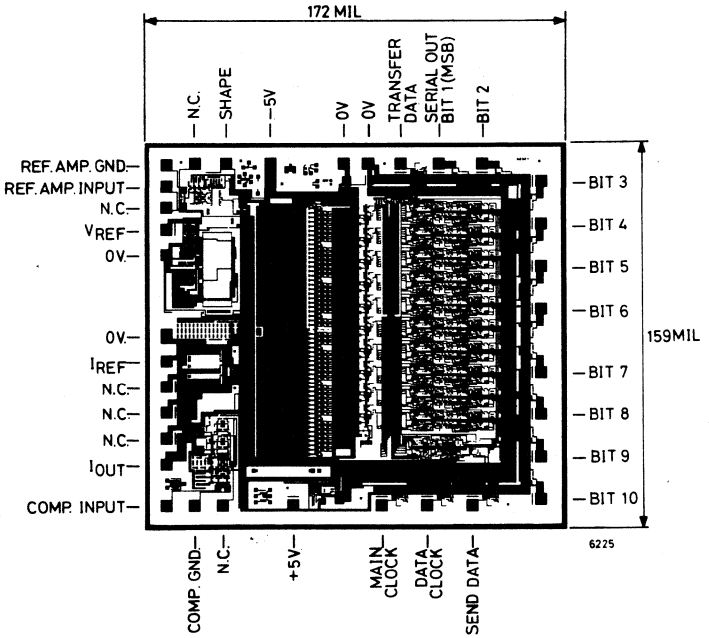
Fig. 6 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE (ALL TYPES)

ZN433 Series

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZN440

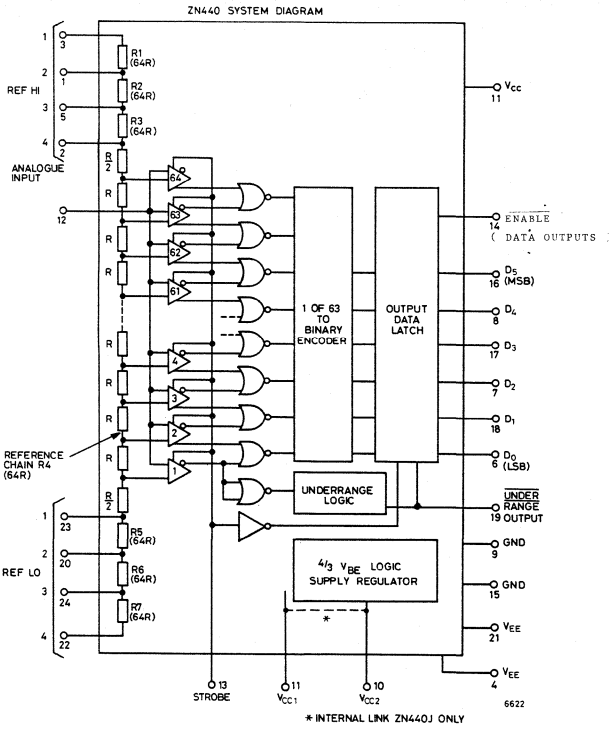
Ultra Fast Monolithic Video A/D Converter

ADVANCE PRODUCT INFORMATION

Some parametric limits may be subject to change

Features

- 18 million conversions per second
- 6 bit resolution
- Expandable to 7 or 8 bits
- ± 1/2 LSB linearity
- No sample-and-hold required
- Unipolar or bipolar input range
- TTL compatible
- ±5V supply
- 1W power dissipation



Description

The ZN440 is a high-speed, 6 bit parallel A to D converter capable of digitising an analogue signal at rates from DC to 18 megasamples per second. AC signals with frequency components up to several MHz can accurately be digitised without the need for an external sample-and-hold circuit. Two or four ZN440's can be stacked to give a 7- or 8-bit converter with a minimum of external components.

Applications include high-speed data acquisition, video and radar data conversion, digital signal storage and image processing.

Absolute Maximum Ratings

V_{CC}.....0 to +5.5V
V_{EE}.....0 to -5.5V
Inputs, digital.....0 to +5V
Input, Analogue Signal.....-4.2V to +1.4V
Maximum Reference Chain Current.....60mA
Operating Temperature Range.....0 to +70°
Storage Temperature Range.....-55°C to +125°C
Electrical Characteristics (± 5V supply, Tamb = +25°C unless otherwise stated. Output load as figure 8).

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
POWER SUPPLY					
Recommended Supply Voltage					
V_{CC}	+4.75	+5	+5.25	volts	
V_{EE}	-4.75	-5	-5.25	volts	
Supply Current					
I_{CC}	-	95	150	mA	
I_{EE}	-	55	80	mA	
ANALOGUE					
Reference Voltage Across	-	-	1	volts	0 to +70°C
Comparator Chain $-V_{REF}$					
Reference Resistor R	-	0.3	-	ohms	
Resolution	6	-	-	bits	
Linearity Error	-	-	±0.5	LSB	V_{REF} = 1V
	-	-	±0.5	LSB	V_{REF} = 0.5V
Input Signal Range	-4.0	-	+0.5	volts	
Input Resistance, R_{IN}	8	-	-	K	V_{REF} = 1V
Input Capacitance, C_{IN}	-	-	100	pF	
Input Bias Current I_{BIAS}	-	-	90	µA	

Continued overleaf.....

Electrical Characteristics cont/d

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL (static)					
High Level Input Voltage, V_{IN}	1.4	-	-	volts	
Low Level Input Voltage, V_{IL}	-	-	0.8	volts	
High Level Input Current, I_{IH}	-	-	-	µA	)
Low Level Input Current, I_{IL}	-	-	-	mA	) (Note 2)
High Level Output Voltage, V_{OH}	2.4	-	-	volts	I_{OH} = 400µA
Low Level Output Voltage, V_{OL}	-	-	0.4	volts	I_{OL} = -1.6 mA
DYNAMIC					
Convert Pulse Width $-\tau_H$	20	-	-	ns	(Note 1)
Strobe Low Period $-\tau_L$	-	40	-	ns	
Maximum Sampling Frequency	16	18	-	MHz	
Digital Output Delays					
t_1	50	55	100	ns	
t_2	90	95	120	ns	
t_3	50	55	80	ns	
t_4	65	70	100	ns	
Aperture Delay $-T_{ad}$	-	20	-	ns	
Transient Response (Recover from full-scale step input)	-	15	-	ns	
Output Enable Delays					
T_{D1}	7	8	15	ns	
T_{D2}	27	28	15	ns	
T_{E1}	22	25	35	ns	
T_{E2}	35	40	80	ns	

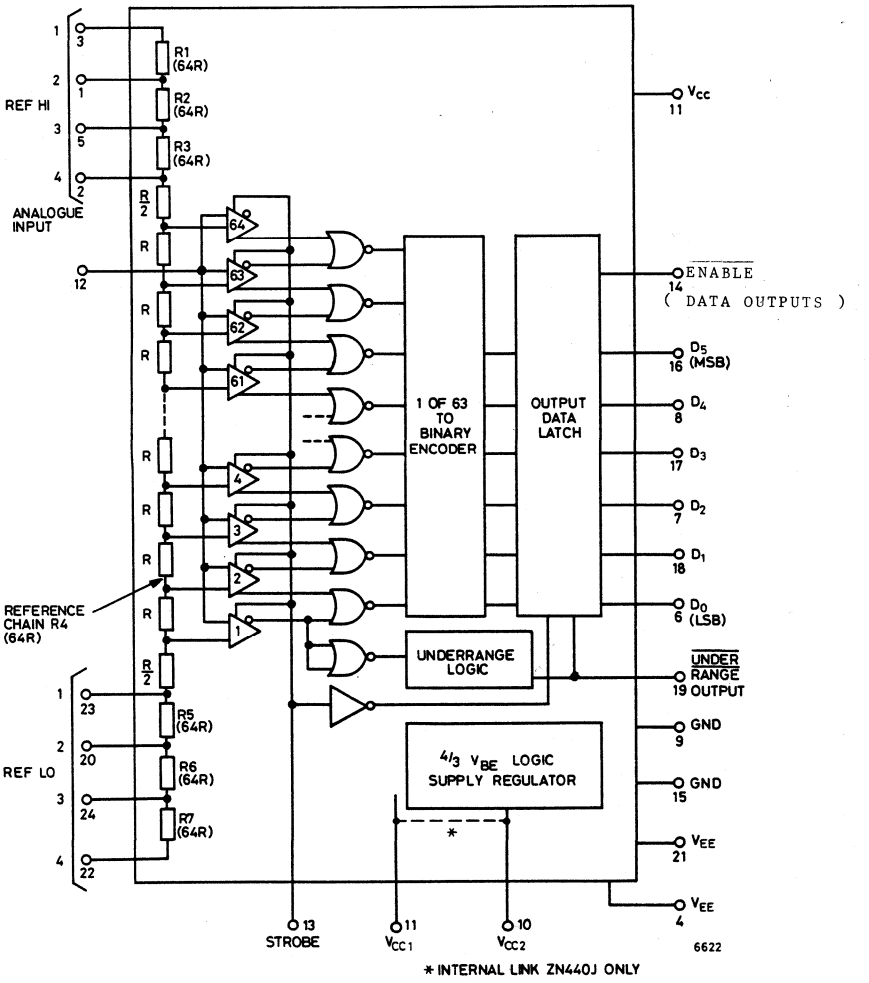
Note 1

Although the STROBE input is TTL compatible, for maximum speed the HIGH Level should be at least +3V. If a normal totem-pole TTL output is used to drive pin 13 then a 1k pullup should be used to ensure this.

Note 2

The $\overline{\text{output ENABLE}}$ input consists of a high speed buffer circuit which can be driven from a standard TTL totem-pole output. if other TTL inputs are to be driven by the same signal the ZN440 $\overline{\text{Output ENABLE}}$ input should be buffered owing to its input loading characteristics.

ZN440 SYSTEM DIAGRAM



SYSTEM DESCRIPTION

The ZN440 is an ultra-high speed parallel (flash) A to D converter comprising an array of 64 strobed comparators and encoding logic. A reference voltage applied across a tapped resistor chain defines 63 quantisation levels plus overrange and underrange, one input of each comparator being connected to the resistor string, whilst the other inputs are commoned and connected to the analogue input. When an analogue input is applied all the comparators whose reference voltage is less than the analogue input will change state, i.e. if the input voltage is $\frac{n}{64} V_{REF}$ then n comparators will have tripped. The comparator outputs are decoded into 1 of 64 format by NOR gates and then re-encoded into binary by a high-speed ROM.

STROBE INPUT

The STROBE input controls the comparators and the output data latch. Whilst STROBE is high the comparators are sampling the input signal, the results of the last sample are stored in the latch and are available as the output data.

When STROBE goes low the comparator outputs are latched in their current state whilst the output data latch is made transparent and the results of the new sample appear at the data outputs.

When STROBE goes high again this new value is latched at the data outputs whilst the comparators again sample the input. in this way valid data always appears at the outputs except at a negative going STROBE edge. A STROBE timing diagram is shown in figure 2.

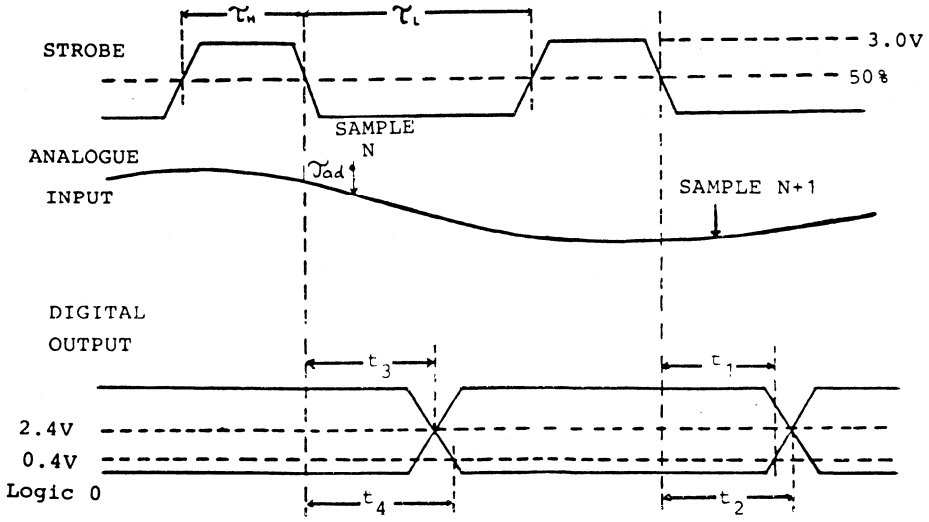


FIG. 2. STROBE TIMING

Output ENABLE

All logic outputs of the ZN440 are of the open-collector type requiring an external pullup of nominally 2k. The data output transistors may be turned off by taking the $\overline{\text{ENABLE}}$ pin high. A timing diagram for output enable/disable delays is given in figure 3.

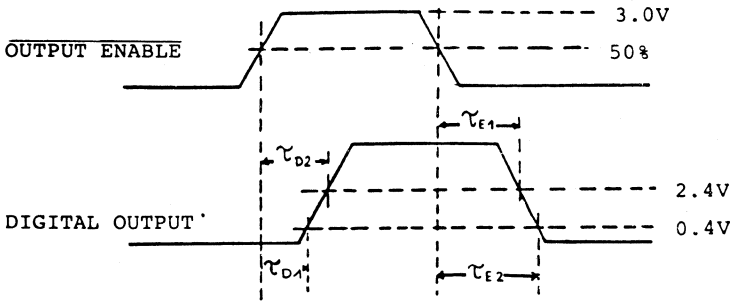


FIG. 3. OUTPUT $\overline{\text{ENABLE}}$ TIMING

Underrange/Overrange

When the analogue input voltage is less than the threshold of comparator 1 the data outputs turned off and the $\overline{\text{underrange}}$ output is low. Similarly, if the analogue input is above the threshold of comparator 64 then the outputs are also turned off.

Whenever the input voltage is greater than the threshold of comparator 1 then the underrange output is high.

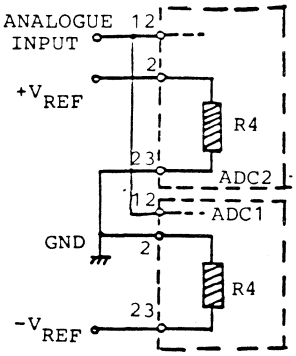
Stacking

Provision of an $\overline{\text{underrange}}$ output and the fact that both ends of the reference resistor chain are accessible means that two or four ZN440's can easily be stacked to form a 7- or 8- bit converter. In theory the reference resistor chains of two or four ZN440's could simply be connected in series to give an array of 128 or 256 comparators and thus 7- or 8- bit resolution.
However, due to differences in the absolute value of resistor between different ICs the voltage drop across each reference chain might not be the same, giving rise to linearity errors.

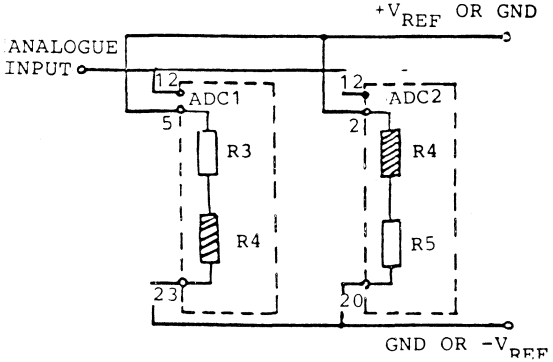
To overcome this problem the ZN440 is provided with (untapped) resistors at each end of the reference chain. By making suitable connection to these resistors it is possible to make each ZN440 operate over half the total reference voltage in the case of the 7- bit stack or one-quarter of the total reference voltage in the case of the 8-bit stack. The reference chain connections for 7- and 8-bit stacks, for both unipolar and bipolar operation, are shown in figure 4.

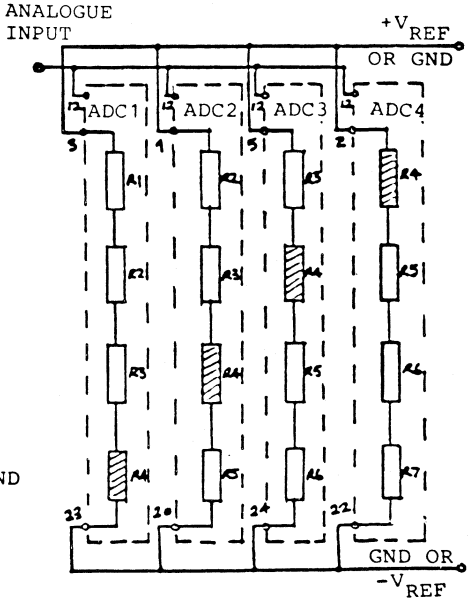
The matching of the reference resistors is sufficiently accurate to ensure that linearity is maintained for the 7- and 8-bit stacks. Each converter operates over its own portion of the reference range without any overlap or gaps at the transition points.

Note that the total reference voltage for the stacked converters should be chosen so that the reference voltage across the reference chain (R4) in each converter is within the 0.5 to 1V limit, e.g. for the 8-bit unipolar stack the total reference voltage should be between 2V and 4V.



7-BIT (BIPOLAR INPUT RANGE SYMMETRICAL ABOUT ZERO)





8-BIT (UNIPOLAR OR ASYMMETRIC BIPOLAR INPUT)

7-BIT(UNIPOLAR OR ASYMETRIC BIPOLAR INPUT)

In stacked configurations the six least significant bits are obtained simply by bussing together the D_0 to D_6 outputs of all the converters. In the case of a 7-bit stack the MSB (D6) is simply the underrange of the second converter, as shown in figure 5. In order to give the same loading conditions as the other six outputs it is wire AND-ed to the output of the first converter though this has no effect from a logic point of view.

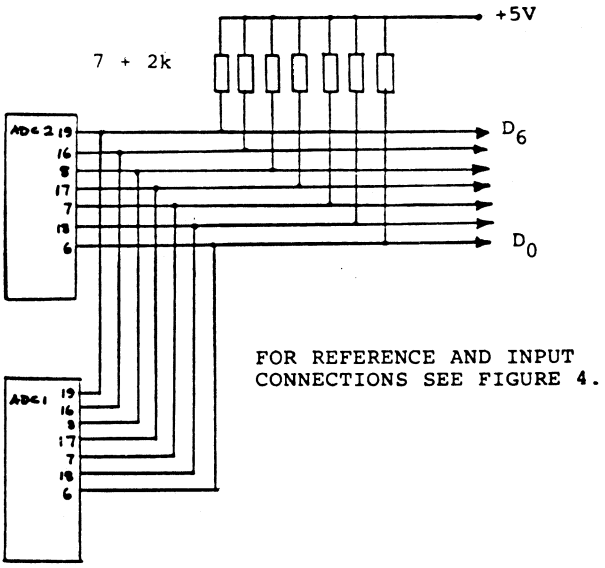


Fig. 5. LOGIC CONNECTIONS FOR 7-BIT STACKING

For the eight bit configuration bit 7 and bit 8 are obtained by decoding the underrange outputs using two exclusive-OR gates as shown in figure 6. This, of course, increases the conversion time due to the additional propagation delays introduced into the bit 7 and bit 8 outputs.

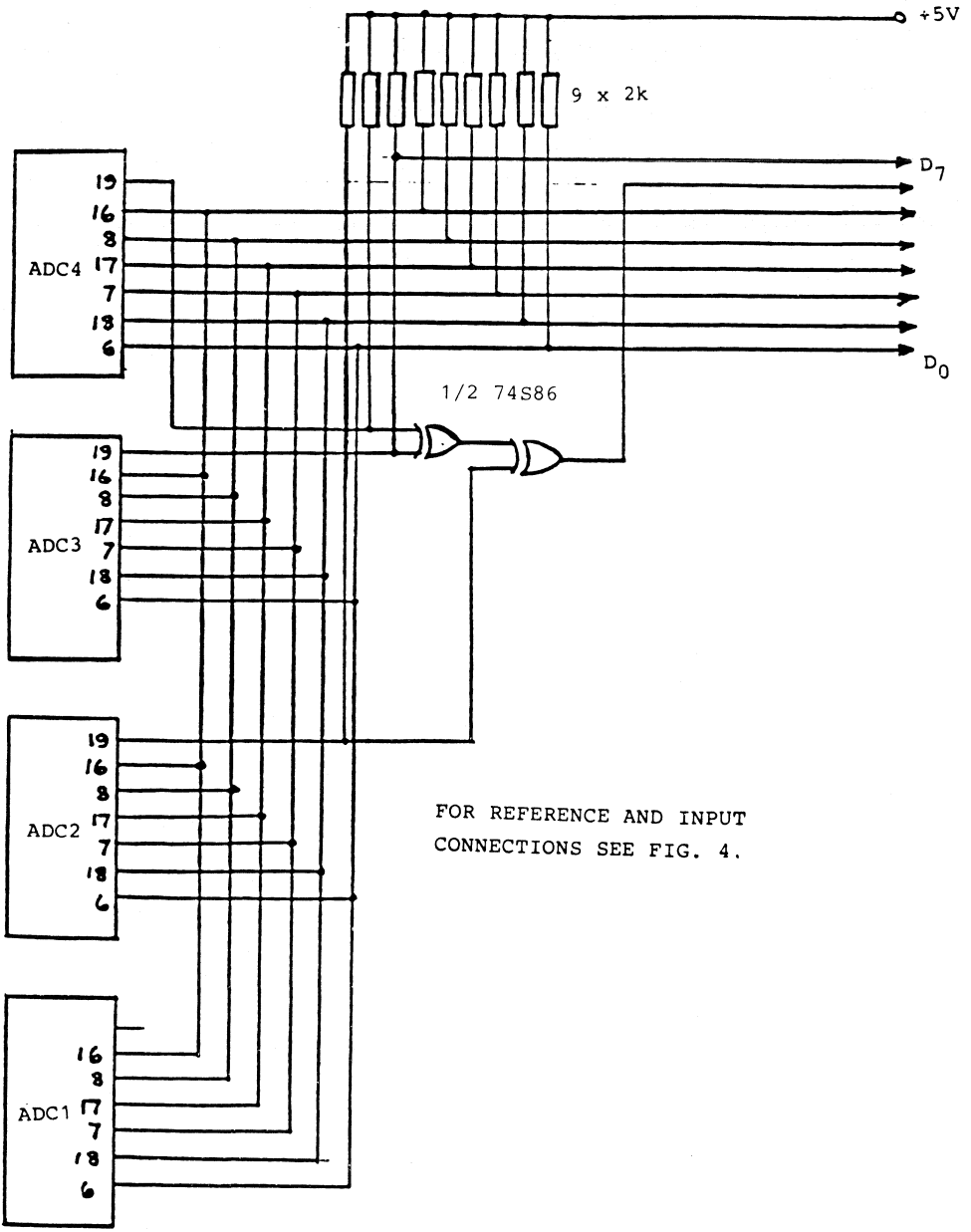


FIG. 6. LOGIC CONNECTIONS FOR 8-BIT STACKING

Clock Generator and Strobe Driver Circuit

A suggested circuit for generating the STROBE pulses to the ZN440 is shown in figure 7. This consists of an oscillator based on Schmitt trigger N1 driving a pulse shaper circuit comprising N3-N6. The clock frequency and STROBE high period can be independently adjusted using P1 and P2 respectively.

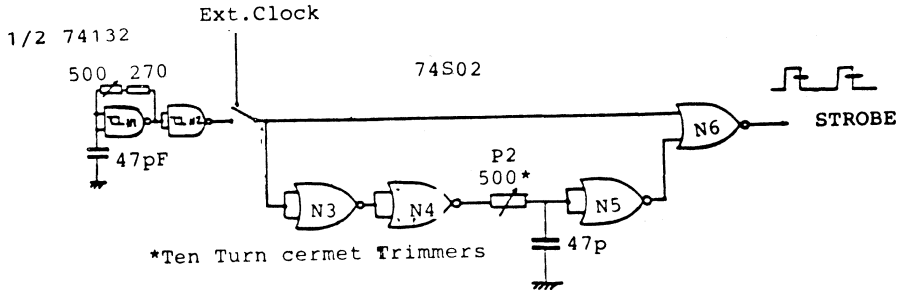


FIG. 7. CLOCK GENERATOR AND STROBE PULSE SHAPER

Test Circuit

A suggested test circuit for the ZN440 is shown in figure 8a. The loading conditions on all data outputs should be as shown in figure 8b.

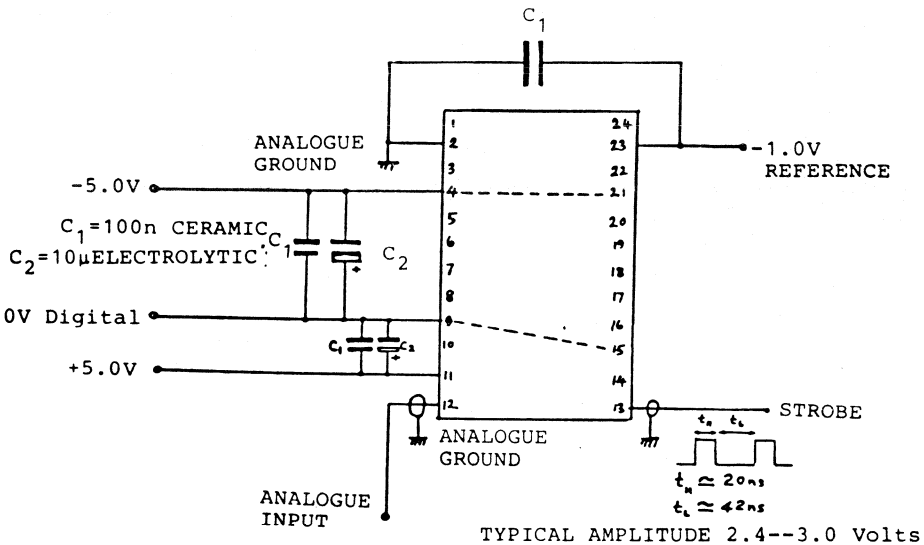


FIG. 8a. ZN440 TEST CIRCUIT

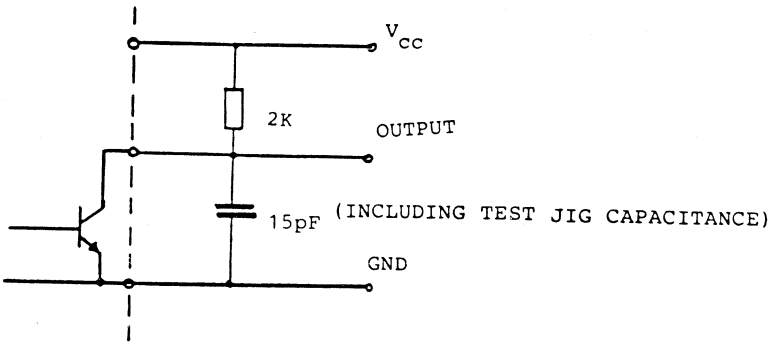
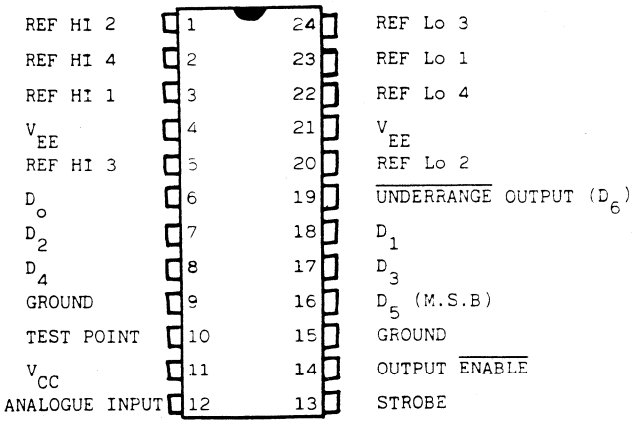


FIG. 8b. ZN440 OUTPUT TEST CIRCUIT



ZN440 PIN CONNECTIONS

FERRANTI semiconductors

A–D CONVERTER
ZN447
ZN448
ZN449

8-Bit µP – Compatible A to D Converters

FEATURES

- Easy interfacing to microprocessors or operates as a 'stand alone' converter
- Fast 9 µs conversion time guaranteed
- Choice of linearity: ¼LSB–ZN447, ½LSB–ZN448, 1LSB–ZN449
- On-chip clock
- Choice of on-chip or external reference voltage
- Unipolar or bipolar input ranges
- Choice of commercial or military temperature range

DESCRIPTION

The ZN447, ZN448 and ZN449 are 8-bit, successive approximation A to D converters designed for easy interfacing to microprocessors. All active circuitry is contained on-chip including a clock generator and stable 2.5V bandgap reference.

Only a reference resistor and capacitor, clock resistor and capacitor and input resistors are required for operation with either unipolar or bipolar input voltages. The ZN447, -8 and 9 are the most complete 8-bit monolithic ADCs available.

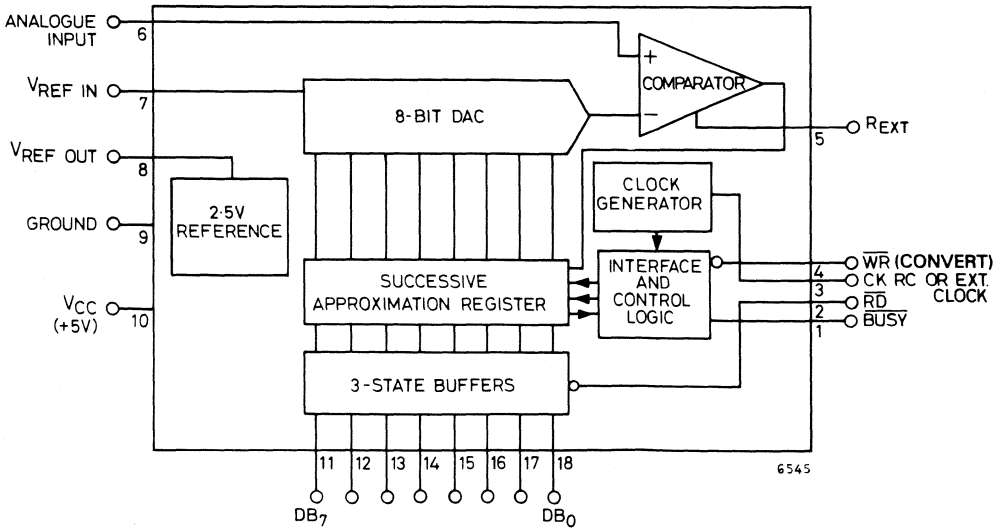


Fig. 1 SYSTEM DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{cc} ..... +7.0 volts
Max. Voltage, Logic and V_{REF} Inputs ..... V_{cc}
Operating Temperature Range ..... 0°C to +70°C ('E' package)
−55°C to +125°C ('J' package)
Storage Temperature Range ..... −55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{cc} = +5V, Tamb = 25°C, f_{c1k} = 900kHz, unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
ZN447					
Linearity Error	—	—	±¼	LSB	
Differential Linearity Error	—	—	±½	LSB	
Zero Transition (00000000→00000001)	13.5 15.0	15 16.5	16.5 18.0	mV mV	Moulded 'E' package Ceramic 'J'package
Full-scale Transition (11111110→11111111)	2.548	2.550	2.552	V	V_{REF} = 2.560V
ZN448					
Linearity Error	—	—	±½	LSB	
Differential Linearity Error	—	—	±1	LSB	
Zero Transition (00000000→00000001)	12.0 13.0	15.0 16.5	18.0 20.0	mV mV	Moulded 'E' package Ceramic 'J'package
Full-scale Transition (11111110→11111111)	2.545	2.550	2.555	V	V_{REF} = 2.560V
ZN449					
Linearity Error	—	—	±1	LSB	
Differential Linearity Error	—	—	±2	LSB	
Zero Transition (00000000→00000001)	10.0 11.5	15.0 16.5	20.0 21.5	mV mV	Moulded 'E'package Ceramic 'J'package
Full-scale Transition (11111110→11111111)	2.542	2.550	2.558	V	V_{REF} = 2.560V
ALL TYPES					
Resolution	8	—	—	Bits	
Linearity Temperature Coefficient	—	±3.0	—	ppm/°C	
Differential Lienarity Temperature Coefficient	—	±6.0	—	ppm/°C	
Full-scale Temperature Coefficient	—	±2.5	—	ppm/°C	
Zero Temperature Coefficient	—	±8.0	—	µV/°C	
Reference Input Range	1	—	3	V	
Supply Voltage	4.5	5	5.5	V	
Supply Current	—	25	40	mA	
Power Consumption	—	125	—	mW	

ELECTRICAL CHARACTERISTICS (V_{cc} = +5V, Tamb = 25°C, f_{c1k} = 900kHz, unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
COMPARATOR					
Input Current	—	1	—	µA	V_{IN} = +3V, R_{EXT} = 82k
Input Resistance	—	100	—		
Tail Current	25	65	150	µA	V— = —5v
Negative Supply	-3	-5	-30	V	
Input Voltage	-0.5	—	+3.5	V	
ON CHIP REFERENCE					
Output Voltage ZN447	2.530	2.550	2.570		R_{REF} = 390
ZN448	2.520	2.550	2.580	V	
ZN449	2.500	2.550	2.600		C_{REF} = 4µ7
Slope Resistance	—	0.5	2	ohms	
V_{REF} Temperature Coefficient	—	50	—	ppm/°C	
Reference Current	4	—	15	mA	
CLOCK					
On-chip Clock Frequency	—	—	1	MHz	
Clock Frequency Tempco	—	+0.5	—	%/°C	
Clock Resistor	—	—	2.0	kohms	
Maximum External Clock Frequency	—	0.9	1	MHz	
Clock Pulse Width	500	—	—	ns	
High Level Input Voltage V_{IH}	4.0	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	—	800	µA	V_{IN} = +4.0 V, V_{CC} = MAX
Low Level Input Current I_{IL}	—	—	−500	µA	V_{IN} = +0.8 V, V_{CC} = MAX
LOGIC (over operating temperature range)					
CONVERT INPUT					
High Level Input Voltage V_{IH}	2	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	300	—	µA	V_{IN} = +2.4 V, V_{CC} = MAX
Low Level Input Current I_{IL}	—	±10	—	µA	V_{IN} = +0.4 V, V_{CC} = MAX
$\overline{RD}$ INPUT					
High Level Input Voltage V_{IH}	2.0	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	−150	—	µA	V_{IN} = +2.4V, V_{CC} = MAX
Low Level Input Current I_{IL}	—	−300	—	µA	V_{IN} = +0.4V, V_{CC} = MAX

ELECTRICAL CHARACTERISTICS (V_{cc} = +5V, Tamb = 25°C, f_{c1k} = 900kHz, unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
High Level Output Voltage V_{OH}	2.4	—	—	V	I_{OH} = MAX, V_{CC} = MIN
Low Level Output Voltage V_{OL}	—	—	0.4	V	I_{OL} = MAX, V_{CC} = MIN
High Level Output Current I_{OH}	—	—	−100	μA	
Low Level Output Current I_{OL}	—	—	1.6	mA	
Three-state Disabled Output Leakage	—	—	2	μA	V_{OUT} = +2.0V
Input Clamp Diode Voltage	—	—	−1.5	V	
$\overline{RD}$ Input to Data Output Enable/Disable	—	180	250	ns	
Delay Times T_{E1}	180	210	260	ns	
T_{E0}	60	80	100	ns	
T_{D1}	80	110	140	ns	
T_{D0}	60	80	100	ns	
Convert Pulse Width $T_{\overline{WR}}$	200	–	—	ns	
$\overline{WR}$ Input to $\overline{BUSY}$ Output	—	—	250	ns	
Propagation Delay T_{BD}	—	—	—	—	

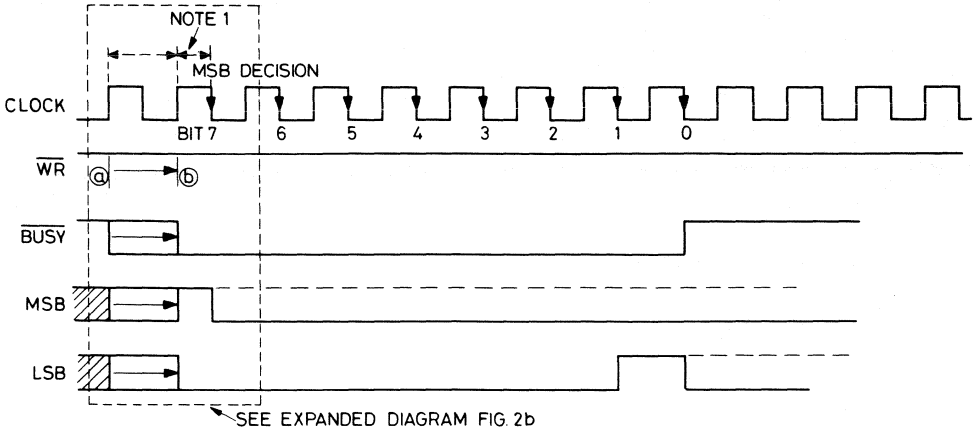
GENERAL CIRCUIT OPERATION

The ZN447 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2}$ V_{IN} or leave it set to 1 if $\frac{V_{REF}}{2}$ V_{IN}. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2}$ + $\frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the eighth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the $\overline{RD}$ input will normally be held high to keep the 3-state buffers in their high impedance state. Data can be read out by taking $\overline{RD}$ low, thus enabling the 3-state outputs. Readout is non-destructive.

CONVERSION TIMING

The ZN447 will accept a low-going CONVERT pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 7½ and 8½ clock pulses later depending on the relative timing of the clock and CONVERT signals. Timing diagrams for a conversion are shown in figure 2.



NOTE 1. GUARANTEED PERIOD OF ½ CLOCK CYCLE MIN. 1½ CLOCK CYCLES MAX. ALLOWS MSB TO SETTLE BEFORE MSB DECISION

FIG. 2a

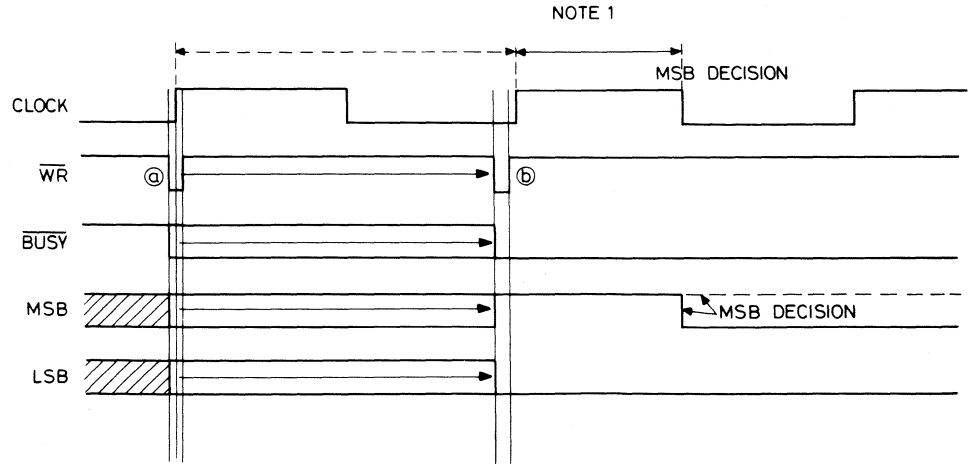


FIG. 2b (EXPANDED INSET)

6554

Fig. 2 ZN447 TIMING DIAGRAMS

The converter is cleared by a low-going CONVERT pulse, which sets the most significant bit and resets all the other bits and the $\overline{\text{BUSY}}$ flag. Whilst the CONVERT input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited.

After the CONVERT input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The CONVERT pulse can be as short as 200ns; however the MSB must be allowed to settle for at least 550ns before the MSB decision is made. To ensure that this criterion is met even with short CONVERT pulses the converter waits, after the CONVERT input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 550ns at maximum clock frequency. The CONVERT input is not locked out during a conversion and if it is pulsed low at any time the conversion will restart.

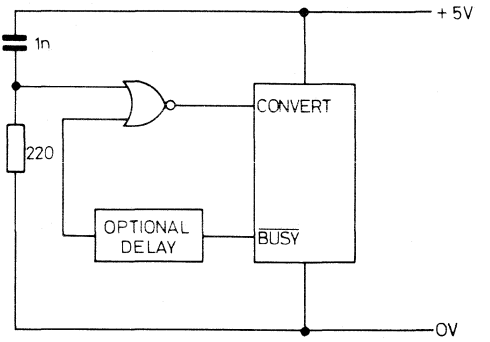
The $\overline{\text{BUSY}}$ output goes high at the end of a conversion indicating data valid. Note that if the three-state data outputs are enabled during a conversion then valid data will be available at the outputs on the rising edge of the $\overline{\text{BUSY}}$ signal. If, however the outputs are not enabled until after $\overline{\text{BUSY}}$ goes high then the data will be subject to the propagation delay of the three-state buffers. (See under DATA OUTPUTS).

CONTINUOUS CONVERSION

If a free-running conversion is required then the converter can be made to cycle by inverting the BUSY output and feeding it to the CONVERT input. To ensure that the converter starts reliably after power up an inital start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied, as shown in figure 3a.

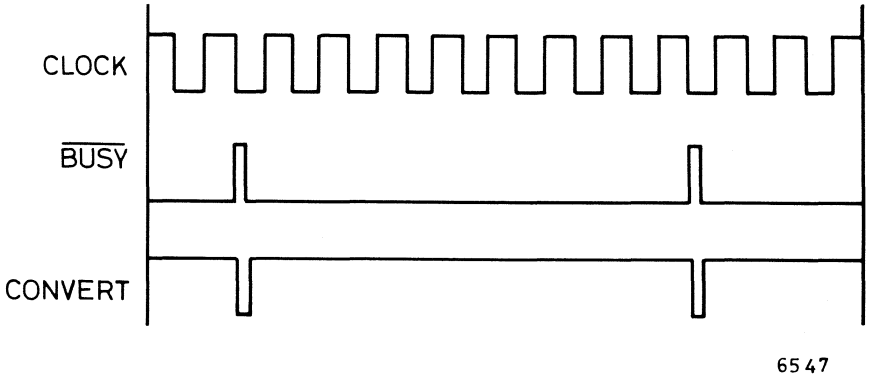
The ADC will complete a conversion on every eighth clock pulse, with the $\overline{\text{BUSY}}$ output going high for a period determined by the propagation delay of the NOR gate, during which time the data can be stored in a latch. The time available for storing the data can be increased by inserting delays into the inverter path.

A timing diagram for the continuous conversion mode is shown in figure 3b.



6546

Fig. 3a CIRCUIT FOR CONTINUOUS CONVERSION



6547

Fig. 3b TIMING FOR CONTINUOUS CONVERSION

As the $\overline{BUSY}$ output uses a passive pullup the rise time of this output depends on the RC time constant of the pullup resistor and load capacitance. In the continuous conversion mode the use of a 4k7 external pullup resistor is recommended to reduce the risetime and ensure that a logic 1 level is reached.

DATA OUTPUTS

The data outputs are provided with 3-state buffers to allow connection to a commmon data bus. An equivalent circuit is shown in figure 4. Whilst the $\overline{RD}$ input is high both ouput transistors are turned off and the ZN447 presents only a high impedance load to the bus. When $\overline{RD}$ is low the data ouputs will assume the logic states present at the outputs of the successive approximation register.

A test circuit and timing diagram for the output enable/disable delays are given in figure 5.

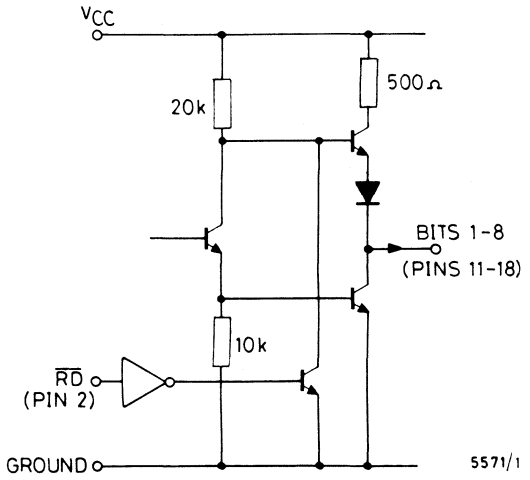


Fig. 4 DATA OUTPUT

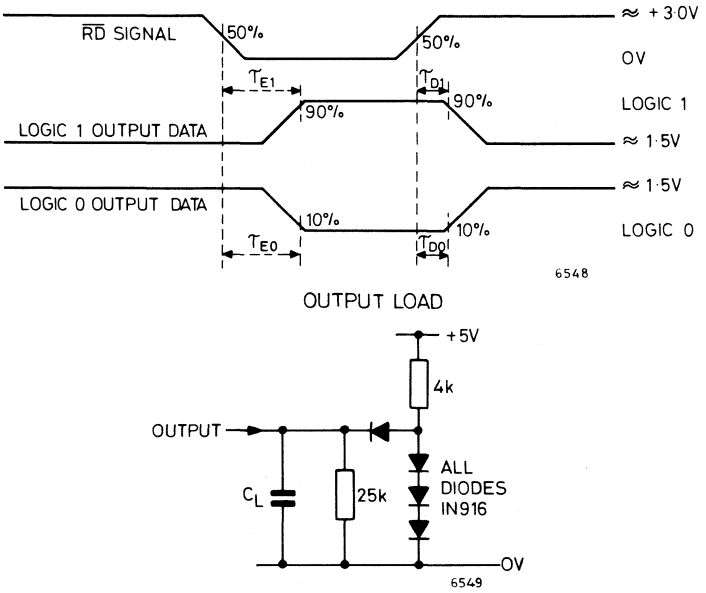


Fig. 5 OUTPUT ENABLE/DISABLE DELAYS

$\overline{\text{BUSY}}$ OUTPUT

The $\overline{\text{BUSY}}$ output, shown in figure 6, utilises a passive pullup for CMOS/TTL compatibility. This also allows up to four $\overline{\text{BUSY}}$ outputs to be wire-ANDed together to form a common interrupt line.

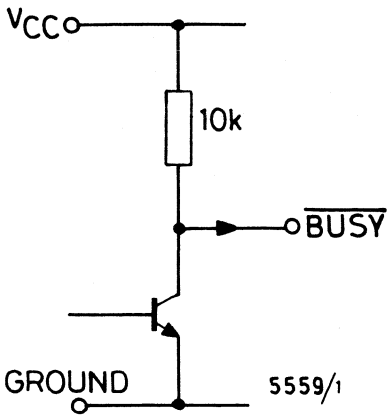


Fig. 6 $\overline{\text{BUSY}}$ OUTPUT

ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 3 and ground as shown in figure 7a. A graph of typical oscillator frequency versus capacitance is given in figure 8. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in figure 7b. For optimum accuracy and stability of the oscillator frequency without trimming the use of a crystal or ceramic resonator is recommended, as shown in figure 7c. The final option is to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate, as shown in figure 7d.

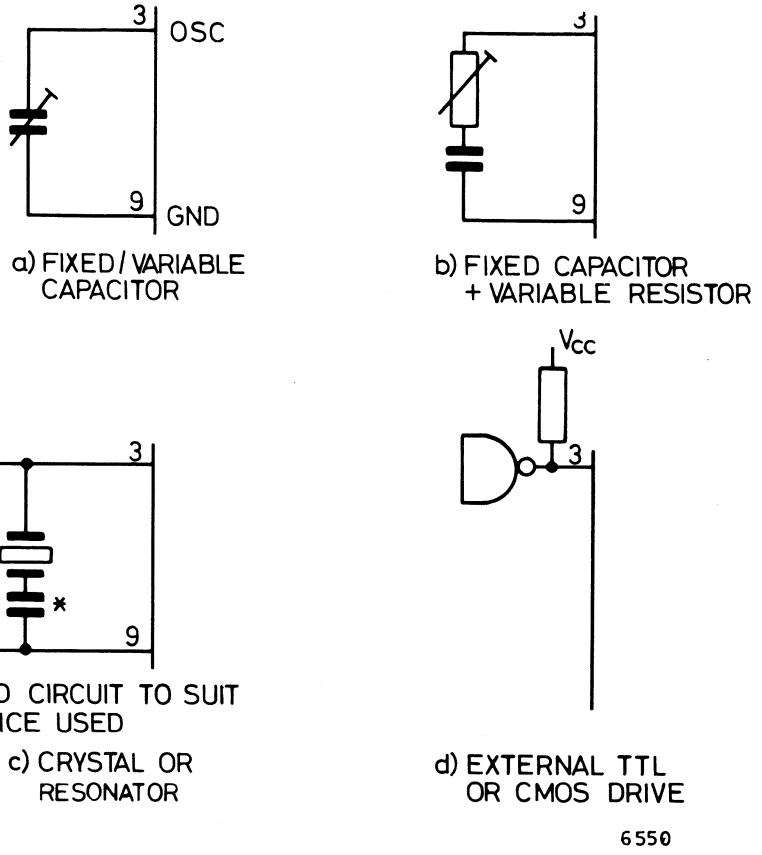


Fig. 7 CLOCK CIRCUIT EXTERNAL COMPONENTS

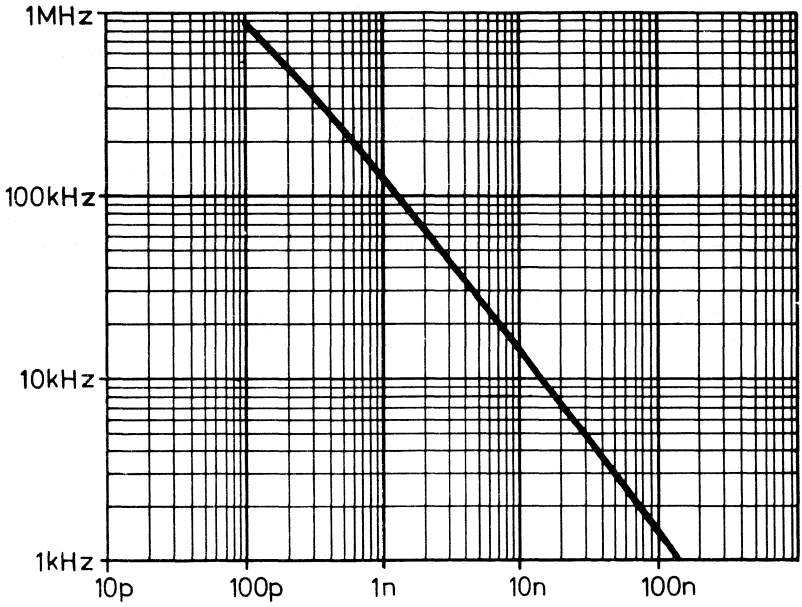


Fig. 8 TYPICAL CLOCK FREQUENCY vs. C_{CR} (R_{CK} = 0)

ANALOGUE CIRCUITS

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in figure 9. Each element is connected to either OV or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D to A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8 μV/°C) the effect on accuracy will be negligible.

The D to A output range can be considered to be $0 - V_{REF\ IN}$ through an output resistance R (4k).

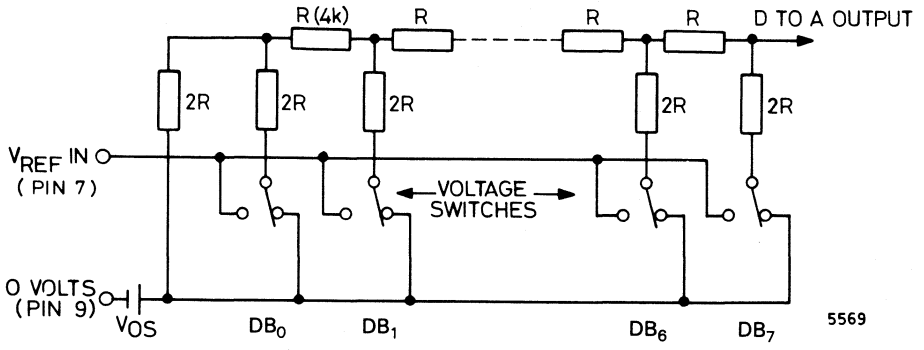


Fig. 9 R2-R LADDER NETWORK

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (figure 10). A resistor (R_{REF}) should be connected between pins 8 and 10.

The recommmended value of 390Ω will supply a nominal reference current of (5.0−2.5) /0.39 = 6.4mA. A stabilising/decoupling capacitor, C_{REF} (4 μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (Pin 8) is connected to $V_{REF\ IN}$ (Pin 7).

Up to five ZN447s may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

(b) External Reference

If required an external reference voltage in the range +1.5 to +3.0 volts may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

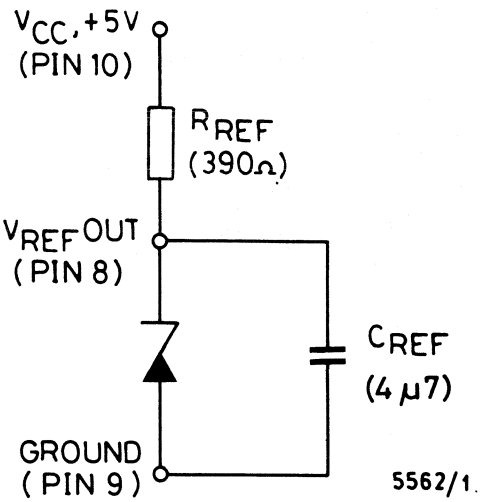


Fig. 10 INTERNAL VOLTAGE REFERENCE

RATIOMETRIC OPERATION
If the output from a transducer varies with its supply then an external reference for the ZN447 should be derived from the same supply. The external reference can vary from +1.5 volts to +3.0 volts. The ZN447 will operate if $V_{REF\ IN}$ is less than +1.5 volts but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR
The ZN447 contains a fast comparator, the equivalent input circuit of which is shown in figure 11. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150 µA and need not be well stabilised it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output.

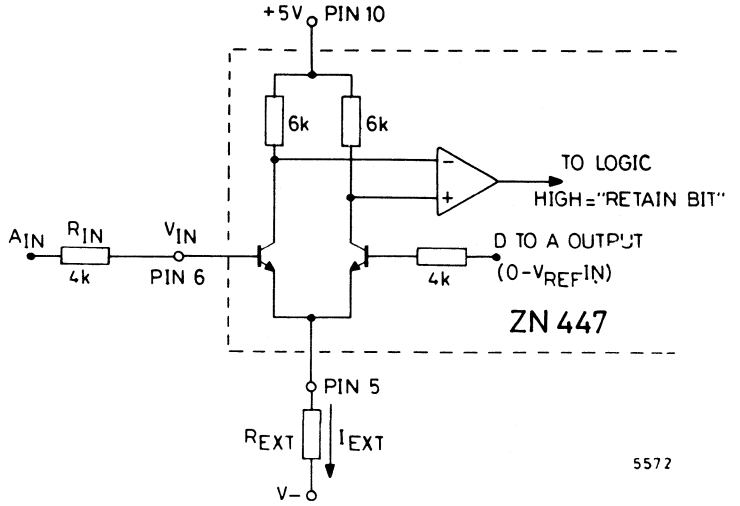


Fig. 11 COMPARATOR EQUIVALENT CIRCUIT

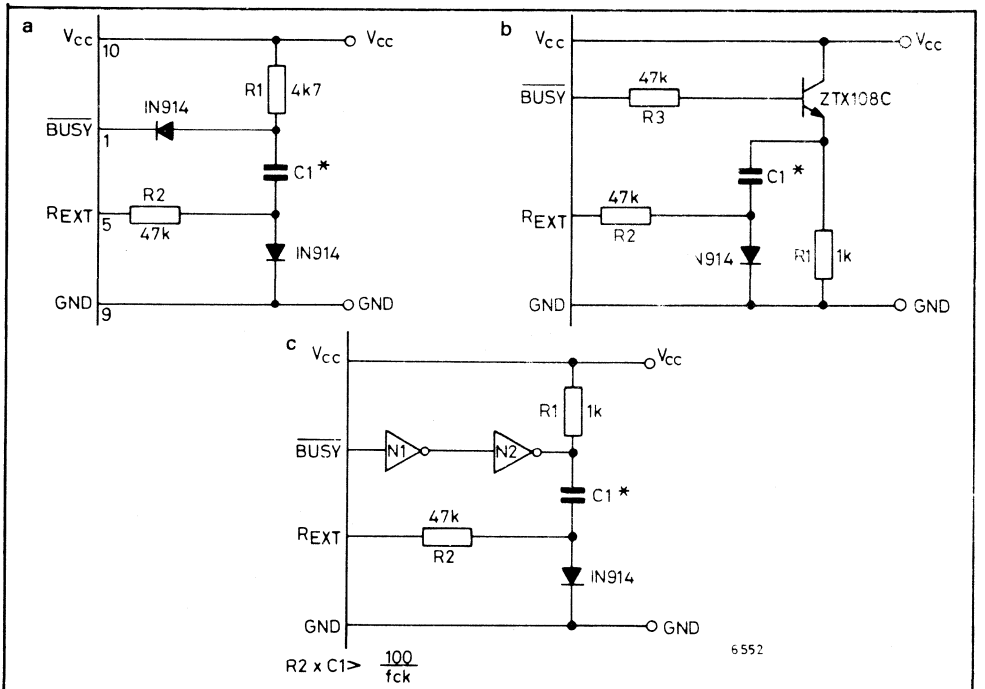


Fig. 12 DIODE PUMP CIRCUITS TO SUPPLY COMPARATOR TAIL CURRENT

Several suitable circuits are shown in figure 12. The principle of operation is the same in each case. Whilst the $\overline{BUSY}$ output is high capacitor C1 is charged to about 4.—4.5 volts. During a conversion the $\overline{BUSY}$ output goes low and the upper end of C1 is thus also pulled low. The lower end of C1 therefore applies about —4V to R2, thus providing the tail current for the comparator. The time constant R2. C1 is chosen according to the clock frequency so that droop of the capacitor voltage is not significant during a conversion.

The constraint on using this type of circuit is that C1 must be recharged whilst the $\overline{BUSY}$ output is high. If the $\overline{BUSY}$ output is high for greater than one converter clock period then the circuit of figure 12a will suffice. If this is not the case, for example, in the continuous conversion mode, then the circuits of figures 12b and 12c are recommended, since these can pump more current into the capacitor.

Where several ZN447s are used in a system the self-oscillating diode pump circuit of figure 13 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistor values for different supply voltages is given in table 1.

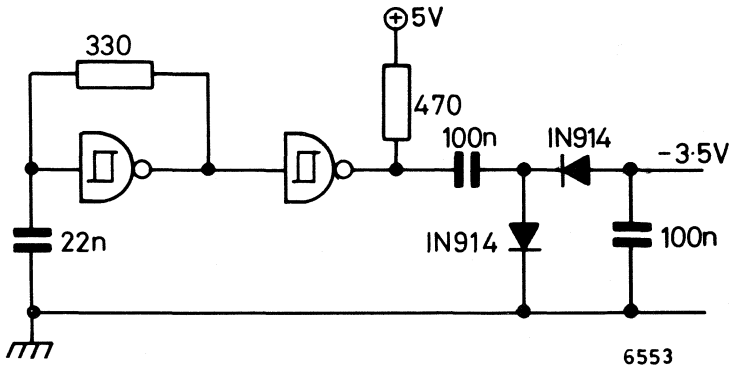


Fig. 13 DIODE PUMP CIRCUIT TO SUPPLY COMPARATOR TAIL CURRENT FOR UP TO FIVE ZN447's.

V– (Volts)	R_{EXT} (k~)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

ANALOGUE INPUT RANGES

The basic connection of the ZN447 shown in figure 14 has an analogue input range 0 to $V_{REF\ IN}$ which, in some applications, may be made available from previous signal conditioning /scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by offsetting the analogue input range so that the comparator always sees a positive input voltage.

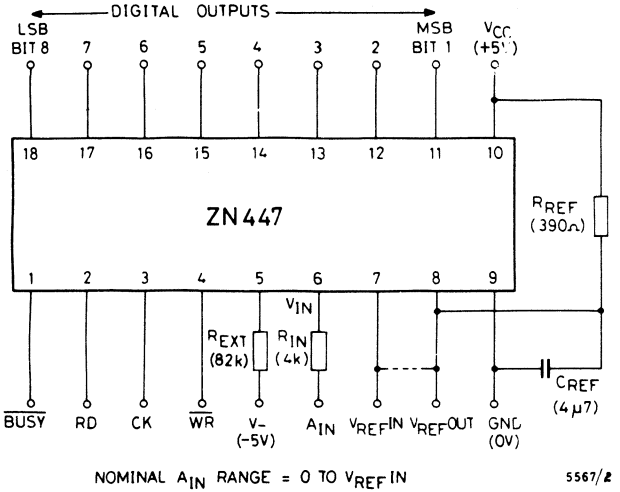


Fig. 14 EXTERNAL COMPONENTS FOR BASIC OPERATION

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in figure 15.
The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input (A_{IN}) is at full scale.

The resulting full scale range is given by: $A_{IN}\ FS = (1 + \frac{R1}{R2})$, $V_{REF\ IN} = G.\ V_{REF\ IN}$.

To match the ladder resistance R1/R2 (R_{IN}) = 4k.

The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ k, $R_2 = \frac{4G}{G-1}$ k.

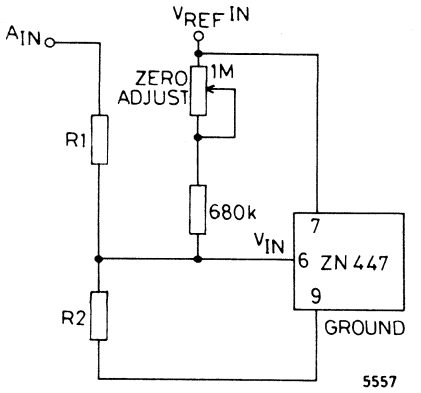


Fig. 15 GENERAL UNIPOLAR INPUT CONNECTIONS

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

INPUT RANGE	G	R_1	R_2
+5V	2	8k	8k
+10V	4	16k	5.33k

GAIN ADJUSTMENT
Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least $\pm$ 5% of its nominal value is suggested.

ZERO ADJUSTMENTS
Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to 1½LSB with a 2.56 volt reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of + ½LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1½ times $V_{REF\ IN}$.

Practical circuit values for +5V and +10V input ranges are given in figure 16 which incorporates both zero and gain adjustments.

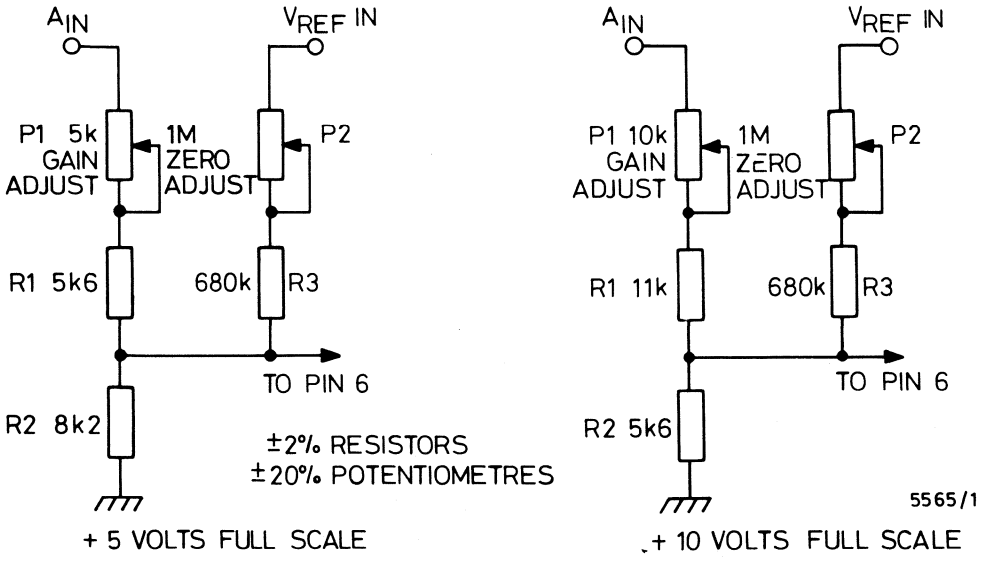


Fig. 16 UNIPOLAR OPERATION COMPONENT VALUES

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous convert pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full scale minus 1½ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply ½ LSB to A_{IN} and adjust zero until Bit 8 just flickers between 0 and 1 with all other bits at 0.

UNIPOLAR SETTING–UP POINTS

INPUT RANGE, +FS	½ LSB	FS–1½ LSB
+5V	9.8mV	4.9797 volts
+10V	19.5mV	9.9414 volts

$1\ LSB = \frac{FS}{256}$

UNIPOLAR LOGIC CODING

ANALOGUE INPUT (A_{IN}) (NOMINAL CODE CENTRE VALUE)	OUTPUT CODE (BINARY)
FS–1 LSB	11111111
FS–2 LSB	11111110
¾ FS	11000000
½ FS + 1 LSB	10000001
½ FS	10000000
½ FS–1 LSB	01111111
¼ FS	01000000
1 LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN447 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (figure 17).

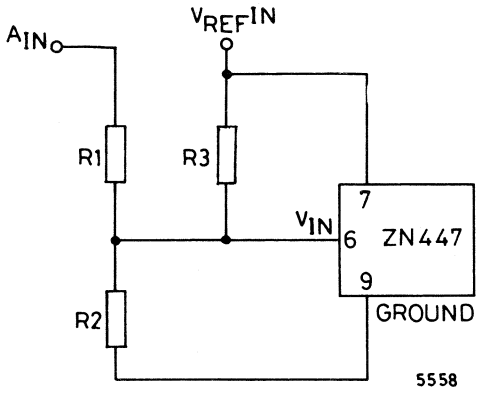


Fig. 17 BASIC BIPOLAR INPUT CONNECTION

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full scale range is $\pm$ G. $V_{REF\ IN}$ then $R_1 = (G-1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance $R_1/R_2/R_3$ ($= R_{IN}$) = 4k.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8$ Gk, $R_2 = 8G/(G-1)$k, $R_3 = 8$k.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 8$k and $R_2 = \infty$.

Assuming the $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for $\pm$ 5V and $\pm$ 10V input ranges are given in the following table.

INPUT RANGE	G	R_1	R_2	R_3
$\pm$5V	2	16k	16k	8k
$\pm$10V	4	32k	10.66k	8k

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.
Practical circuit realisations are given in figure 18.

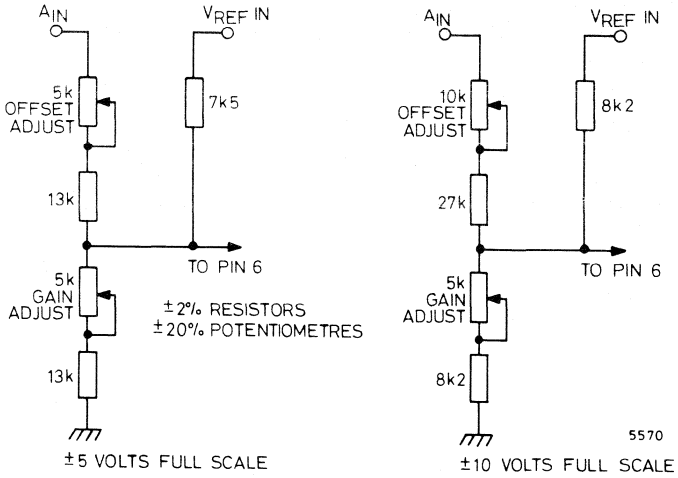


Fig. 18 BIPOLAR OPERATION – COMPONENT VALUES

Note that in the ± 5V case R_3 has been chosen as 7.5 k (instead of 8.2 k) to obtain a more symmetrical range of adjustment using standard potentiometers.

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.
(ii) Apply – (FS – ½ LSB) to A_{IN} and adjust offset until the Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.
(iii) Apply + (FS – 1 ½ LSB) to A_{IN} and adjust gain until Bit 8 just flickers between 0 and 1 with all other bits at 1.
(iv) Repeat step (ii).

BIPOLAR SETTING – UP POINTS

INPUT RANGE, ± FS	–(FS – ½ LSB)	+ (FS – 1 ½ LSB)
±5V	–4.9805V	+4.9414V
±10V	–9.9609V	+9.8828V

1 LSB = $\frac{2FS}{256}$

ZN447/8/9

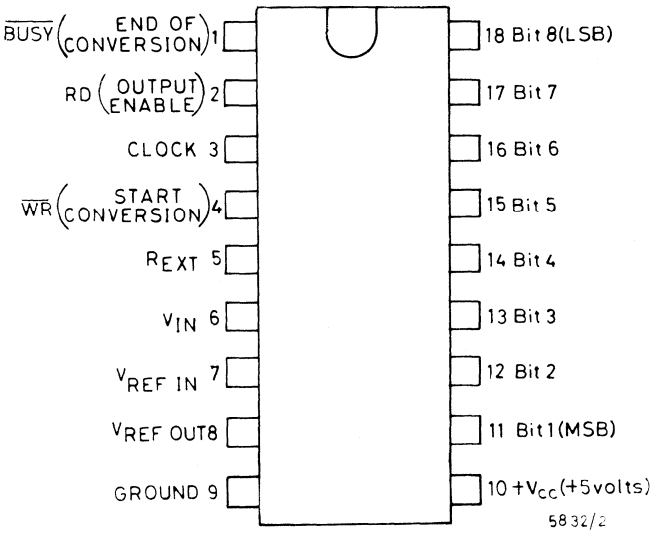
BIPOLAR LOGIC CODING

ANALOGUE INPUT (A_{IN}) (NOMINAL CODE CENTRE VALUE)	OUTPUT CODE (OFFSET BINARY)
+ (FS − 1 LSB)	11111111
+ (FS − 2 LSB)	11111110
+ ½ FS	11000000
+ 1 LSB	10000001
0	10000000
− 1 LSB	01111111
− ½ FS	01000000
− (FS − 1 LSB)	00000001
− FS	00000000

ORDERING INFORMATION

TYPE	LINEARITY (LSB)	OPERATING TEMPERATURE RANGE	PACKAGE
ZN447E	¼	0°C to + 70°C	Moulded
ZN447J	¼	−55°C to + 125°C	Ceramic
ZN448E	½	0°C to + 70°C	Moulded
ZN448J	½	−55°C to + 125°C	Ceramic
ZN449E	1	0°C to + 70°C	Moulded
ZN449J	1	−55°C to + 125°C	Ceramic

PIN CONNECTIONS



FERRANTI semiconductors

ZN450E
ZN450CJ

Single Chip 3½ Digit DVM IC

FEATURES

- **199.9 mV full-scale reading**
- **Digital Auto-zero with guaranteed zero reading for 0V input**
- **True polarity at zero for null detection**
- **True differential inputs**
- **Direct drive of Liquid Crystal Display**
- **On-chip clock and precision reference**
- **Underrange/overrange indication**
- **Low power consumption, less than 35 mW**
- **Wide supply voltage range, single supply rail**
- **No external active circuits required**

DESCRIPTION

The ZN450 is a complete digital voltmeter fabricated on a monolithic chip and requires only ten external, passive components for operation. A novel charge-balancing conversion technique ensures good linearity. The auto-zero function is completely digital in operation, thus obviating the need for a capacitor to store the error voltage. This versatile I.C. can be used as the basis not only for digital voltmeters and multimeters but also for other instruments such as digital thermometers.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	−0.5 to +7 volts
Maximum Voltage, all other inputs	−0.5 to (V_{CC} +0.5) volts
Operating Temperature range	0 to +70°C
Storage Temperature Range	−55°C to +125°C

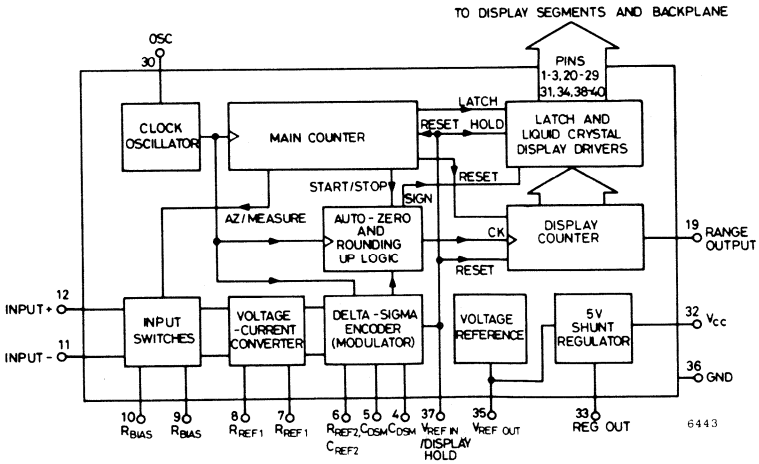


Fig. 1 – ZN450 SYSTEM DIAGRAM

Parameter	Min.	Typ.	Max.	Units	Conditions
Full-scale Reading	−1999	—	+1999		
Zero Reading	−000.0	±000.0	+000.0	Digital Reading	$V_{IN}=0$, $V_{FS}=200\,mV$
Rollover Error	−2	0	+2	Count	$-V_{IN}=+V_{IN}=\pm 200\,mV$ conversion time ⩾0.5 sec.
Linearity	−1	0	+1	Count	$V_{FS}=200\,mV$ conversion time ⩾0.5 sec.
Common Mode Range	1.8	—	3.8	Volts	
Common Mode Rejection	—	120	—	μV/V	
Supply Rejection	—	100	—	μV/V	
Input Offset Current	—	0.1	1	nA	Input bias resistors matched to 0.1%
Input Resistance	7	10	13	MΩ	With 10 M input resistors
Zero Temperature Coefficient	—	—	1	μV/°C	
Full-scale Temperature Coefficient	Determined by tracking of external resistors				Ref T.C. = 0 ppm/°C
Oscillator Frequency Range	—	—	300	kHz	
Conversion Time (48000 Oscillator Periods)	0.25	—	—	Seconds	
VOLTAGE REFERENCE Output Voltage	1.26	1.3	1.35	Volts	
Temperature Coefficient	—	50	80	ppm/°C	
Knee Current	—	—	150	μA	
Maximum Sink Current	1	2	—	mA	
SUPPLY VOLTAGE (a) Direct (b) Using on-chip Shunt Regulator (c) Using external NPN transistor (d) Using two transistor regulator	 4.5 6.0 6.5 5.5	 5 — — —	 5.5 — — —	 Volts Volts Volts Volts	
Supply Current	—	4	6.5	mA	
SHUNT REGULATOR Output Voltage Sink Current	 4.5 —	 5 —	 5.5 15	 Volts mA	
DISPLAY OUTPUTS Peak Voltage	—	$\pm V_{CC}$	—		
D.C. Component	—	—	±25	mV	
Backplane Frequency	—	$\frac{1}{2000}$	—	Oscillator Frequency	

GENERAL DESCRIPTION

The ZN450 utilises a charge-balancing conversion principle, which offers a number of advantages over the more common dual-slope integration method.

These include a fixed conversion time which is independent of the analogue input voltage, completely digital auto-zero and inherently bipolar operation. Linearity is also extremely good over the entire input voltage range, unlike some dual slope designs where stray capacitance can cause problems around zero.

The conversion time of the ZN450 is divided into two periods, measure and auto-zero, unlike the dual-slope system which has three distinct phases, signal integrate, reference integrate and auto-zero.

The heart of the ZN450 is the delta-sigma encoder, a simplified circuit of which is shown in figure 2.

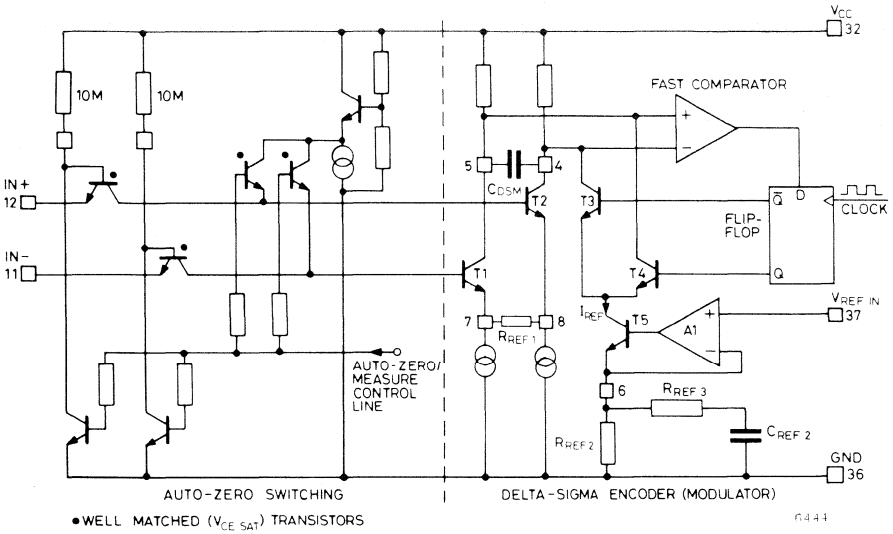


Fig. 2 – INPUT SWITCHING AND DELTA-SIGMA ENCODER

The delta-sigma encoder of the ZN450 consists of a voltage-current converter comprising T1 and T2, a reference current generator A1/T5 and a feedback loop containing a fast comparator, D-type flip-flop and current switches T3 and T4. These can switch a current $I_{REF} = \frac{V_{REF}}{R_{REF2}}$ into the collector circuit of either T1 or T2, depending on the state of the flip-flop.

The polarity of the voltage across capacitor C_{DSM} is monitored by the comparator, whose output is sampled on every clock pulse by the flip-flop. The outputs of the flip-flop switch I_{REF} into the collector circuit of either T1 or T2 so as to oppose the existing voltage on C_{DSM} i.e. to maintain the average charge acquired by C_{DSM} at zero, thus keeping the circuit in equilibrium.

Assuming perfect symmetry in the circuit, with zero volts applied between the bases of T_1 and T_2 their collector currents will be equal, and the only charge acquired by C_{DSM} will be that put on it by I_{REF}. The flip-flop will thus change state on every clock pulse so that C_{DSM} will alternately acquire charge quanta of $+I_{REF}T_C$ and $-I_{REF}T_C$ (where T_C is the clock period) and the nett charge acquired will be zero. The output of the flip-flop will thus be a square-wave with a 50% duty cycle.

During the measurement phase the voltage to be measured is applied between the bases of T1 and T2 and is converted into a current $I_{IN} = \frac{V_{IN}}{R_{REF1}}$ flowing in R_{REF1}. This produces a difference current $2I_{IN}$ in the collector currents of T1 and T2, so that the charge acquired by C_{DSM} is no longer equal and opposite ($\pm I_{REF}$) but is now ($I_{REF} - 2I_{IN}$) T_C when T_4 is turned on and ($-I_{REF} - 2I_{IN}$) T_C when T3 is turned on.

In order to maintain equilibrium the flip-flop will now no longer change state on every clock pulse but will remain in one state for a longer period than it remains in the opposite state.

$$\text{i.e. } N_1T_C(I_{REF} - 2I_{IN}) + (N - N_1)T_C(-I_{REF} - 2I_{IN}) = 0$$

where N_1 is the number of clock pulses for which the flip-flop output is a '1' and N is the total number of clock pulses over which the measurement is made and assuming N is so large that quantising error can be ignored.

$$\text{Thus } N_1(I_{REF} - 2I_{IN}) = (N - N_1)(I_{REF} + 2I_{IN})$$

At this point it is perhaps worth noting that the DSM saturates (0% or 100% duty cycle) when I_{IN} is plus or minus $\frac{I_{REF}}{2}$

In order to provide an overload margin for series mode rejection the ZN450's DSM operates with a peak duty-cycle of nominally 10% for minus full-scale and 90% for plus full-scale ($I_{IN} = \pm\frac{2}{5}I_{REF}$) giving an overload margin of 25% of the full-scale input voltage.

$$\text{Now } \frac{2N_1 - N}{N} = \frac{2I_{IN}}{I_{REF}} \quad \text{i.e. } N_1 - \frac{N}{2} = \frac{NI_{IN}}{I_{REF}} = \frac{NV_{IN}\,R_{REF2}}{R_{REF1}\,V_{REF}}$$

What this means is that an up counter preset to $-\frac{N}{2}$ and allowed to count N_1 will accumulate a number proportional to V_{IN}, assuming N, R_{REF1}, R_{REF2} and V_{REF} are fixed. By suitable choice of these parameters $N_1 - \frac{N}{2}$ can be made directly equal to V_{IN} in volts or millivolts. Furthermore, by making the preset number greater or less than $\frac{N}{2}$ in proportion to any zero error in the system it is possible to provide a digital auto-zero.

The ZN450 indicates positive overrange at a count of +2000 when the duty cycle is 90% and $I_{IN} = \frac{2}{5}I_{REF}$. The required value of N can thus be obtained by substituting the overrange reading of 2000 for $N_1 - \frac{N}{2}$ and the corresponding value of $\frac{2}{5}$. for $\frac{I_{IN}}{I_{REF}}$, $2000 = \frac{2N}{5}$, N = 5000.

In fact the display counter is preceded by a ÷4 stage which is part of the auto-zero logic so the actual measurement period must be 20,000 clock periods to give a maximum of 5000 pulses at the display counter.

The display counter of the ZN450 can count from −5000 to +5000. It is preset to nominally −2500 during the auto-zero phase by allowing it to count from −5000 to −2500, as explained below.

Auto-Zero

Due to offsets and component mismatching in the delta-sigma encoder the displayed count accumulated for zero input voltage will not be zero. In order to remove this error and give a true zero reading for 0V input the ZN450 incorporates an auto-zero facility. This is completely digital in operation and there is no need to store the error as an analogue voltage on a capacitor, as is the case with some dual slope-designs. Furthermore the conversion period of the ZN450 comprises two well-defined phases, measure and auto-zero, unlike dual-slope DVMs which have signal integrate, reference integrate and auto-zero phases.

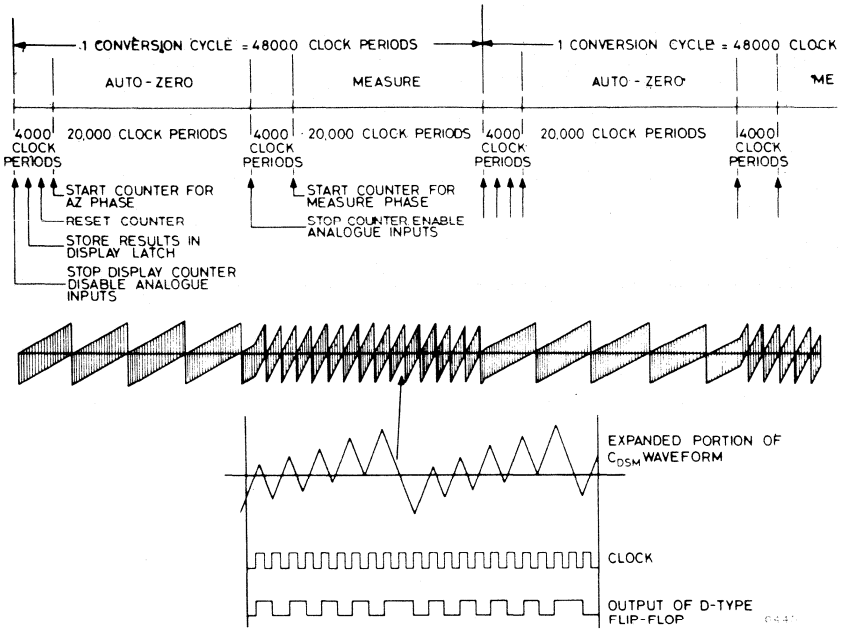


Fig. 3 – TIMING DIAGRAM OF ZN450

A timing diagram of the ZN450 is shown in figure 3. Its duration is 48000 clock periods and its two principal components are the measurement phase and the auto-zero phase which each occupy 20,000 clock periods. Each phase is separated by a space of 4000 clock periods to allow the input switches to settle. This also illustrates another advantage of the charge balancing conversion technique. Since the delta sigma encoder can run continuously without saturating and its average duty-cycle is always a measure of the input voltage, it is possible to allow the input switches to settle in this way before starting a measurement by activating the system counters.

Contrast this with the dual-slope DVM where the integrator capacitor begins to accumulate charge immediately the input voltage is connected. The system counter must start at the precise instant that the input voltage is connected which means that the input switches must be fast and noise-free. Furthermore termination of the measurement is determined by the comparator accurately detecting a single zero-crossing, so noise in the comparator or from other sources can cause errors. In the charge balancing DVM the comparator detects many zero crossings and noise tends to be integrated out.

Operation of the auto-zero system is best understood by considering what happens when an auto-zero phase is followed by a measurement with zero volts input. During the auto-zero phase the inputs of the DSM are disconnected from the analogue inputs and shorted to a point within common-mode range of the DVM. The counter is reset to -5000 and the system is allowed to run for 20,000 clock periods, but with the DSM output inverted. This means that the number of clock pulses counted will be, not N_1 but $(N - N_1)$. During the subsequent measurement with zero input voltage N_1 pulses will be counted, so that the total count will be N, i.e. 5000. The display counter will thus have counted from -5000 up to zero and zero will be displayed.

Due to the quantising error inherent in any digital measurement it is possible that the result of the measurement with zero input could differ from the result of the auto-zero by 1 count, thus giving rise to a zero error of ±1 digit. To avoid this problem the ZN450 incorporates two guard bits in the form of a ÷4 stage and rounding up logic preceding the display counter. This means that although the display resolution is 1 part in ±2000 the resolution of the measurement is four times better. Any zero error in the two (non-displayed) guard bits will not appear in the display and the logic also subdivides the zero state into +0000 and −0000 for true polarity indication.

As an additional benefit flicker in the last digit of the display is minimised.

Input Resistance

The input resistance of the ZN450 is determined by the two 10M bias resistors, the value of R_{REF1}, and h_{fe} and r_e of T1 and T2.

An equivalent input circuit is shown in figure 4. The input resistance comprises h_{fe} ($R_{REF1} + 2_{re}$) in parallel with 20M due to the two 10M input resistors.

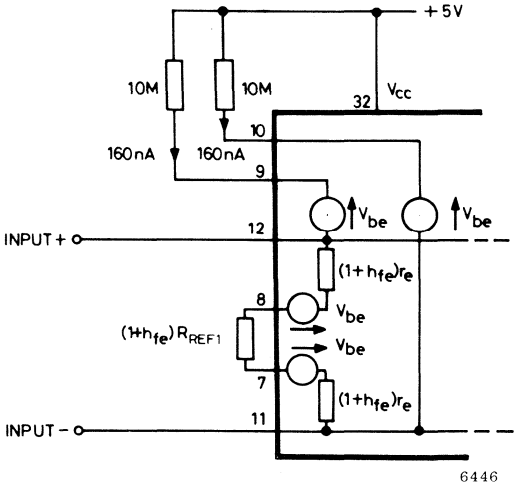


Fig. 4 – EQUIVALENT INPUT CIRCUIT OF ZN450

The h_{fe} of T1 and T2 is typically about 100 and r_e is around 2.5k, therefore:

$$R_{IN} = \frac{100\,(R_{REF1} + 5k) \times 20M}{100\,(R_{REF1} + 5k) + 20M}$$

For 200 mV full-scale, when $R_{REF1} = 200k$ the input resistance is around 10M.

Reference Loop and Supply Regulator

The reference current defining loop is shown in more detail in figure 5.

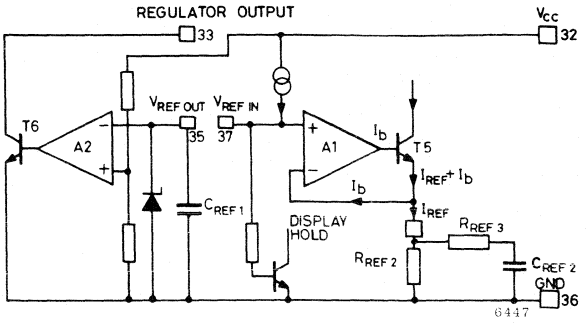


Fig. 5 – REFERENCE CURRENT LOOP AND SUPPLY REGULATOR

A reference input voltage applied to the non-inverting input of A1 causes the output of A1 to bias T5 such that the inverting input of A1 assumes the same potential and a current $\frac{V_{REF\ IN}}{R_{REF2}}$ flows in R_{REF2}. By making the input bias current of A1 the same as the base current of T5 this base current flows into the inverting input of A1 instead of through R_{REF2}. The reference current flowing in the collector of T5 is therefore almost identical to the current flowing in R_{REF2}. The reference loop is stabilized by C_{REF2} and R_{REF3}.

A highly stable on-chip bandgap reference of approximately 1.28V is provided and this may be used by linking $V_{REF\ OUT}$ to $V_{REF\ IN}$ when the reference will be biased on by the 150 μA current source connected to the non-inverting input of A1. The on-chip reference is stabilised by C_{REF1}. The on-chip reference also provides the reference voltage for the on-chip supply regulator A2. This compares V_{REF} against $\frac{V_{CC}}{4}$ and controls V_{CC} with transistor T6 such that the two are kept equal, i.e. $V_{CC} \simeq 5V$.

The supply regulator can be configured as a shunt or series regulator using only a few external components.

If $V_{REF\ OUT}$ is not connected to $V_{REF\ IN}$ but supply regulation is still required then the on-chip reference must be biased on by a 22k resistor to V_{CC}.

Setting Full-Scale Range

The described equation previously arrived at for the charge-balancing converter was:

$$\frac{NV_{IN}.R_{REF2}}{V_{REF}.R_{REF1}} = N_1 - \frac{N}{2}$$

i.e. displayed reading $= \frac{NV_{IN}.R_{REF2}}{V_{REF}.R_{REF1}}$

and since N = 5000

Displayed reading $= 5{,}000\ \frac{V_{IN}.R_{REF2}}{V_{REF}.R_{REF1}}$

or, substituting the maximum reading of ± 1999 and rearranging again:

V_{IN}(full-scale) $= \frac{\pm 1999\,V_{REF}.R_{REF1}}{5000.R_{REF2}}$

$\simeq \frac{\pm 0.4\,V_{REF}.R_{REF1}}{R_{REF2}}$

These equations are in fact not exact since they do not take account of the reference amplifier offset

voltage, which is typically ±5mV. This offset means that I_{REF} is not precisely $\frac{V_{REF}}{R_{REF2}}$. r_e of T1 and T2 in the voltage-current converter also appears in series with R_{REF2} (typically 5k). In practice this is not a problem since the tolerance of the on-chip reference means that a calibration adjustment must be provided anyway.

Using the on-chip reference voltage of 1.26 – 1.35 volts the recommended component values for a full-scale reading of 199.9mV would be $R_{REF1} = 200k$, $R_{REF2} = 500k$ (min.), 520k (max.). Allowing for the use of 2% tolerance components for R_{REF1} and R_{REF2} an adequate adjustment range for calibration purposes will be provided if R_{REF2} is made up of a 470k resistor in series with a 100k multiturn trimmer. Full-scale ranges less than 200mV can be accommodated by reducing the value of R_{REF1}, thus producing the same full-scale input current for a smaller input voltage. The limitations on the minimum value of R_{REF1} are caused by non-linearity in the voltage-current converter, offsets in the auto-zero switches, and the fact that r_e becomes a much larger proportion of R_{REF1}. These factors place a practical limit of about 20k on R_{REF1}.

Similarly full-scale ranges greater than ±200mV can be accommodated by the value of R_{REF1}. The maximum input voltage that can be applied is limited by the common-mode range of the differential inputs. Provided the common-mode range of either input terminal is not exceeded the maximum differential voltage that can be applied between the inputs is about ±2V.

The full-scale range can also be adjusted by varying R_{REF2} which determines the reference current, and indeed placing a preset in series with R_{REF2} is the recommended method of calibration.

I_{REF} can also be varied by using an adjustable external reference voltage instead of the internal reference, which makes ratiometric operation possible.

The minimum value of I_{REF} is limited to about 3μA since above this value the voltage-current converter becomes non-linear. The maximum value of I_{REF} is not quite so well defined as it is determined by deterioration in the performance of current switches T3 and T4 at low collector currents. The minimum useable value of I_{REF} is typically 500nA. This means that the upper and lower limits are $\frac{V_{REF}}{500\,nA}$ and $\frac{V_{REF}}{3\,\mu A}$ respectively. The upper and lower limits on V_{REF} itself are determined by the common-mode range of the reference current amplifier A1 which is 1V to 1.5V. Ratiometric operation with a variable V_{REF} within these limits is possible provided that the upper or lower limit of I_{REF} is not exceeded.

Supply Voltage Options

The ZN450 is designed to be extremely flexible with regard to supply voltage and four power supply options are possible allowing operation over a wide range of supply voltages. These options are illustrated in figure 6.

The first option is to ignore the on-chip regulator and to connect an externally stabilised voltage of 4.5V to 5.5V direct to pin 32, for example a 5V logic supply.

For supply voltages greater than 6V the on-chip shunt regulator (pin 33) may be used by linking pins 32 and 33. When using the shunt regulator an external resistor must be placed in series with the supply to limit the regulator current as shown in figure 6b. The value of this resistor is given by:

$$R = \frac{V_{supply} - 5\,volts}{5}\left(k,\frac{V}{mA}\right)$$ which allows for the maximum 5mA current consumption of the I.C.

If the supply voltage is unstabilised then R should be calculated using the minimum supply voltage that will be encountered. The current drawn by this configuration increases with supply voltage as the shunt regulator sinks more current in order to maintain V_{CC} at 5V. The maximum allowable supply voltage is thus determined by the 15mA maximum rating of the shunt regulator, assuming very little current is drawn by the DVM circuitry, i.e.

$$V_{max} = 15(mA) \times R(k\Omega) + 5\,volts$$
$$= (3V_{min} - 10)\ volts$$

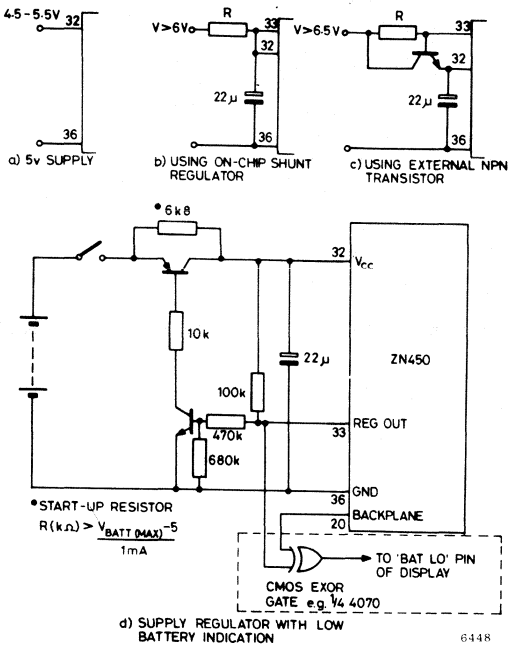


Fig. 6 – SUPPLY VOLTAGE OPTIONS

Since the current drawn by the shunt regulator increases with supply voltage this configuration is not recommended for battery operation where long battery life is a prime criterion, as the current drawn from a new battery could be up to three times the maximum current consumption of the DVM.

For battery operation a series regulator circuit is recommended which can be constructed using one or two external transistors controlled by pin 33. The simplest series regulator, shown in figure 6c, uses a single NPN transistor and allows operation down to about 6.5V. Current consumption of this circuit is the normal current consumption of the DVM plus the base current of the transistor.

The base resistor must be chosen such that it can supply sufficient base drive when the supply voltage is a minimum assuming

(a) Maximum DVM current of 6.5 mA

(b) Maximum shunt regulator voltage of 5.5V

(c) Minimum gain of the transistor

$$\text{Now base current } I_b \text{ (mA)} = \frac{V_{min} - V_{reg} - V_{be\,T1}}{R_b}$$

$$\text{required base current} = \frac{6.5\,mA}{h_{fe\,(min)}}$$

$$\text{Therefore } R_b(k\Omega) = \frac{(V_{min} - V_{reg} - V_{be\,T1}) \times h_{fe}}{6.5}$$

$$\simeq \frac{(V_{min} - 6) \times h_{fe}}{6.5}$$

Example. The circuit is to operate down to 6.5V with a transistor type whose minimum gain is 80

$$R_b = \frac{(6.5-6)\times 80}{6.5}$$

$$= 6.1k$$

Nearest value of 5k6 is used.

Although a great improvement on the shunt regulator, the circuit of figure 6c still does not achieve maximum battery life since V_{min} must always exceed the regulator voltage by $V_{be\ T1}$ plus the voltage drop across R_b.

For the ultimate in battery life the circuit of figure 6d is suggested. This allows operation down to voltages as low as $V_{reg} + V_{CE(sat)\ T1}$ and, as an added bonus, it automatically detects the end of useful battery life, i.e. the point at which the regulator ceases to function.

T1 is a PNP series regulator transistor controlled by pin 33 via T2, which provides the required signal inversion. During normal operation the voltage drop across R1 is small since the base current required by T2 is only a few hundred nanoamps, and the voltage at pin 33 is not much above the V_{be} of T2 (about 0.6V).

When the battery voltage drops to $V_{reg} + V_{CE(sat)\ T1}$ the voltage at the non-inverting input of the regulator amplifier will fall below V_{REF} and the shunt regulator output transistor will turn off causing the voltage at pin 33 to rise to about 80% of supply.

Pin 33 can conveniently be connected to a low battery indicator consisting of a CMOS EXOR gate, as shown in the dotted box. When pin 33 is low the output of the EXOR gate will be in phase with the backplane and the LO BAT indicator will be extinguished. When pin 33 is high the output will be out of phase with the backplane and LO BAT will be visible.

Oscillator Options

The on-chip oscillator of the ZN450 may be used with various configurations of external components, as shown in figure 7. It will operate with only an external capacitor, which may be fixed, or variable to adjust the oscillator frequency. Alternatively the frequency may be adjusted by placing a variable resistor in series with the capacitor. Graphs of oscillator frequency versus capacitor and resistor values are given in figure 8. If absolute accuracy of the oscillator frequency is required then a crystal or ceramic resonator may be used as the frequency determining element. By making the integration time a whole number of mains cycles a degree of mains interference rejection can be provided. For example a 100 kHz crystal gives an integration time of 200 ms which is 10 cycles at 50 Hz mains frequency or 12 cycles at 60 Hz, the total measurement interval being 480 ms or just over two conversions/second.

If mains interference is superimposed on the input signal it is important that its peak amplitude should be less than 25% of full-scale to avoid saturation of the DSM. If this is not the case then the ZN450 should be preceded by a lowpass filter to give additional mains rejection.

The final option is to overdrive the oscillator input from a TTL or CMOS gate, as shown in figure 7d.

In order to maintain an adequate drive to the comparator the value of C_{DSM} must also be changed in proportion to the oscillator period. A table of suitable values is given below.

Oscillator frequency	C_{DSM}	
(kHz)	Min.	Max.
50	200n	2μ
100	100n	1μ
150	68n	680n

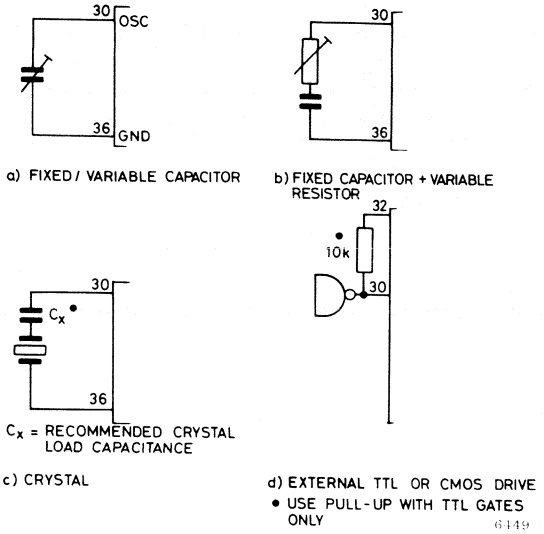


Fig. 7 – OSCILLATOR OPTIONS

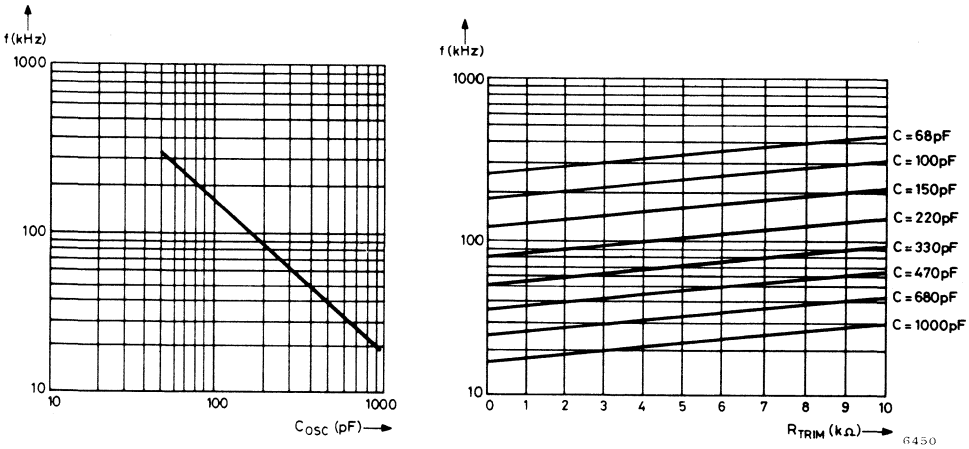


Fig. 8 – OSCILLATOR FREQUENCY vs EXTERNAL CAPACITOR AND RESISTOR

Range Output

To simplify the design of auto-ranging instruments, underrange and overrange detection circuits are provided in the ZN450. Overrange is indicated when the count exceeds 1999, whilst underrange is indicated for counts less than 150. This provides a degree of hysteresis to prevent the instrument jittering between ranges, which could occur if underrange was indicated at a count of 199 and there was a mismatch in the attenuators or other signal conditioning circuits.

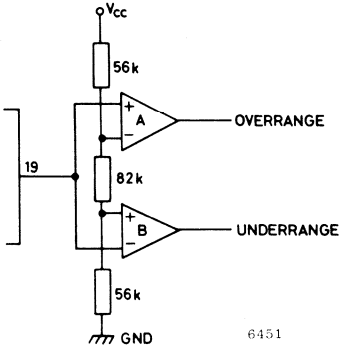
Because the pins of the ZN450 are fully utilised it is not possible to provide separate underrange and overrange pins, so a single three-state output is provided.

If the measurement is in range then pin 19 will be at $\frac{V_{CC}}{2} \pm 0.5V$ with a source resistance of approx. 40k.

For an overrange measurement pin 19 will go HIGH for 1000 clock pulses synchronous with the data store pulse at the end of the measurement. For an underrange measurement pin 19 will pulse LOW in a similar manner. In each case the output resistance is approx. 80k.

The range output can be fully decoded using a dual comparator, as shown in figure 9.

A visual overrange indication is also provided. In this condition the leading digit of the display shows a '1' whilst all other digits are blanked.



Range Output	Output A	Output B
Underrange (GND)	0	⎍
In Range ($\frac{1}{2}V_{CC}$)	0	0
Overrange (V_{CC})	⎍	0

Fig. 9 – DECODING THE RANGE OUTPUT

Display Hold

The reference input, pin 37, also doubles as a display hold pin. If this pin is grounded then the display will continue to show the results of the last valid measurement until pin 37 is released. Display hold also resets the system counters and a new measurement begins immediately display hold is released. The method of activating display hold depends on whether or not the on-chip reference and shunt regulator are being utilised.

If an external reference voltage is used (pins 35 and 37 not joined) then display hold can be activated by grounding pin 37 with a single-pole switch, transistor or open-collector logic gate, provided that the external reference is not required to supply other circuits. If the on-chip regulator is to be used then pin 35 must, of course, be biased up with an external 22k resistor so that V_{REF} can supply the reference voltage for the regulator. If the on-chip reference is used but the on-chip regulator is not then display hold can be activated in a similar manner by grounding the junction of pin 35 and pin 37.

However, since the on-chip reference also provides the reference voltage for the on-chip regulator pin 35 must not be grounded if the regulator is in use or the supply voltage will drop to zero. If the on-chip reference and shunt regulator are both used then pin 37 must be disconnected from pin 35 before it is grounded to activate display hold. This is illustrated in figure 10. As pin 37 normally supplies the bias current for the on-chip reference this must be provided by an external 22k resistor when these pins are not linked.

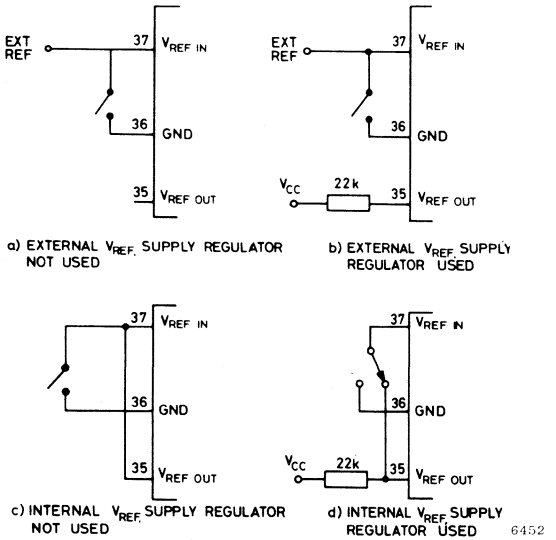


Fig. 10 – DISPLAY HOLD OPTIONS

Backplane Output

The backplane output normally provides a squarewave of the same frequency as, but 180° out of phase with, the active segment outputs. This provides the necessary a.c. drive to the L.C. display. By grounding the backplane output the a.c. drive to the segments may be inhibited and the segment outputs become normal active low (TRUE = 0) outputs. This facility is useful if the output data is to be used for some purpose other than display driving. An L.C. display should not be connected to the ZN450 in this condition as d.c. drive will eventually damage it.

Decimal Point Drive

The ZN450 provides all the outputs necessary to drive the segments of a 3½ digit liquid crystal display. However, in order to drive decimal points and annunciators such as low battery indicators, some external components are required. To turn on a decimal point it is necessary to provide it with a drive signal of the same frequency as, but 180° out of phase with, the backplane output. For driving a single, fixed decimal point, the simple inverter circuit of figure 11a can be used.

If more than one decimal point is to be selected then it is necessary for the unused decimal points to be switched off by arranging their drive waveforms to be in phase with the backplane output. This is simply achieved using exclusive OR gates as shown in figure 11b.

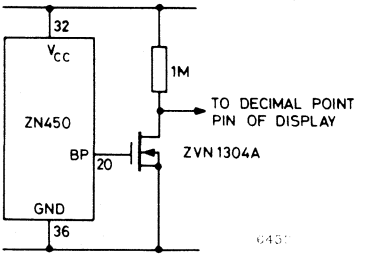
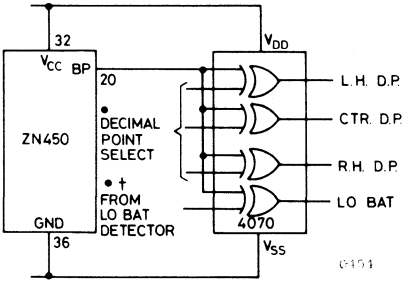


Fig. 11a – DRIVING A FIXED DECIMAL POINT



*Logic 1 = ON
Logic 0 = OFF
†See also figure 6

Fig. 11b – DECIMAL POINT SELECT AND 'LO BAT' INDICATOR DRIVE USING EXCLUSIVE OR GATES

A logic '1' on the input causes the output waveform to be out of phase with the backplane and the appropriate decimal point is activated. Conversely a logic '0' causes the output to be in phase with the backplane. A single 4070 CMOS quad-EXOR gate I.C. will provide the drive for the three decimal points of a 3½ digit liquid crystal display plus the drive to a low battery indicator. A suitable low battery detection circuit is shown in figure 6d.

External Components

A basic 200 mV DVM can be built using only ten external passive components, as shown in figure 12. In addition to these components it is good practice to include input protection resistors to limit the maximum input current to 50 mA in the event of an input overload. The resistance and power rating of these components depends on the maximum voltage against which the inputs are to be protected.

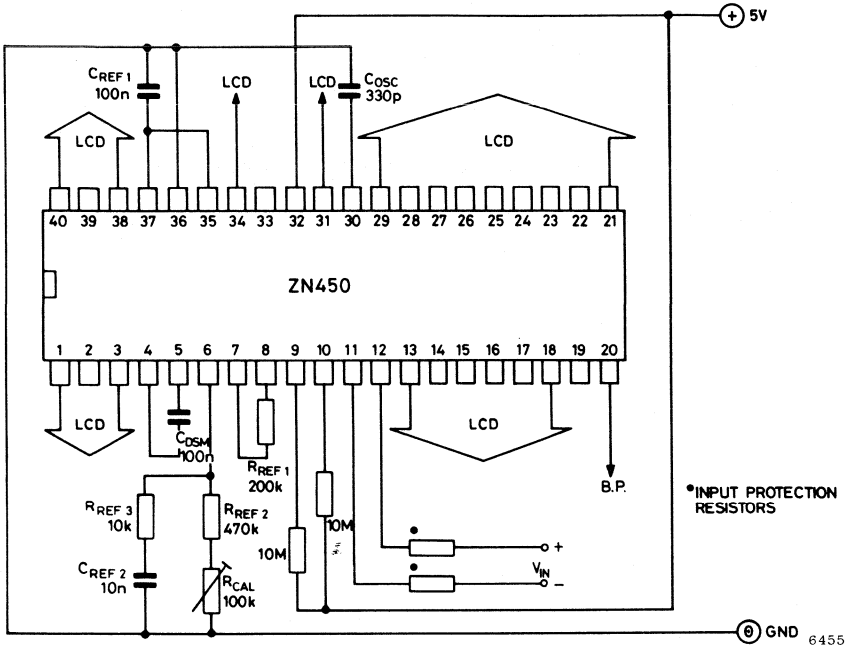


Fig. 12 – EXTERNAL COMPONENTS FOR A BASIC 200 mV DVM WITH 5V SUPPLY

Signal Conditioning

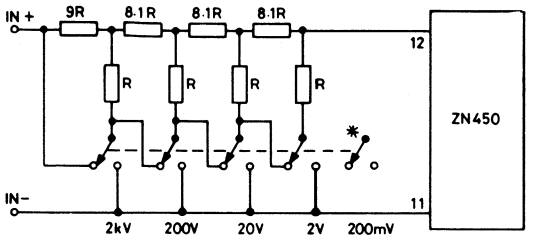
The ZN450 can be used with a wide variety of signal conditioning circuits and transducers to provide a digital display of any parameter that can be converted into a suitable d.c. voltage.

Voltage Measurement

The most obvious signal conditioning circuit is a switched input attenuator which will allow d.c. voltages greater than 200 mV to be measured. To minimise time-consuming calibration procedures it should be possible to calibrate the DVM on only one range and to rely on the precision of the attenuator resistors to give accurate results on other ranges.

However, since the input resistance of the ZN450 is about 10 MΩ its loading effect on the attenuator cannot be ignored. Fortunately this effect can be eliminated by designing an attenuator with a constant output resistance so that the ZN450 sees the attenuator as a 199.9 mV (full-scale) source with a constant source resistance on all ranges.

Three suitable types of attenuator circuit are shown in figure 13, a ladder attenuator and two types of T attenuator. The ladder attenuator has the advantage that the input resistance is fairly constant and only 3 resistor values are required, but the switching is somewhat complicated.



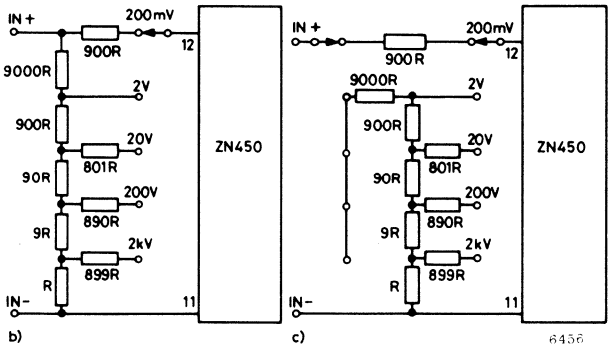


Fig. 13 – ATTENUATORS FOR MULTIRANGE VOLTMETER

The T attenuator of figure 13b has the advantage of simplicity, using only a single-pole switch, but the resistor values are slightly odd. Furthermore the input resistance drops to about 5 MΩ on the 200 mV range since the attenuator appears in parallel with the ZN450's input resistance. This problem can be overcome by using a two-pole switch so that the attenuator is disconnected on the 200 mV range as shown in figure 13c.

When designing signal conditioning circuits for use with the ZN450 care must be taken to ensure that the input offset current does not cause errors. The offset current generates an error voltage $I_{OS} \times R_O$ where R_O is the output resistance of the attenuator. There are two components in the offset current; that due to the ZN450 itself, typically 100 pA, and a component due to the mismatch of the 10 MΩ input resistors, typically 150 pA per kΩ mismatch. The offset current can be minimised by using well matched 10 MΩ resistors, or can be nulled out entirely using the circuit of figure 14.

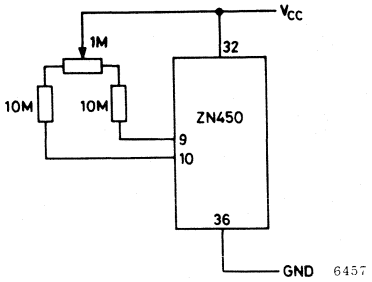


Fig. 14 – OFFSET CURRENT NULLING CIRCUIT

Current Measurement

Measurement of d.c. current is also very simple. The current to be measured is allowed to flow through a shunt resistor connected across the input terminals of the ZN450, the voltage measured being equal to the product of the current and the shunt resistors.

Currents as low as 20 μA full-scale can be measured before the input resistance and offset current of the ZN450 become significant.

For multi-range current measurement the preferred circuit is the so-called universal shunt, an example of which is shown in figure 15.

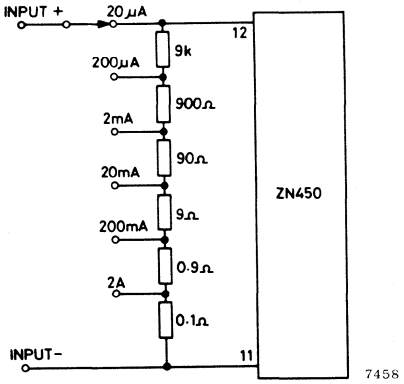


Fig. 15 – MULTIRANGE AMMETER CIRCUIT USING UNIVERSAL SHUNT

Although the full-scale voltage drop of this circuit is 200 mV it is perfectly feasible to design an ammeter with a smaller voltage drop by increasing the sensitivity of the ZN450. This has two advantages. Firstly, the voltage loss in the ammeter is reduced, which can be useful when making measurements in low-voltage circuits. Secondly, the power dissipation in the shunt resistors is reduced.

Example:
Measuring 20A full-scale with a 200 mV voltage drop the required shunt resistor will be $\frac{0.2}{20} = 10\,\text{m}\Omega$ and the full-scale power dissipation will be 4 watts. With a 20 mV drop the required resistor will be 1 mΩ and the power dissipation 400 mW.

Transducer Bridge Circuits

The high sensitivity and true differential inputs of the ZN450 make it ideal for use with transducers, particularly those which function best in a bridge configuration. The regulated 5V supply can also provide a stable excitation voltage for passive transducers such as semiconductor pressure gauges, platinum resistance thermometers and semiconductor temperature sensors.

Figure 16 shows a thermometer circuit using a silicon diode as the temperature sensor. The forward voltage drop has a temperature coefficient of approximately $-2\,mV/°C$ when the device is run at a constant current. In the bridge circuit shown this gives an increase of about $1.28\,mV/°C$ at the + input of the ZN450. The full-scale reading of the ZN450 is set to about 256 mV so that one digit corresponds to 0.1°C and the full-scale reading is 199.9°C.

The bridge configuration allows the forward voltage drop of the diode to be nulled out using P1 to give a reading of 000.0 at 0°C, whilst P2 adjusts the full-scale range of the ZN450 to read 100.0 at 100°C.

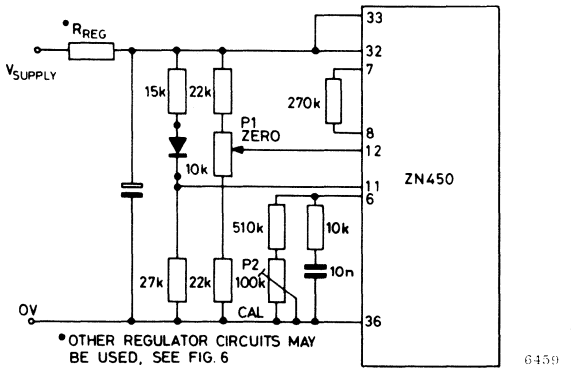


Fig. 16 – DIGITAL THERMOMETER CIRCUIT

Common-Mode Performance

The ZN450 has true differential inputs with a common-mode range of 1.8 – 1.3 volts and good common-mode rejection. However, if the full potential of the differential inputs is to be realised then care must be taken when designing with the ZN450.

When open-circuit, the inputs of the ZN450 are biased at about 2.8 volts above supply common. If a common-mode voltage other than this is applied to the inputs then care must be taken to ensure that any impedances between the inputs and the common-mode voltage (attenuators, series resistors, etc.) are the same for each input, otherwise the common-mode rejection will be impaired. This is illustrated in figure 17. Balancing the input of impedances of differential inputs to ensure good common-mode rejection is, of course, normal practice.

This is generally a problem only in systems where the voltage to be measured is referenced to the ZN450's supply ground. In battery-powered applications no common-mode voltage exists between the measured voltage and the inputs, since the supply voltage of the ZN450 is floating. However, care must be taken in battery-powered systems to ensure good a.c. rejection.

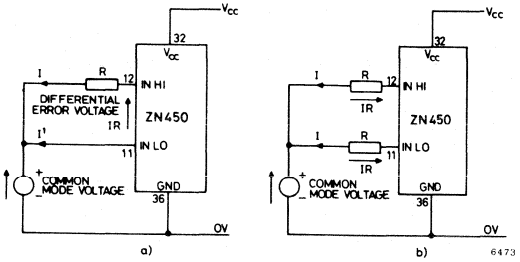


Fig. 17 – (a) UNBALANCED INPUT RESISTANCES IMPAIR COMMON-MODE REJECTION.

(b) WITH BALANCED INPUT RESISTANCES COMMON-MODE VOLTAGE DOES NOT CAUSE DIFFERENTIAL ERROR VOLTAGE.

If the voltage being measured has a large a.c. common-mode signal superimposed upon it then the supply voltage of the ZN450 will normally float up and down with the a.c. component, thus keeping the inputs of the ZN450 within their common-mode range. However, the resistance between the a.c. signal at the inputs and the ZN450 supply rails is the 5MΩ common-mode resistance of the ZN450 inputs. If significant stray capacitance exists between the ZN450 supplies and ground (for example if the battery is close to an earthed metal surface) then this can form a low pass filter with the common-mode input resistance with the result that the ZN450 supply rails do not follow the a.c. common-mode voltage at the inputs. This is shown in figure 18.

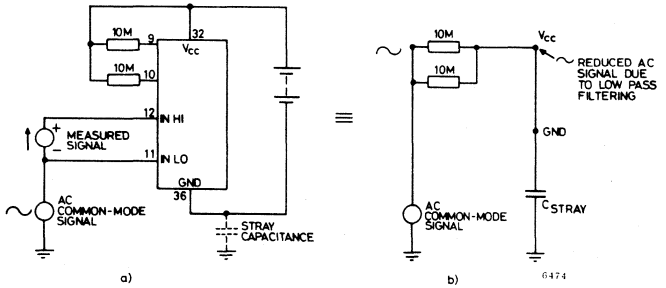


Fig. 18 – (a) BATTERY-POWERED ZN450 CONNECTED TO SIGNAL WITH LARGE A.C. COMMON-MODE SIGNAL. (SUPPLY REGULATOR NOT SHOWN).

(b) EQUIVALENT A.C. CIRCUIT.

The problem can be overcome in one of two ways. The simpler method, shown in figure 19a, is to connect a capacitor between input low and supply ground. This provides a low impedance a.c. path between these two points so that the supply rails will track the a.c. common-mode voltage.

The value of this capacitor should be several times greater than the maximum stray capacitance. On the other hand, at switch-on it must charge up via the 10M input resistance of the ZN450, so it should not be too large. A value of 22n is about the optimum.

An alternative solution is to mount the DVM in a screened enclosure, the screening being connected to input LO. This has the effect of producing a stray capacitance between the ZN450 supply rails and screen. However, since the screen is not at a fixed potential, but follows the common-mode signal, the effect of this capacitance is bootstrapped out.

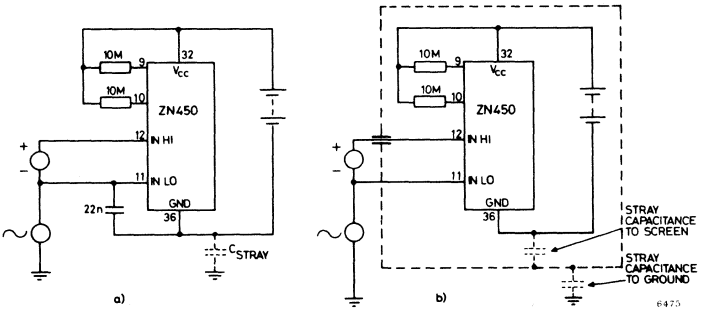


Fig. 19 – TWO METHODS OF ENSURING A.C. REJECTION IN BATTERY-POWERED CIRCUITS.

A.C. Measurements

To measure a.c. voltage or current it is first necessary to convert it into a proportional d.c. voltage. The simplest way to do this is to interpose a precision active rectifier circuit between the attenuator or shunt and the inputs of the ZN450. Such a circuit produces d.c. voltage proportional to the mean of the rectified voltage rather than a true R.M.S. result and for true R.M.S. measurements an R.M.S. converter must be used. The rectifier can be calibrated to read R.M.S. but the result is true only if the input signals have a constant form factor.

A simple precision rectifier circuit is shown in figure 20. It is completely a.c. coupled throughout by C2, C3 and C4, so the offset voltage of A1 does not appear at the output and no zero adjustment is required. To prevent the offset voltage of A1 causing it to saturate in the absence of an input signal, 100% d.c. feedback is provided by R3.

R1 and R2 provide a d.c. bias path for the non-inverting input of A1, whilst C2 provides bootstrapping to increase the a.c. input impedance.

Amplifier A2 is a voltage follower biased into the middle of the ZN450's common-mode range to provide a low impedance analogue common point. The output of the rectifier is connected to a lowpass filter comprising R6 and C5. So that both inputs of the ZN450 see the same d.c. resistance R6 is placed in series with the input LO terminal and is made equal to R4 + R5. This in no way affects the performance of the filter. With the component values shown the circuit is calibrated to read R.M.S. for sinewave inputs, so the use of this type of waveform will be assumed throughout.

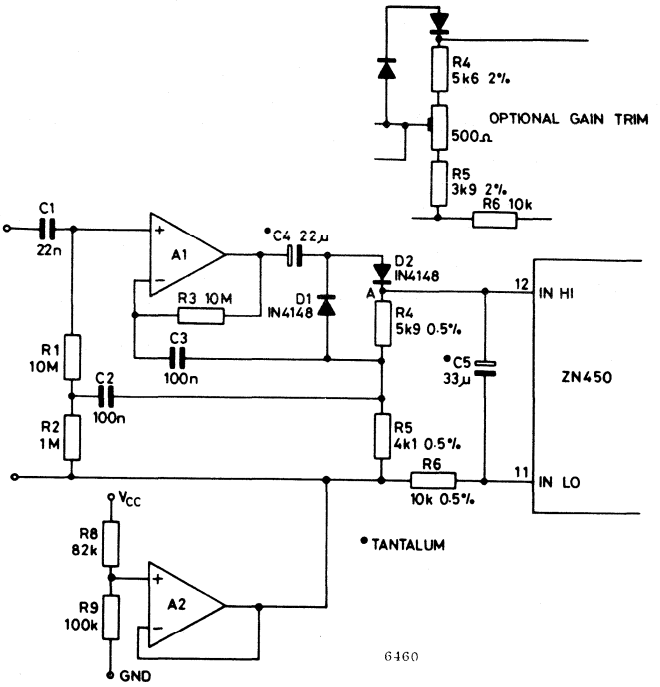


Fig. 20 – PRECISION RECTIFIER FOR A.C. MEASUREMENTS

The circuit functions as follows: when the input signal crosses zero in a positive going direction the output of A1 slews positive until D2 conducts after which the voltage at point A is defined by the equation:

$$V_A = G \times V_{IN}, \text{ where } G = \frac{R_4 + R_5}{R_5}$$

and since

$$R_6 = R_4 + R_5$$

$$G = \frac{R_6}{R_6 - R_4}$$

and

$$R_4 = R_6 \frac{(G-1)}{G}$$

This voltage tends to charge up C_5 in a positive direction via R_6. When the signal crosses zero in a negative going direction the output of A1 slews negative until D1 conducts, after which the output voltage at point B is equal to (minus) V_{IN}. This voltage tends to charge up C_5 in a negative direction via R_6 and R_4.
Now, assuming the time constant R_6/C_5 is long compared to the period of the input waveform, the voltage on C_5 will eventually reach equilibrium. When this is the case the mean current flowing into C_5 during the positive half cycle must equal that flowing out of C_5 during the negative half cycle.

i.e.

$$\frac{V_{A(MEAN)} - V_C}{R_6} = \frac{-V_{B(MEAN)} + V_C}{R_6 + R_4}$$

Now the mean value of a rectified sinewave signal is 0.9 times the R.M.S. value therefore

$$V_{A(MEAN)} = 0.9.G.V_{IN(RMS)}$$

and

$$V_{B(MEAN)} = -0.9\,V_{IN(RMS)}$$

In order for the ZN450 to read correctly V_C must equal V_{RMS} therefore

$$V_A = 0.9.G.V_C$$

and

$$V_B = -0.9\,V_C$$

therefore

$$\frac{V_C(0.9G-1)}{R_6} = \frac{1.9V_C}{R_6+R_4}$$

substituting for R_4 and eliminating V_C

$$\frac{0.9G-1}{R_6} = \frac{1.9}{R_6 + R_6\frac{(G-1)}{G}}$$

eliminate R_6

$$0.9G-1 = \frac{1.9G}{2G-1}$$

$$(0.9G-1)(2G-1) = 1.9G$$

$$1.8G^2 - 4.8G + 1 = 0$$

Solving the above quadratic equation gives

$$G = 2.439$$

or

$$R_4 = 0.59R_6$$

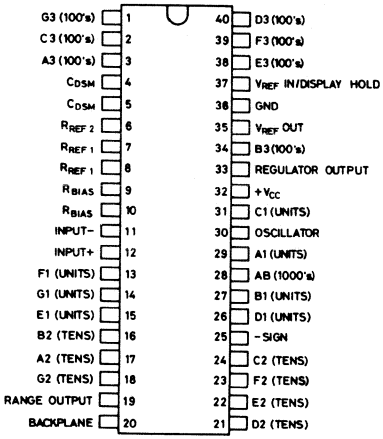
$$R_5 = \frac{R_6}{2.439}$$

These equations allow the values of R_4 and R_5 to be calculated for any value of filter resistor R_6. With the values shown the circuit is accurate to about $\pm 1.5\%$ over the frequency range 40 Hz to 1 kHz.

Ordering Information

Type Number	Package	Operating Temperature Range
ZN450E	Plastic	0°C to +70°C
ZN450CJ	Ceramic	0°C to +70°C

PIN CONNECTIONS



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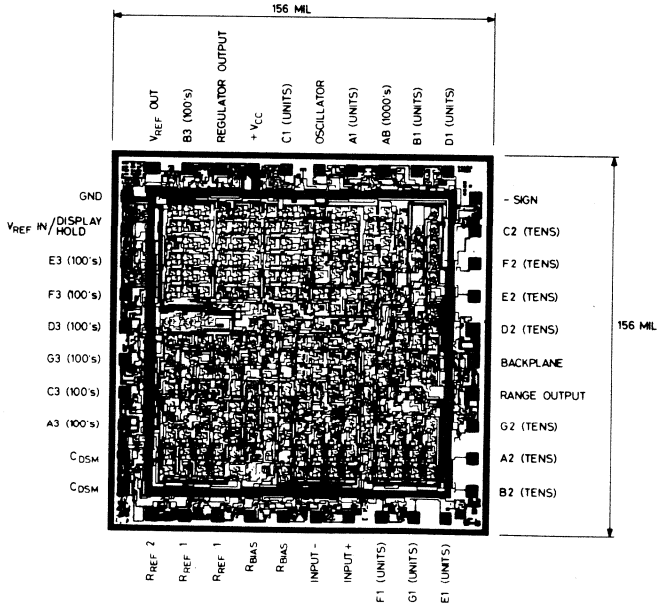
CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZNA116E

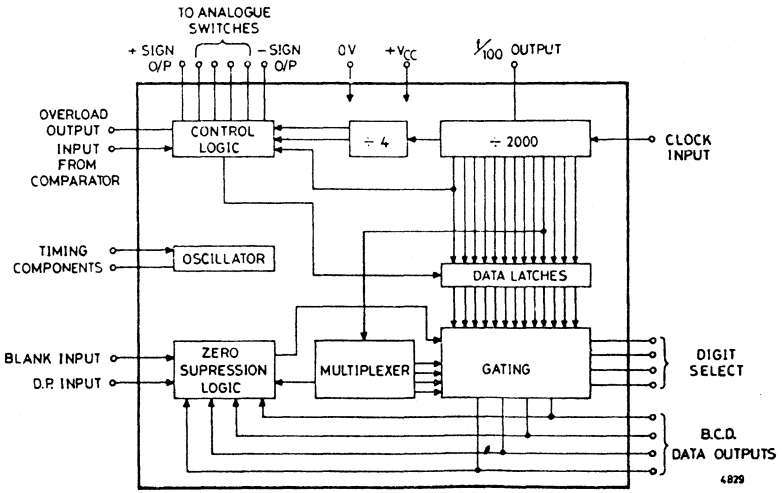
Low Power 3½ Digit D.V.M. Integrated Circuit

FEATURES

- 3½ Decade display (±1999 max. reading)
- Automatic polarity detection and indication
- Leading zero suppression
- Overload indication
- Multiplexed B.C.D. outputs capable of driving a T.T.L. decoder/driver directly (e.g. ZNA7447A)
- External input to blank display
- Internal oscillator, adjustable externally
- An output at $^1/_{100}$ clock frequency for under range indication, or for synchronising the clock frequency for optimum mains rejection
- Single rail, 5 volt supply operation (at 10 mA typical)

GENERAL DESCRIPTION

The ZNA116E allows a precision 3½ digit D.V.M to be constructed very easily. It provides all the control logic necessary for a D.V.M using the well known dual slope integration technique. The low power requirements of the device make it attractive for portable battery operated applications and, since it is bipolar, requires no special handling precautions.



System Diagram

ZNA116E

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
1	Earth	Supply 0 volts
2	f/100 output	An output at $^1/_{100}$ of the clock frequency is available at this pin.
3	Clock input	An external clock can be applied at this pin, or the internal oscillator can be used by linking it to pin 14. A measurement is made every 8000 clock periods. Transfer of a number to the latches occurs at the first –VE going clock edge after comparison has been made. The counter toggles on +VE going clock edges. Max. clock frequency = 50 kHz, Min. logic 0 time at clock input = 8 μsec.
4	M1	Digit drive output. When this output is low, the most significant digit is displayed.
5	M2	Digit drive output. When this output is low, the second most significant digit is displayed.
6	M3	Digit drive output. When this output is low, the third most significant digit is displayed.
7	M4	Digit drive output. When this output is low, the least significant digit is displayed. The multiplexed frequency = $^1/_{40}$ clock frequency.
8	Blank input	When this input is held at logic 1, the data outputs, A,B,C,D, will also all be at a logic 1. This is detected by the T.T.L. decoder/driver and the display is switched off.
9	D.P. input	When this input is at logic 1, leading zeroes are blanked off. Pins 5 and 6 can be wired to the D.P. input to give the correct display when a decimal point is displayed. (see diagrams).
10	A	2^0 BCD data output
11	B	2^1 BCD data output
12	C	2^2 BCD data output
13	D	2^3 BCD data output
14	Oscillator output	Link to pin 3 if internal oscillator is to be used.
15	Oscillator input	External components, connected to this pin, control oscillator frequency. (see figure 1).
16	+VE reference switch output	When this output is at logic 1, it connects the +VE reference voltage into the integrator.
17	–VE reference switch output	When this output is at logic 1, it connects the –VE reference voltage into the integrator.
18	–Sign output	This output is at logic 1 when a negative input voltage is being measured.

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
19	+Sign output	This output is at logic 1 when a positive input voltage is being measured.
20	Comparator input	This input is connected to the output of the external compartaor.
21	Signal switch output	When this output goes to logic 1, it connects the voltage to be measured into the integrator.
22	V_{CC}	Supply +5 volts.
23	Reset switch output	When this output is at logic 1, the switch across the integrator capacitor is turned on to completely discharge it.
24	Overload output	If the integrator capacitor does not discharge completely until after the counter has reached 2000, this output will go to logic 1.

ZNA116E

TECHNICAL DATA

(a) Maximum Ratings:

Supply voltage .. .. 5.5 volts
Operating temperature .. .. 0°C to +70°C
Storage temperature .. .. .. −55°C to +125°C

(b) Electrical Characteristics (T_A = 0°C to +70°C)

Parameter		Min.	Typ.	Max.	Units	Test conditions
Supply voltage	V_{OC}	4.75		5.25	Volts	
Supply current	I_{CC}			15.0	mA	V_{CC} = 5 volts
Logic 0 level All input pins except pin 15	V_{IL}			0.8	Volts	
Logic 1 level All input pins except pin 15	V_{IH}	2.0			Volts	
High-level input current All input pins except pin 15	I_{IH}			4.0	μA	$V_{in} = V_{CC}$
Low-level input current All input pins	I_{IL}			−4.0	μA	V_{in} = 0V
Logic 0 level Output pins 2,4,5,6,7,10, 11,12,13	V_{OL}			0.4	Volts	I_{sink} = 1.6 mA
Logic 0 level Output pins 14,18,19,21,24	V_{OL}			0.4	Volts	I_{sink} = 1.0 mA
Logic 0 level Output pins 16,17,23	V_{OL}			0.4	Volts	I_{sink} = 0.5 mA
Logic 1 level All output pins except pin 14	V_{OH}	2.4			Volts	I_{out} = 10 μA
Oscillator frequency			20.0		kHz	With timing components shown in figure 1
Temperature coefficient of oscillator			±0.02		% per °C	Excluding temp. coefficient of the external timing components
Variation in oscillator frequency with changes in V_{CC}			−0.4		% per volt	T_A = 25°C

(c) Notes:

1. Pin 14 is an open-collector output. All other outputs have a nominal 100 kΩ pull-up resistor to V_{CC} rail.
2. Although the oscillator and logic will function up to 50 kHz, this is not recommended as the analogue circuitry becomes more critical.

OSCILLATOR CIRCUIT

RECOMMENDED COMPONENTS FOR 20 kHz OPERATION

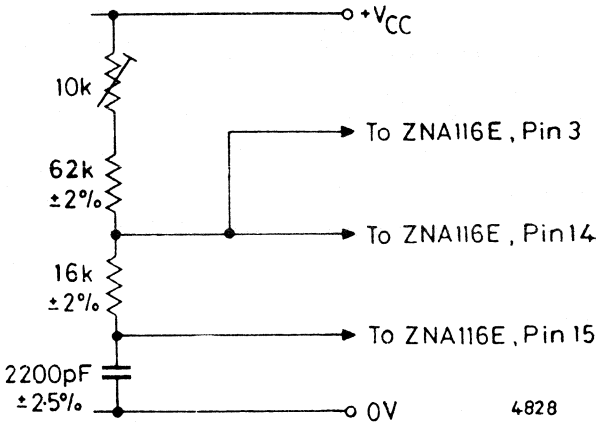


Figure 1.

Notes:

(a) Oscillator stability is better than 0.02% per °C.

(b) The potentiometer should be set so that the frequency of oscillation is 20 kHz. This is best monitored at pin 2, to avoid loading the oscillator while setting up.

(c) The potentiometer and the 62k resistor can be replaced by a single 68k ±2% high stablity resistor at the loss of some mains rejection only.

THE DUAL SLOPE SYSTEM

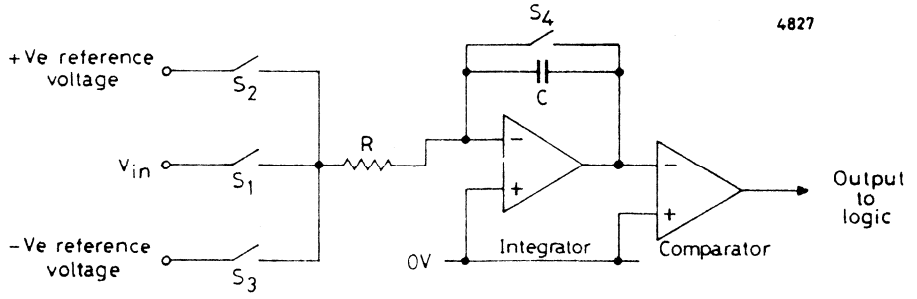


Figure 2.
(Refer to timing diagram, figure 3)

At time T_1 ; S2, S3 and S4 are open and S1 closes to apply the input voltage, V_{in}, to the integrator. The integrator capacitor, C, charges up linearly until time T_2 which is 4000 clock periods after T_1. The voltage at the integrator output, V_x, at time T_2 is proportional to V_{in}.

At time T_2, S1 is opened and either S2 or S3 is closed, to apply a reference voltage, of the opposite polarity to V_{in}, to the integrator, Thus C is made to discharge at a constant rate and at time T_3 the output voltage of the integrator will again be zero. This is detected by the comparator and the reference voltage is now switched off and the number of clock pulses corresponding to T_x will be transferrred to latches and displayed. This number is proportional to V_x and hence is proportional to V_{in}. If T_x exceeds 2000 clock periods, an overload condition is indicated.

At time T_4, which is 3000 clock periods after T_2, S4 closes to completely discharge the capacitor. At time T_5, which is 4000 clock periods after T_2, S4 opens and the cycle is repeated.

If S1 is closed for a time which is a multiple of 20 msec., any 50 Hz mains ripple superimposed on V_{in} will be integrated to zero and thus good mains rejection is obtained.

The dual slope D.V.M. does not require a high stability capacitor or high stability oscillator (unlike single slope systems) to achieve high accuracy.

ZNA116E TIMING

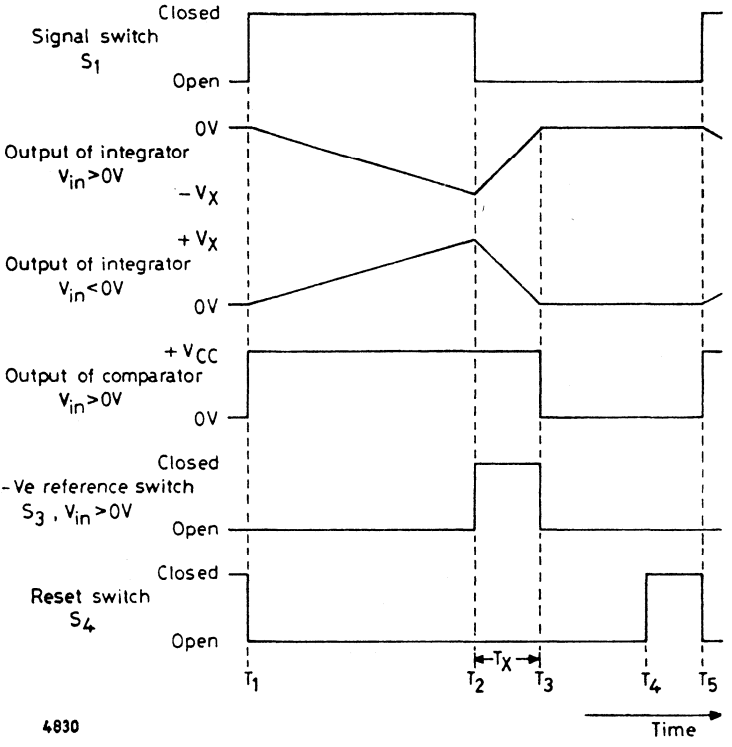


Figure 3.

THE DESIGN OF D.V.M. CIRCUITS USING THE ZNA116E

The ZNA116E provides the control logic necessary to construct a D.V.M. with a $3\frac{1}{2}$ digit display having an accuracy of $\pm\frac{1}{2}$ digit. The actual accuracy obtained will depend on four factors:

(a) Accuracy of calibration.

(b) Stability of reference sources.

(c) Stability of transistor switches.

(d) Operational amplifier drift.

The circuit details are given for the construction of a simple D.V.M. circuit which runs off a single 5 volt supply rail. The accuracy of this D.V.M., typically 0.1% $\pm$1 mV., (on the 1v. range) should be adequate for many applications.

To achieve this accuracy, the nominal 5 volt supply rail should be held stable to $\pm$50 mV. An I.C. voltage regulator is ideal for this purpose.

The main factor limiting the performance of this circuit is (d). If a better performance is required, an amplifier with a lower bias current must be used (e.g. ZN741) running of $\pm$5 volt supply rails, so that the drift becomes less significant. More elaborate interfacing with the ZNA116E will be required in this case.

D.V.M. CONSTRUCTION

Due to the clearly defined application of the ZNA116E, the full circuit is given for a simple $3\frac{1}{2}$ digit D.V.M. together with full printed circuit board details.

The construction is defined in two distinct halves an analogue board containing integrator, comparator, reference supplies and transistor switches; and a digital board containing the ZNA116E, display, driver and oscillator components. This allows the constructor the chance to alter the 'front end' (analogue circuit) if desired, without disturbing the digital board.

PRINTED CIRCUIT BOARD

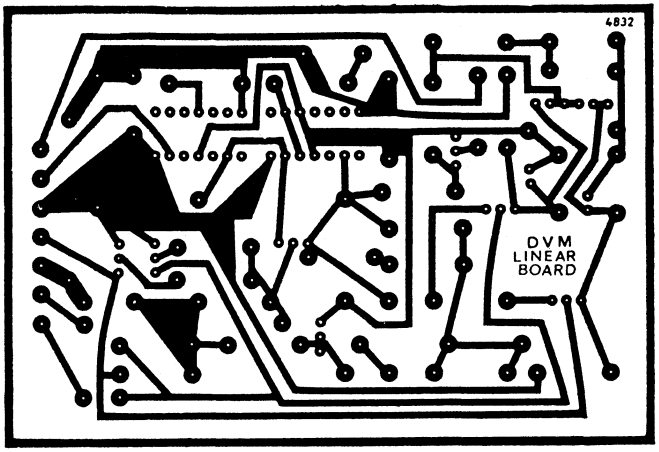


Figure 4. ANALOGUE BOARD (copper side) ¾ FULL SIZE

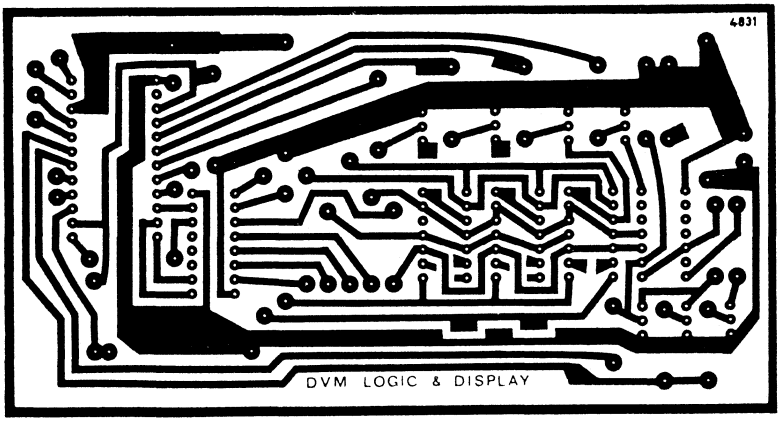
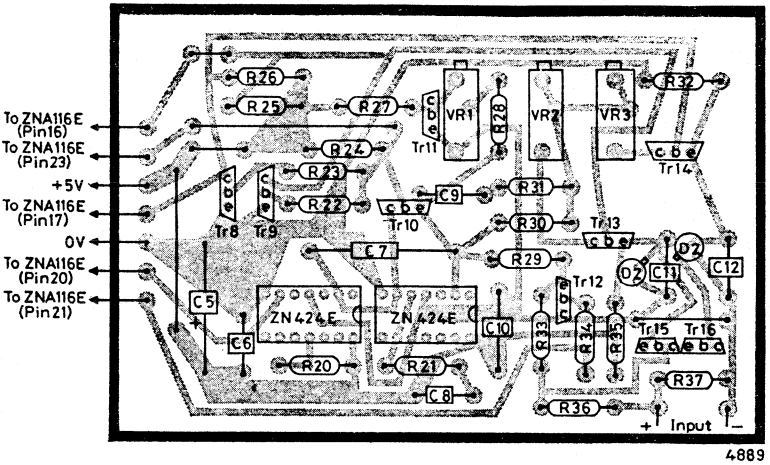
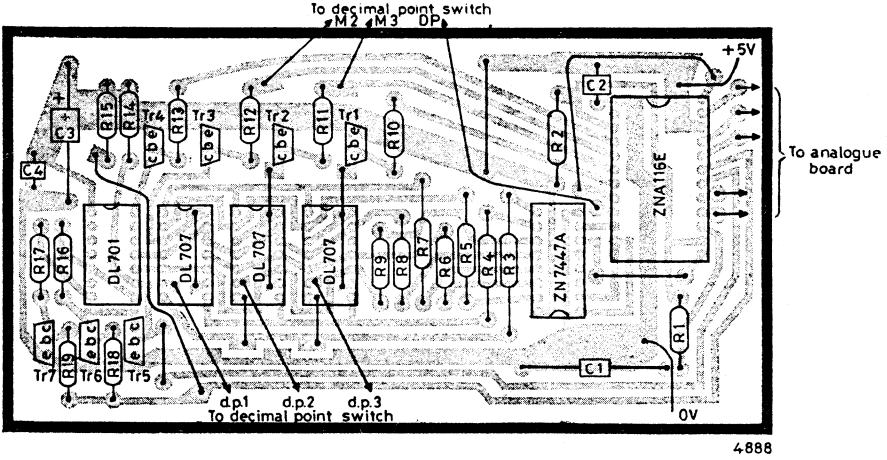


Figure 5. DIGITAL BOARD (copper side) ¾ FULL SIZE



ANALOGUE BOARD – Component positions

Figure 6.



DIGITAL BOARD – Component positions

Figure 7.

CIRCUIT DIAGRAM OF ANALOGUE BOARD

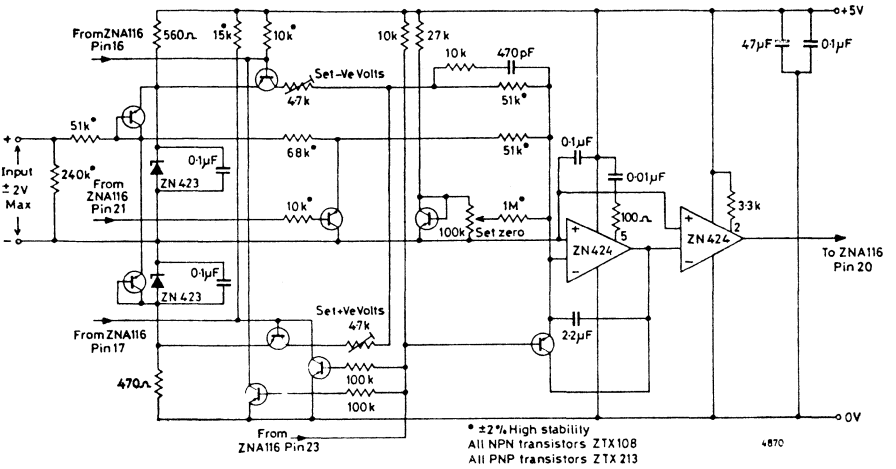


Figure 8.

CIRCUIT DIAGRAM OF DIGITAL BOARD

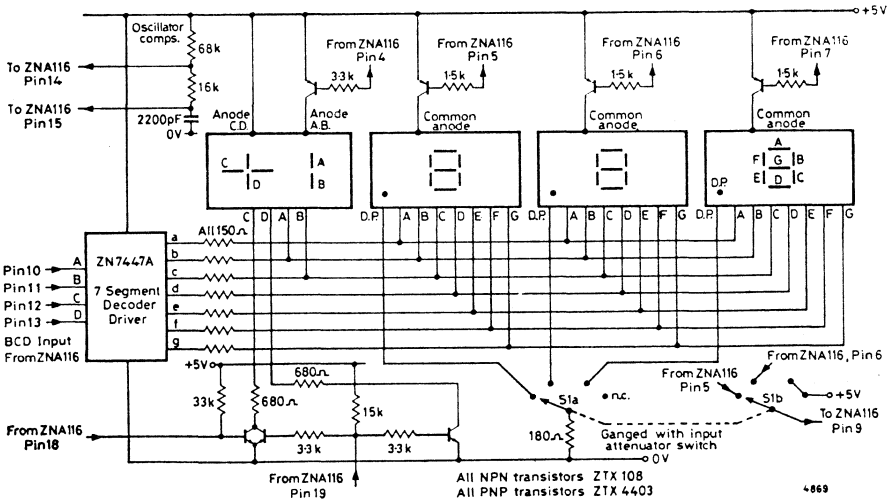


Figure 9.

D.V.M. COMPONENT LIST

R1	16k ±2%	R14	33k	R27	27k
R2	68k ±2%	R15	15k	R28	1M ±2%
R3	150	R16	680	R29	51k ±2%
R4	150	R17	680	R30	51k ±2%
R5	150	R18	3.3k	R31	10k
R6	150	R19	3.3k	R32	470
R7	150	R20	3.3k	R33	68k ±2%
R8	150	R21	100	R34	10k ±2%
R9	150	R22	100k	R35	560
R10	1.5k	R23	100k	R36	51k ±2%
R11	1.5k	R24	10k	R37	240k ±2%
R12	1.5k	R25	10k	R38	180
R13	3.3k	R26	15k		

VR1 100k
VR2 5k
VR3 5k
} Bourns 3009P

All values given in ohms.

All resistors ±10% unless stated otherwise.

C1 2200 pF ±2.5%
C2 0.033 µF
C3 68 µF 10 vw. electrolytic ±50%
C4 0.033 µF
C5 68 µF 10 vw. electrolytic ±50%
C6 0.1 µF
C7 2.2 µF ±10%
C8 0.01 µF
C9 470 pF
C10 0.1 µF
C11 0.1 µF
C11 0.1 µF
C12 0.1 µF

All capacitors ±20% non-electrolytic unless stated otherwise.

Tr1, Tr2, Tr3 Tr4 — all ZTX4403
Tr5, Tr6, Tr7, Tr8, Tr9, Tr10, Tr11, Tr13 Tr14, Tr15, Tr16, — all ZTX 108
Tr12 — ZTX213

D1, D2 — both ZN423

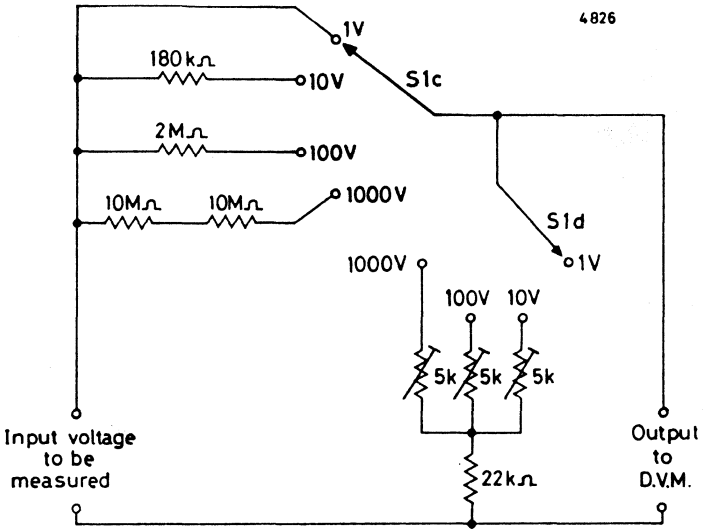
ZNA116E 1 off
ZN424E 2 off
ZN7447A 1 off

DL707L display 3 off
DL701 display 1 off

ZNA116E

ATTENUATION OF INPUT VOLTAGE

For measuring voltages of ±2 volts or more, the following input attenuator circuit may be used.



All resistors ±2% high stability, presets ±20% carbon.
Figure 10.

The input impedance is 100 kΩ on the 1 volt range and 20 kΩ/volt on the other three ranges. If a greater impedance than this is required, an attenuator using higher value resistors followed by an F.E.T. input buffer amplifier should be used.

Note: In the above diagram, switches S1c and S1d are ganged with S1a and S1b, the decimal point switch, shown in figure 9.

CONSTRUCTIONAL NOTES

(1) The leads joining the analogue board to the digital board should not be longer than about six inches.

(2) Before connecting the circuit to a power supply, make sure that all the external links, shown in figures 6 and 7, have been connected to the printed circuit boards. There should be five links on the analogue board and twelve on the digital board.

(3) If the applied input voltage is too large, the display will be blanked off as an overload indication. If a diode is connected between pins 8, 24 and 21 of the ZNA116E, as shown below in figure 11, the display will flash for overload conditions.

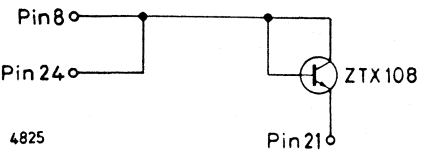


Figure 11.

CALIBRATION PROCEDURE

The range switch is placed in the 1 volt position and the input terminals are shorted together. VR2 and VR3 should be set about half-way. The set-zero preset VR1 is now adjusted until the display just flickers between +0 and –0.

A known positive voltage, between one and two volts, is now connected to the input terminals and VR3 is adjusted until this voltage is displayed.

The input voltage is then reversed and VR2 is adjusted until the display is again correct.

VR1, VR2 and VR3 are now correctly set and should not need altering again.

Since the three 5k presets in the attenuator section are completely independent of each other, these can be easily set to give the required attenuation of 10, 100 and 1000.

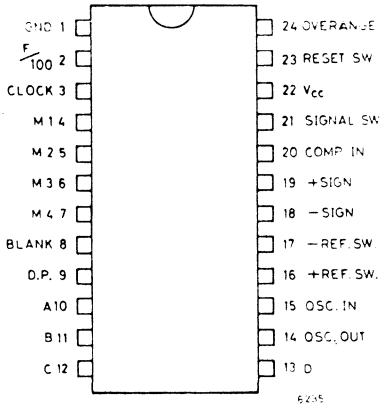
Calibration is now complete.

SPECIFICATION OF D.V.M.

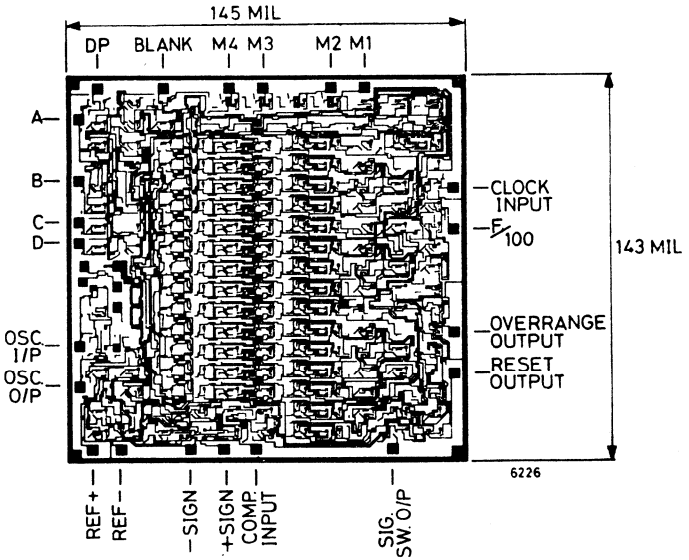
Maximum reading	±1999
Readings per second	2½ typical
Typical accuracy (1 volt range)	0.1% of reading ±1 mV
Temperature coefficient (1 volt range)	±0.1 mV per °C typical
Input impedance	100 kΩ for 1 volt range 200 kΩ for 10 volt range 2 MΩ for 100 volt range 20 MΩ for 1000 volt range
Total supply current (with all segments on)	200 mA typical

ZNA116E

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZNA216E
ZNA216J

Low Power 3¾ Digit D.V.M. Integrated Circuit

FEATURES

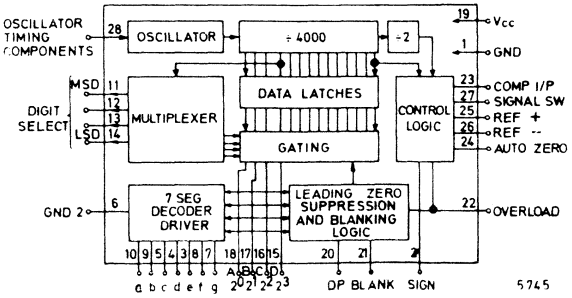
- 3¾ digit display (±3999 max. reading)
- Automatic zero adjustment with 1 μV/°C temperature coefficient
- Seven-segment outputs for direct drive of LED displays
- BCD outputs
- Automatic polarity detection and indication
- Flashing overload indication, separate overload output
- Blanking input, e.g. for low battery indication
- Automatic blanking of display leading zeroes
- On-chip clock, may be externally synchronised
- TTL and CMOS compatible
- Single +5V supply
- Pinning optimised for easy p.c.b. layout

DESCRIPTION

The ZNA216 D.V.M. I.C. is a versatile D.V.M. system component which contains all the control logic necessary to construct a dual-slope digital voltmeter, whilst leaving the designer free to configure the analogue circuitry to his own requirements.

The I.C. has multiplexed data outputs, both in BCD format and in seven-segment format for direct drive of LED displays. A number of useful features are incorporated into the device, including leading zero blanking of the display, flashing over range indication and an auto zero facility which removes the need for manual zero adjustment.

Apart from the more obvious applications of D.V.M. and D.P.M. the I. C. can be used to construct any other instrument where an analogue input from, say, a transducer is to be converted into a digital reading, for example a digital thermometer. The ZNA216 may also be used as an A-D converter in single-channel data acquisition systems, or to interface to a microprocessor system.



System Diagram

ZNA216E/J

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
1	Gnd 1	Supply 0 volts
2	Sign	Open collector output, goes low when –ve input voltage is being measured.
3	e	Open collector segment output, goes low when segment is on.
4	d	Segment output as above.
5	c	Segment output as above
6	Gnd 2	0 volt supply for segment drivers, must be connected to Pin 1.
7	g	Segment output as above
8	f	Segment output as above
9	b	Segment output as above.
10	a	Segment output as above
11	M1	Digit drive output, goes low for the most significant digit to be displayed, first in digit scan sequence.
12	M2	Digit drive output, goes low for the second most significant digit fo be displayed, second in digit scan sequence.
13	M3	Digit drive output, goes low for the third most significant digit to be displayed, third in digit scan sequence.
14	M4	Digit drive output, goes low for the least significant digit to be displayed, fourth in digit scan sequence.
15	D	2^3 BCD data output.
16	C	2^2 BCD data output.
17	B	2^1 BCD data output.
18	A	2^0 BCD data output.
19	V_{CC}	Supply +5 volts.
20	DP	When this input is at logic 1, leading zeroes are blanked.
21	Blank	While this input is at logic 1, all segment outputs are off and all BCD data outputs are at logic 1.
22	Overload	If the integrator capacitor does not discharge before the conter reaches 4000, this output goes to logic 1.
23	Comp.	This input is connected to the output of the external comparator.
24	Azero	When this output is high, auto zero correction is applied to the integrator.

Pin number	Name	Function
25	Ref+	When this output is at logic 1, the +ve reference voltage is connected to the integrator.
26	Ref–	When this output is at logic 1, –ve reference voltage is connected to the integrator.
27	Signal switch	When this output is at logic 1, the input voltage to be measured is connected into the integrator.
28	Clock	The external clock oscillator components are connected to this pin (see diagrams). Alternatively, this pin may be driven by an external signal. A measurement is made every 8000 clock periods. The counter toggles on –ve going clock edges and transfer to the latches occurs at the first +ve going clock edge after comparison has been made which avoids false triggering from the integrator output. Max. clock frequency 50 kHz.

ZNA216E/J

(a) Absolute Maximum Ratings:

Supply voltage	7.0 volts
Operating temperature	0°C to +70°C
Storage temperature	−55°C to +125°C

(b) Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V unless otherwise specified).

Parameter		Min.	Typ.	Max.	Unit	Test conditions
Supply voltage		4.5		5.5	V	
Supply current				20	mA	
Low level input voltage	All inputs			0.8	V	
Low level input current	All inputs			−4	μA	V_{in} = 0V
Input clamp diode voltage	All inputs			−1.5 V_{CC} +1.5	V V	I_{in} = −12 mA I_{in} = 10 mA
High level input voltage	Oscillator RC input	2.5			V	
	All other inputs	2.0			V	
High level input current	Oscillator RC input			100	μA	V_{in} = 2.5V
	All other inputs			4	μA	V_{in} = 5.0V
Low level output voltage	a, b, c, d, e, f, g			0.8	V	I_{sink} = 20 mA
	Sign			0.4	V	I_{sink} = 5 mA
	Overload, Ref+, Ref−, Azero, Signal switch, a,b,c,d,M1,M2, M3, M4			0.4	V	I_{sink} = 1.6 mA
High level output voltage	Overload, Ref+, Ref−, Azero, Signal switch, a,b,c,d,M1,M2, M3, M4	2.4			V	I_{out} = 10 μA
			V_{CC} −0.1		V	I_{out} = 0
High level output current	a,b,c,d,e,f,g Sign			−10	μA	V_{out} = 5.0V

(c) Note:

Although the oscillator and logic will function up to 50 kHz, this is not recommended as the analogue circuitry becomes more critical.

THE DUAL SLOPE SYSTEM

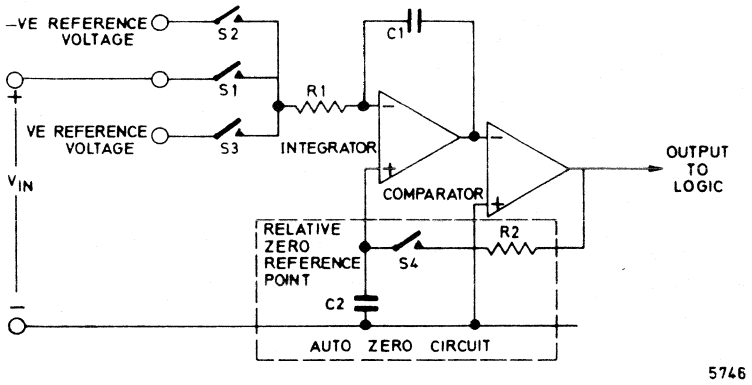


Figure 1. Dual Slope Block Diagram.

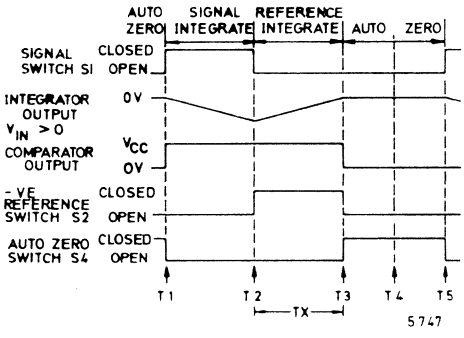


Figure 2a. Timing Diagram for in-range input.

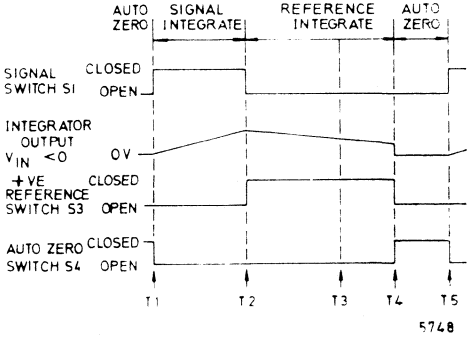


Figure 2b. Timing diagram for overrange input

Dual slope integration is a D.V.M. circuit technique designed to cancel out the effects of drift in circuit components. A block diagram of the analogue section of a dual-slope D.V.M. is shown in figure 1, whilst a timing diagram for its operation is shown in figure 2.

At time T_1, S1 is closed by the D.V.M. logic, connecting the input signal to the integrator until time T_2, which is 2000 clock periods after T_1. During this time the integrator output ramps positive or negative, depending on input voltage polatrity, to a voltage

$$V_o = \frac{-V_{in}\, 2000\, t_c}{R_1 C_1}$$

where t_c is the clock period.

The polarity of the integrator output voltage during this period, and hence of the input voltage, is sensed by the comparator, whose output is connected to the control logic.

At time T_2, S1 is opened and, depending on the input voltage polarity, either S2 or S3 is closed. This connects a reference voltage of opposite polarity to V_{in} to the integrator input, so that the integrator output ramps back towards zero. The number of clock periods required for the integrator output to reach zero is counted by the DVM counter. When the output reaches zero the comparator output changes state, S2 or S3 opens and the count is stopped. Since the second integration also takes place over a voltage V_o then,

$$V_o = \frac{-V_{REF}\, nt_c}{R_1 C_1} \text{ where n is the count at time } T_3$$

but V_o also equals $\dfrac{-V_{in}\, 2000 t_c}{R_1 C_1}$

$$\text{thus } n = \frac{2000\, V_{in}}{V_{REF}}$$

R_1, C_1 and t_c have disappeared from this final equation, so the accuracy of the D.V.M. is unaffected by the long-term stability of these parameters. The only factors influencing accuracy are the stability of V_{REF} and variations in the 'on' resistance of the analogue switches S1 to S3. The former can be assured by careful choice of a reference source, e.g. the Ferranti ZN423 or ZN458, whilst the effect of the latter can be minimised by making R_1 lage compared to the on resistance of S1 to S3.

If V_{REF} is exactly 2V then $n = 1000\, V_{in}$, i.e. the count will be equal to the input voltage in millivolts. For the ZNA216 the maximum reading is 3999. If a count of 4000 occurs before the integrator output reaches zero, as shown in figure 2b, then S2 or S3 will open and the overrange output will go high.

In a practical D.V.M. it is unlikely that a reference voltage of exactly 2V will be available, or an input range other than 3.999V may be required. In this case a different resistor value (R_{REF}) will be used for the reference integration. The equation then becomes :

$$n = \frac{2000\, V_{in} \,.\, R_{REF}}{V_{REF} \,.\, R_1}$$

R_1 and R_{REF} should be high-stability types.

AUTO ZERO

Any offset voltage and bias current in the integrator will be integrated along with the input signal and since, for example, a 3.999V D.V.M. has a resolution of 1 mV an offset of a few hundred microvolts can lead to errors in the least significant digit. Manual zero adjustment is time-consuming and has to be repeated frequently due to temperature drift.

The auto zero of the ZNA216 operates during the period T_3 to T_5, or T_4 to T_5 in the case of an overrange input. S4 is closed, S1 S2 and S3 are opened so that only the integrator offset voltage is integrated, thus causing the integrator output to drift either positive or negative. The integrator output is amplified by the comparator (which is nothing more than an extremely high gain amplifier) and this charges C2 via R2 to apply a voltage to the non-inverting input of the integrator. The polarity of this voltage is such as to null out the effects of integrator offset voltage and bias current and thus cancel integrator drift. Depending on comparator gain a zero error of a few hundred nanovolts may be achieved by this method.

HUM REJECTION

Any mains hum pickup superimposed on the input signal will cause errors in the D.V.M. reading. However, if the period $T_2 - T_1$ is made a multiple of the mains period then equal numbers of positive and negative half-cycles of the mains waveform will be integrated and will cancel each other out. For 50 Hz mains $T_2 - T_1$ should be 20 ms or a multiple thereof, while for 60 Hz mains $T_2 - T_1$ should be 16.67 ms or a multiple thereof.

Adjustment of the period $T_2 - T_1$ is achieved by varying the frequency of the clock oscillator which controls the operation of the D.V.M.

DISPLAY MULTIPLEXING

The BCD and seven-segment data outputs are multiplexed, the data appearing in the sequence MSD to LSD. To identify which digit is present at the outputs at any time the four digit select outputs go low in turn, synchronous with the relevant digit appearing at the data outputs. The seven segment outputs can be used to drive the cathodes of a multiplexed common-anode LED display whilst the digit select outputs may be used to turn on digit-drive transistors, which activate each display digit in sequence.

DECIMAL POINT (ZERO BLANKING) INPUT

Before the start of each multiplex cycle a latch in the I.C. is set. This holds the display blanked until non-zero data appears at the BCD outputs, when the latch is reset and the disply is unblanked. For example, if the MSD were non-zero the latch could reset immediately the MSD appeared, so all four digits would be displayed. Conversely if the MSD were zero but the second digit were non-zero then the display would be blanked for the MSD and only three digits would appear. In this way leading zeroes in the display are suppressed. The LSD is always displayed whether zero or not.

The D.P. input can be used to override the zero blanking by taking this pin to logic '0'. This facility allows a correct display to be obtained when a decimal point is used.

For example, if the decimal point is to the left of the MSD then a low-going pulse to the D.P. input synchronous with the MSD output will cause all digits to the right of the decimal point to be displayed, whether zero or not. Thus, if the input voltage were, say .0056 volts then the display would be .0056. If the zero blanking were not overridden in this way the display would be .--56, which is clearly unsatisfactory.

OSCILLATOR CIRCUIT

The operation of the D.V.M. circuit is controlled by a clock oscillator, which provides drive for the counter, control logic and display multiplexing. Two external components, a resistor and a capacitor, are required to make the oscillator function. The oscillator temperature stability is typically $\pm 0.02\%$ per °C.

As mentioned earlier, the oscillator frequency should be chosen so that $T_2 - T_1$ is a multiple of the mains period. It should not be chosen so low as to cause noticeable flicker in the display multiplexing, but on the other hand it should not be chosen too high or the design of the analogue circuitry becomes more critical.

The optimum oscillator frequency is 20 kHz since this makes $T_2 - T_1 = 100$ ms which gives good hum rejection at either 50 Hz or 60 Hz. This frequency can be obtained by using the component values shown in figure 3. The potentiometer may be adjusted to give a frequency of 20 kHz measured at pin 28, in which case a high impedance, low capacitance probe should be used to avoid loading the oscillator. Alternatively, the trimmer may be adjusted to give a frequency of 500 Hz at any of the digit select outputs, when no special precautions are required.

If required the oscillator timing components may be omitted and the oscillator input may be driven by an external clock at TTL logic levels.

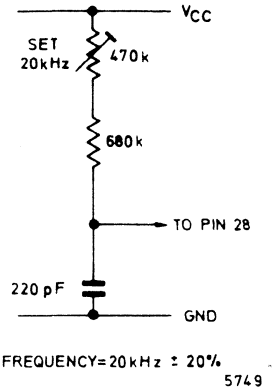


Figure 3. Oscillator external components.

INPUT AND OUTPUT CIRCUITS

Apart from the oscillator input (which is a Schmitt trigger type of circuit) all other inputs are as shown in figure 4a. All outputs are as shown in figure 4b, except for those designated as open-collector, which have no pull-up resistor.

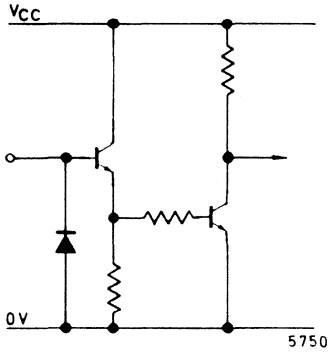


Figure 4a. Input circuit

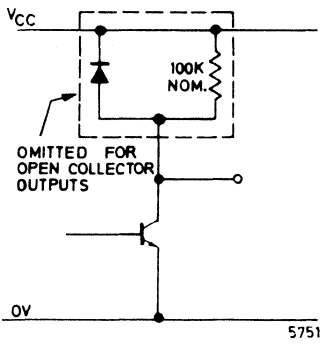


Figure 4b. Output circuit

DISPLAY DRIVING

The 20 mA sink capability of the segment outputs allows common anode LED displays to be driven with a minimum of external components, as shown in figure 5. The segment current limit resistors should be chosen to give the desired segment current, allowing for the forward voltage drop of the LED, whilst the digit output resistors should be chosen to give sufficient base current to saturate the digit drive transistors.

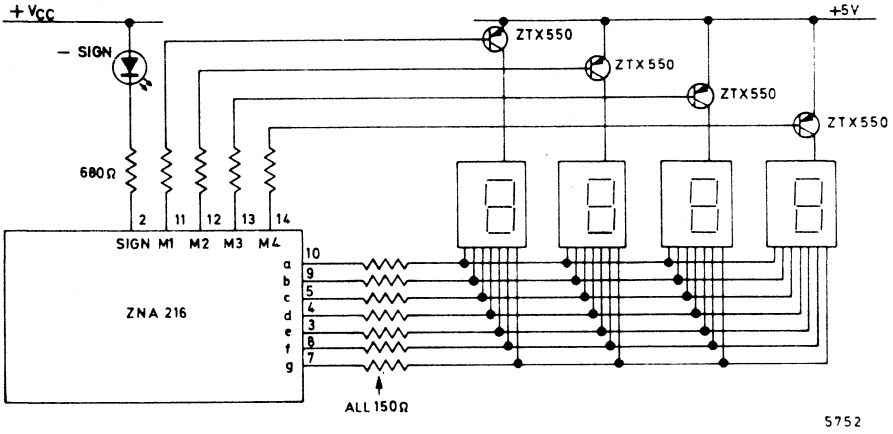


Figure 5. Display drive circuit

OVERRANGE AND LOW BATTERY INDICATION

If the input voltage exceeds the full-scale range then the display will flash all 'eights' and the over-range output, pin 22, will go high. Low battery indication may also be provided by the addition of the simple circuit shown in figure 6.

Whilst the battery voltage is above 4.4V T_1 will be turned on via R1 and R2. Below this volage the base potential supplied by these resistors will be insufficient to turn on T_1 and it will then be turned on and off cyclically by the auto-zero output, causing the display to flash whatever reading is present.

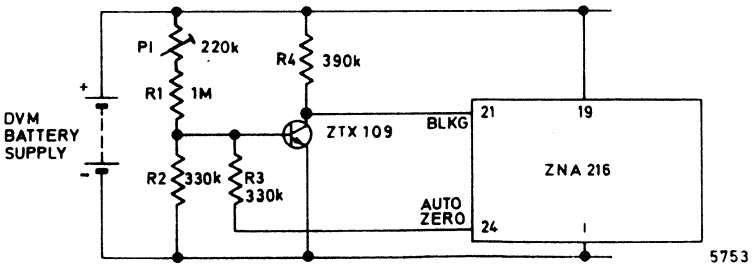


Figure 6. Low battery indication

ZNA216E/J

A PORTABLE D.V.M.

Figure 7 shows the circuit of a battery-powered D.V.M. based on the ZNA216, which uses readily available components. ZN424 op-amps are used for the integrator and comparator, whilst bipolar silicon transistors are used for the analogue switches. The basic sensitivity of the instrument is 4V, and additional ranges of 40V and 400V are provided by means of an input attenuator. Printed circuit board and component layouts for the D.V.M. are given in figures 8a to 9b.

However, this circuit design should by no means be considered as immutable. Since the analogue circuitry is external to the ZNA216 it may be configured to suit the designer's needs to give higher input impedance, increased sensitivity etc.

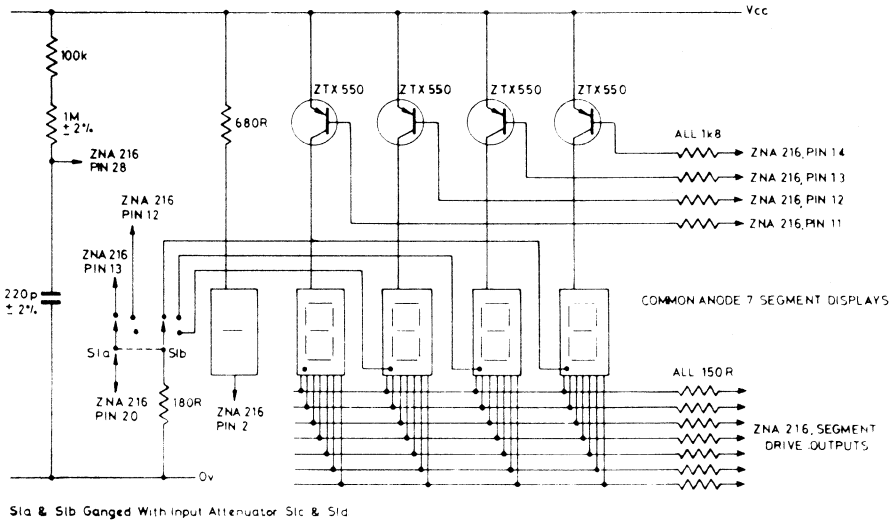


Figure 7a. Battery-powered D.V.M. circuit, display section.

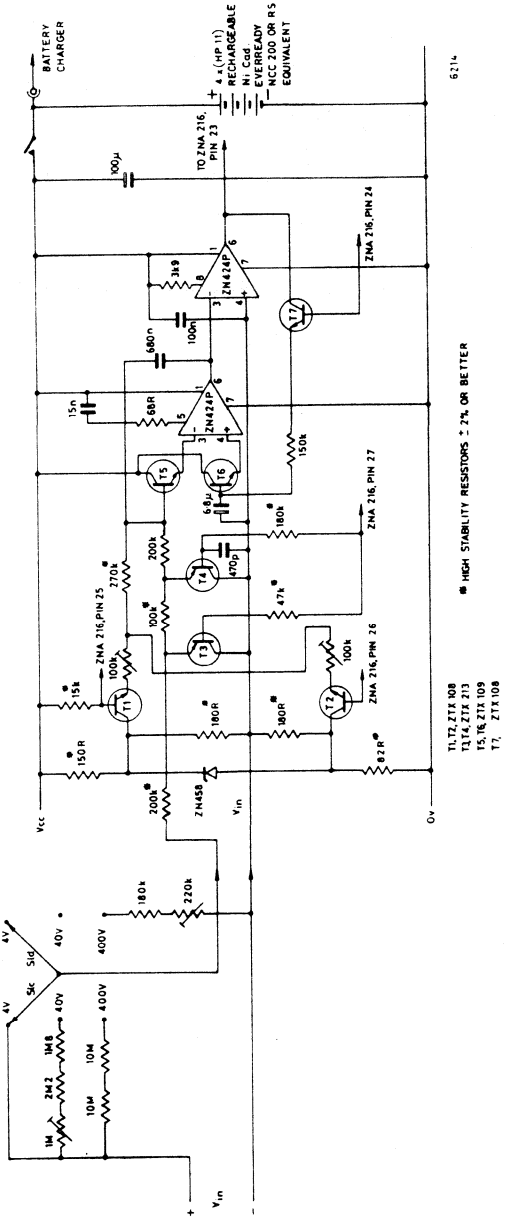
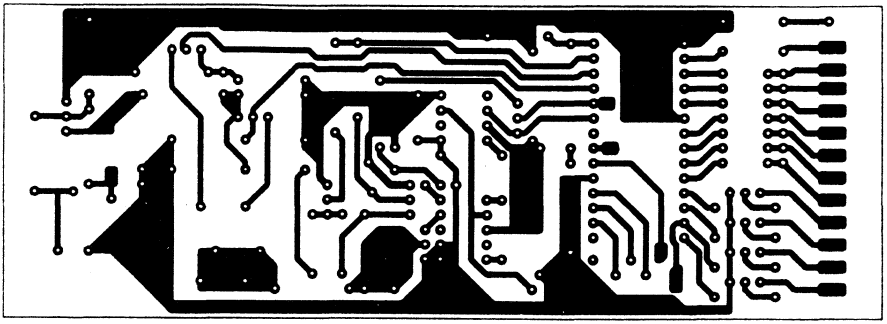


Figure 7b. Battery-powered D.V.M. circuit, analogue section.



6216

Figure 8a. D.V.M. Main Board

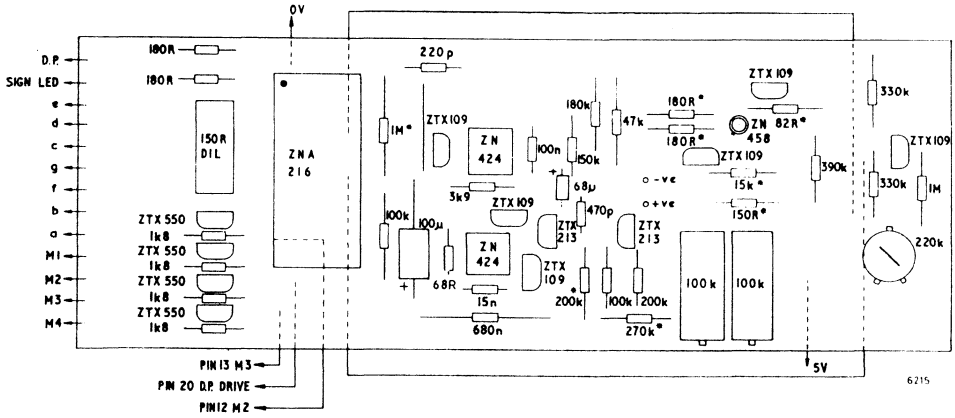


Figure 8b. Component Layout for Figure 8a.

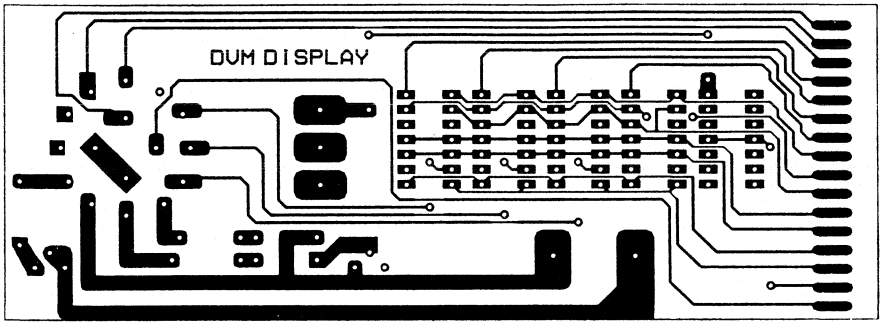


Figure 9a D.V.M. Display Board

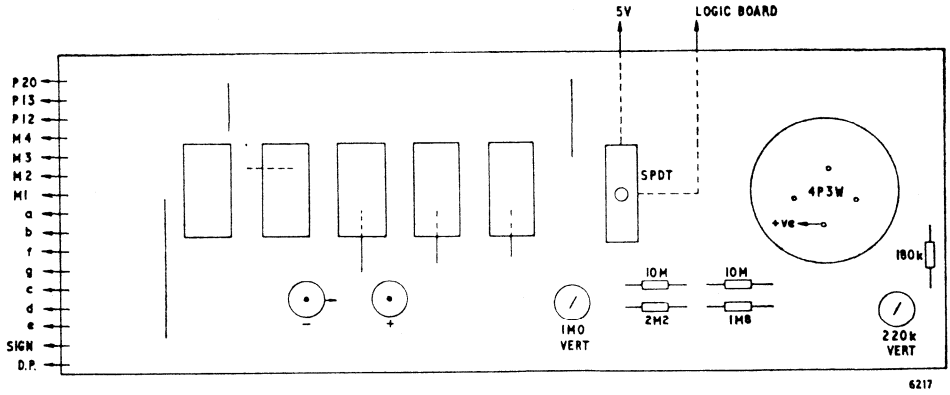


Figure 9b. Component Layout for Figure 9a.

MICROPROCESSOR INTERFACING

The ZNA216 may be used as a dual-slope A to D converter in data loggers and other data acquisiton systems, where its $3\frac{3}{4}$ decade range offers a resolution comparable to a 13 bit binary ADC, but in a more convenient BCD format.

Figure 10 is a block diagram which illustrates how the ZNA216 may be interfaced to an 8-bit microprocessor. The principle of operation is that the four multiplexed BCD digits of the ZNA216, plus the sign and overrange bits, are stored in four 4-bit latches so that they are available in parallel form. The contents of the latches can then be read into the microprocessor as two 8-bit words. The latches used are type 74173 which have three-state outputs for direct connection to the μP data bus. Data is clocked into the latches using the positive-going edge of the appropriate digit drive outputs.

The latches are treated as two memory locations by using an address decoder which is connected to their output enable pins. In this way data can be read out of the latches just as from any other memory locations. Once data is in the latches it may be read out whilst the ZNA216 performs the next measurement, thus eliminating any waiting time. The only time when data cannot be read out of the latches is just after the ZNA216 has completed a measurement. At this time the data in the internal latches of the ZNA216 will have been updated and the data in the 74173s may thus be changing. The data in the latches will be stable after two multiplexed cycles of the ZNA216, which is 4 ms if a 20 kHz clock is used.

Since the auto-zero output of the ZNA216 goes high when a measurement has been completed this output may be used as a BUSY signal. Data should not be read from the 74173 latches until at least 4 ms after the auto-zero output has gone high.

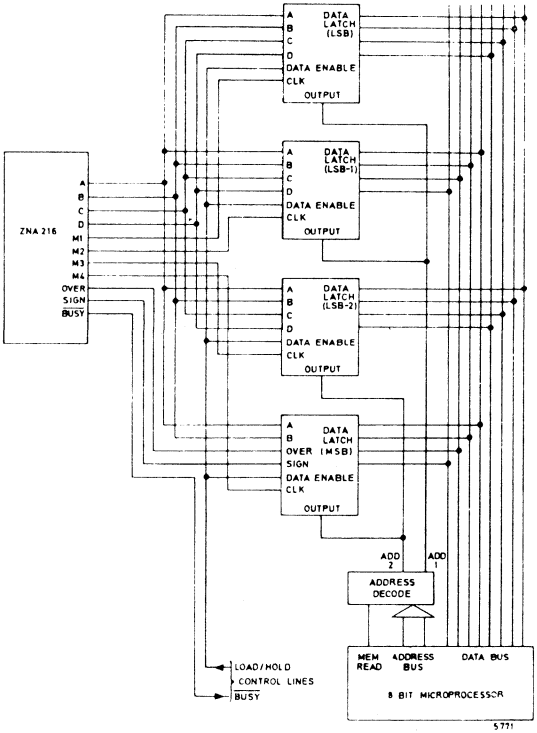
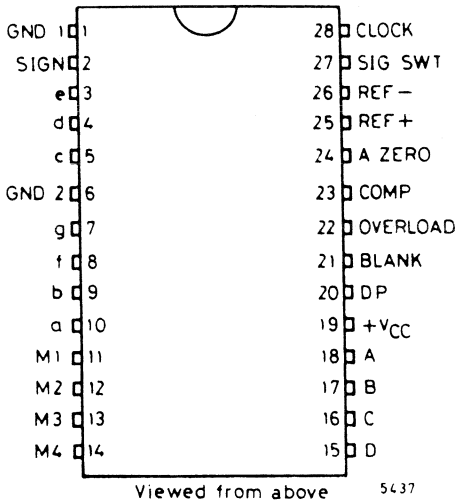
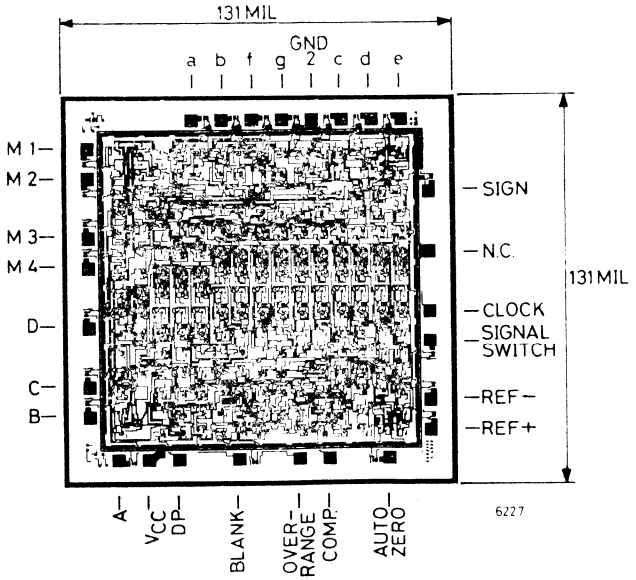


Figure 10. Interfacing the ZNA216 to a Microprocessor

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



3. Precision Voltage References

Contents

PRODUCT SELECTION GUIDE
PRECISION VOLTAGE REFERENCES

TYPE	REFERENCE VOLTAGE (V)	TEMPERATURE COEFFICIENT (ppm)	REFERENCE CURRENT (mA)	OPERATING TEMPERATURE RANGE (°C)	TRIMMABLE ±3 OR ±5 %	FEATURES	PAGE
ZN404	2,45	146	2-120	0 to 70	-	Very low cost	3-5
ZN423	1,26	30	1,5-12	0 to 70	-	Low R.M.S. noise voltage	3-9
ZN458	2,45	100	2-120	0 to 70	-	No shaping capacitor required	3-17
ZN458 A	2,45	50	2-120	0 to 70	-	No shaping capacitor required	3-17
ZN458 B	2,45	30	2-120	0 to 70	-	No shaping capacitor required	3-17
ZN REF 025 A SERIES	2,49	50	0,15-10	-55 to +125	+		3-25
ZN REF 025 B SERIES	2,49	30	0,15-10	-20 to +85	+		3-25
ZN REF 025 C SERIES	2,49	25	0,15-10	0 to 70	+		3-25
ZN REF 040 A SERIES	4,01	01	0,15-10	-55 to +125	+	Available in 3 initial tolerances. 1, 2 and 3%	3-29
ZN REF 040 B SERIES	4,01	30	0,15-10	-20 to +85	+		3-29
ZN REF 040 C SERIES	4,01	25	0,15-10	0 to 70	+		3-29
ZN REF 050 A SERIES	4,98	50	0,15-10	-55 to +125	+	ZN REF SERIES parts are mask-programmable between 2,5 and 10 V	3-33
ZN REF 050 B SERIES	4,98	30	0,15-10	-20 to +85	+		3-33
ZN REF 050 C SERIES	4,98	25	0,15-10	0 to 70	+		3-33
ZN REF 100 A SERIES	9,96	50	0,15-50	-55 to +125	+		3-37
ZN REF 100 B SERIES	9,96	30	0,15-50	-20 to +85	+		3-37
ZN REF 100 C SERIES	9,96	25	0,15-50	-0 to 70	+		3-37

FERRANTI semiconductors

ZN404

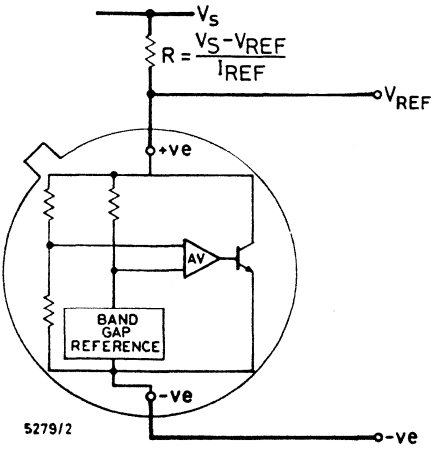
2·45 Volt Precision Reference Regulator

FEATURES

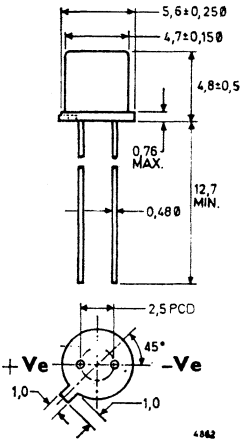
- Low temperature coefficient
- Low slope resistance
- Very good long term stability
- Low noise
- Internally shaped
- Tight tolerance
- Two pin package

DESCRIPTION

The ZN404 is a monolithic integrated circuit providing a precise stable regulator source of 2.45 volts in a two lead package without the need for an external shaping capacitor.



Circuit diagram



Lead Configuration
Dimensions in millimetres

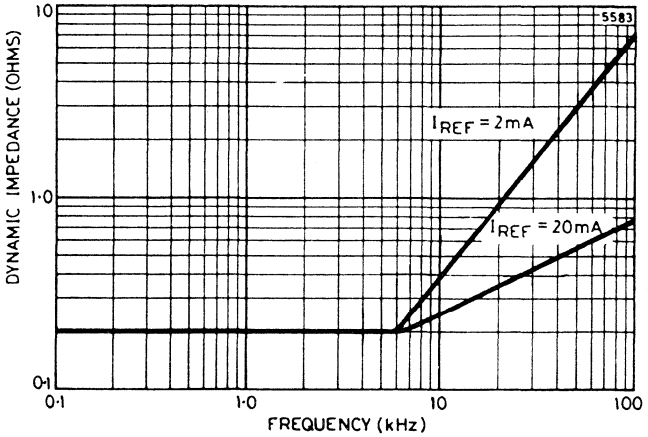
ZN404

MAXIMUM RATINGS

Dissipation .. .. 300 mW
Operating Temperature Range .. .. 0 to + 70°C
Storage Temperature Range .. .. –55 to +150°C

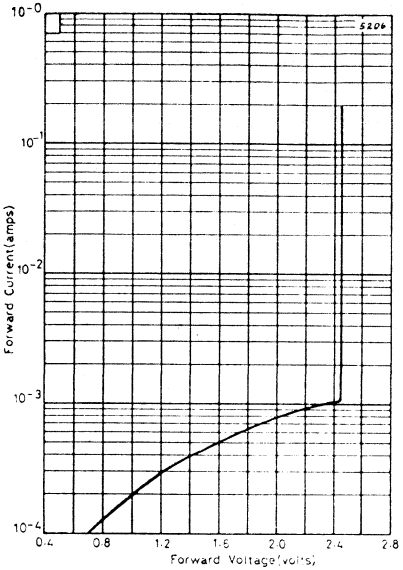
ELECTRICAL CHARACTERISTICS (at 25°C ambient temperature unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_{REF}	2.38	2.45	2.52	V	Measured at 2 mA
Slope Resistance	R_{REF}	—	0.2	0.4	Ω	
Reference Current	I_{REF}	2	—	120	mA	
Maximum Change in V_{REF}	ΔV_{REF}	—	6	25	mV	0 to +70°C

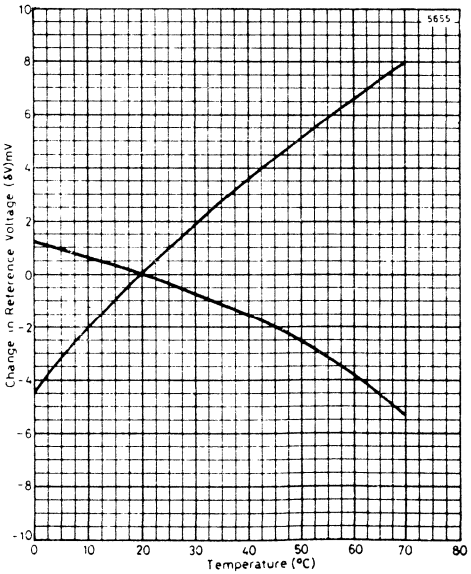


DYNAMIC IMPEDANCE

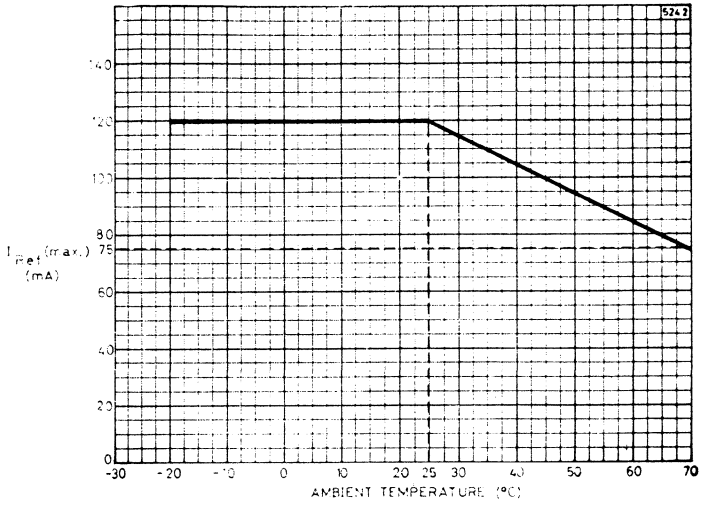
FORWARD CHARACTERISTIC
(Typical)



TEMPERATURE CHARACTERISTIC
(Typical)



DERATING CURVE



FERRANTI semiconductors

ZN423

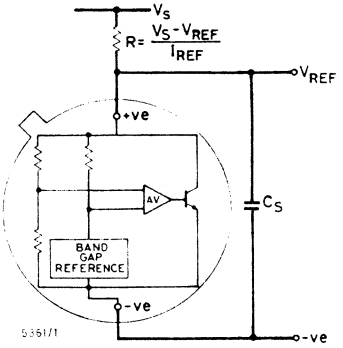
1·26 Volt Precision Voltage Reference Source

FEATURES

- Low voltage
- Low temperature coefficient
- Very good long term stability
- Low slope resistance
- Low RMS noise
- Tight tolerance
- High power supply rejection ratio
- Two pin package

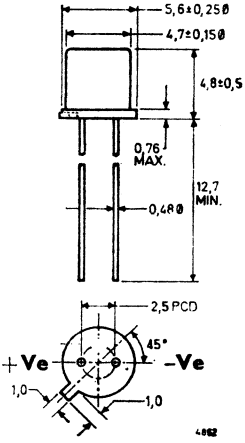
DESCRIPTION

The ZN423 is a monolithic integrated circuit utilising the energy band gap voltage of a base-emitter junction to produce a precise, stable, reference source of 1.26 volts. This is derived via an external dropping resistor for supply voltages of 1.5 volts upwards. The temperature coefficient of the ZN423, unlike conventional Zener diodes, remains constant with reference current. The noise figure associated with breakdown mechanisms is also considerably reduced.



Circuit diagram

PACKAGE OUTLINE



2 LEAD TO-18

Pinning configuration

Dimensions in millimetres

ZN423

ABSOLUTE MAXIMUM RATINGS

Reference current I_{REF}	20 mA
Operating temperature range ..	.. 0°C to + 70°C
	–55°C to +125°C
Storage temperature range	–65°C to +165°C

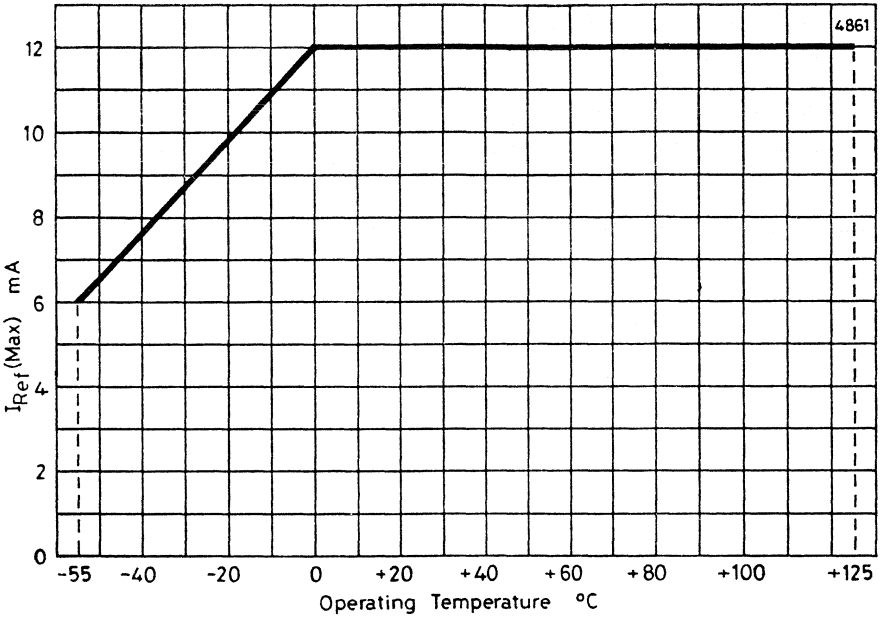
ELECTRICAL CHARACTERISTICS (at ambient temperature of 25°C unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output voltage	V_{REF}	1.2	1.26	1.32	V	
Slope resistance	R_{REF}	—	0.5	1.0	Ω	1
Reference current	I_{REF}	1.5	—	12	mA	
Temperature coefficient		—	30	—	ppm/°C	
Shaping capacitance	C_S	0.1	—	—	μF	
External resistance	R_{EXT}	100	—	—	Ω	2
R.M.S. noise voltage 1 Hz to 10 kHz		—	6	—	μV	
Power supply rejection ratio $V_{REF} = 1.26V$ $I_{REF} = 2 \cdot 5mA$ $V_{CC} = 5.0V$	PSRR	—	60	—	dB	3
V_{REF} drift at 125°C	σV_{REF}	— —	10 100	— —		ppm/1000 hours ppm/year

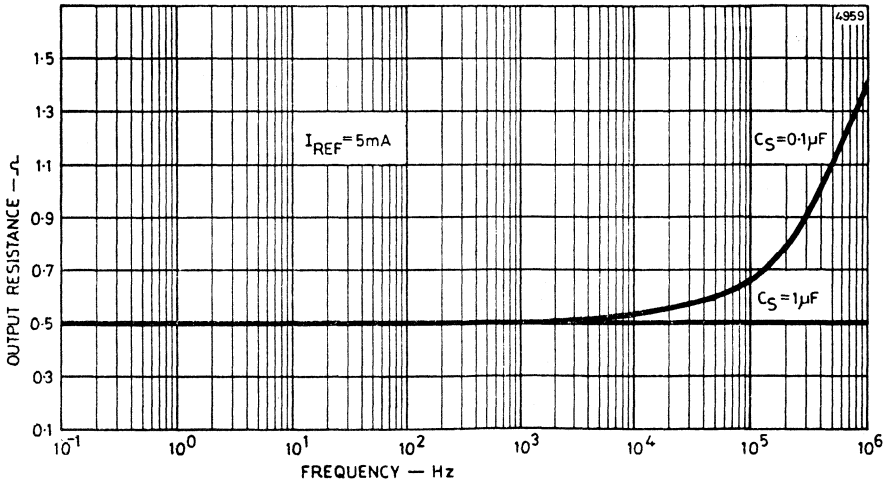
Note 1 $I_{REF} = 5$ mA
Note 2 $R_{EXT} = (V_{CC} - V_{REF})/I_{REF}$
Note 3 PSRR = R_{EXT}/R_{REF}

DERATING CURVE

Reference current I_{REF} (max.) vs Operating temperature.



Slope resistance vs Frequency (I_{REF} = 5 mA).



APPLICATIONS

1. 5 Volt, 0.5 Amp Power Supply.

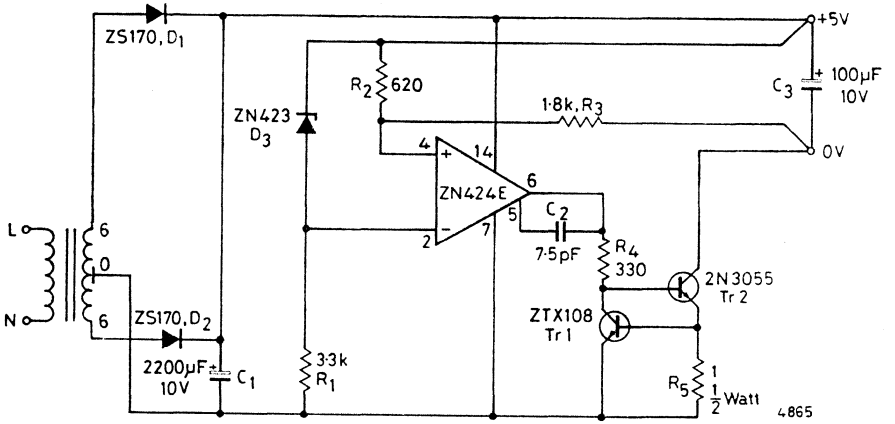


Figure 1.

This circuit is essentially a constant current source modified by the feedback components R_2 and R_3 to give a constant voltage output.

The output of the ZN424E need only be 2 volts above the negative rail, by placing the load in the collector of the output transistor Tr_2. Current circuit is achieved by Tr_1 and R_5 This simple circuit has the following performance characteristics:

Output noise and ripple (Full load) = 1 mV r.m.s.

Load regulation (0 to 0.5A) = 0.1%.

Temperature coefficient = ±100 ppm/°C.

Current limit = 0.65A.

2. 5 Volt, 1.0 Amp Power supply.

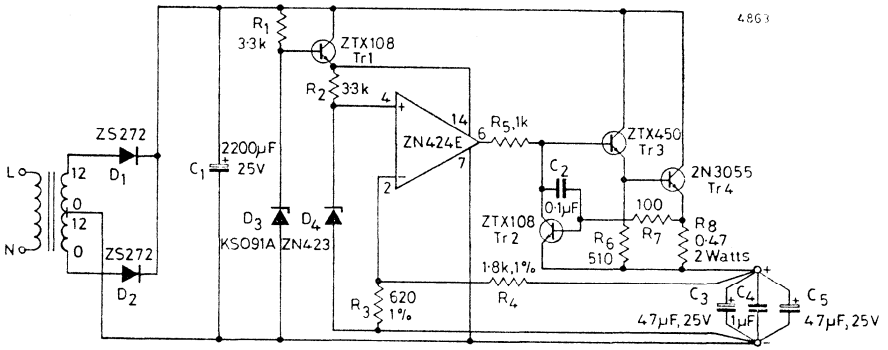


Figure 2.

The circuit detailed in Figure 2 provides improved performance over that in Figure 1. This is achieved by feeding the ZN423 reference and the ZN424E error amplifier from a more stable source, derived from the emitter-follower stage (Tr_1). The supply rejection ratio is improved by the factor R_1/R_S, where R_S is the slope resistance of D_3. The output voltage is given by: $\frac{(R_3 + R_4)}{R_3} . V_{REF}$ and may be adjusted by replacing R_3 with a 220Ω and a 500Ω preset potentiometer.

The output is protected against short circuits by Tr_2 setting a current limit of 1.6A.

3. 0 to 12 Volt, 1 Amp Power Supply.

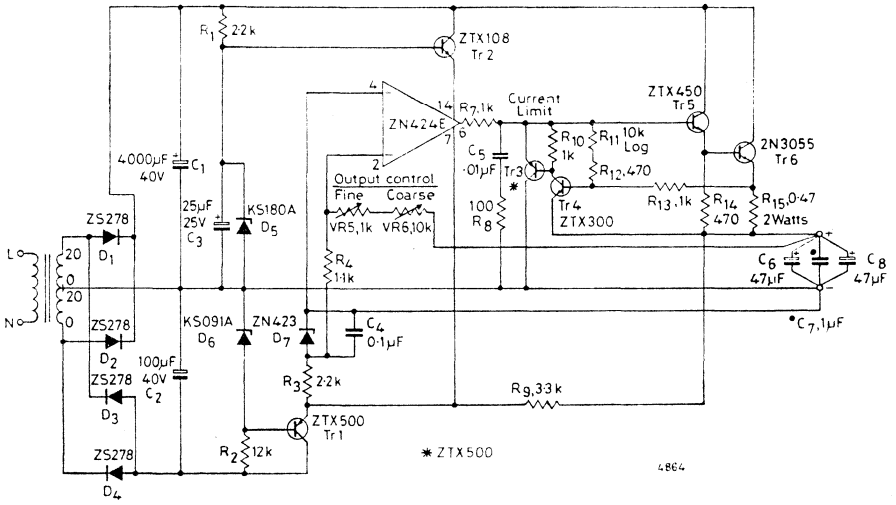


Figure 3.

The above circuit provides a continuously variable, highly stable voltage for load currents up to 1A.

The output voltage is given by: $V_O = \frac{(V_{R5} + V_{R6})}{R_4} V_{REF}$,

and is controlled by V_{R5} and V_{R6} which should be high quality components (preferably wire wound).

The emitter follower stages Tr_1 and Tr_2 buffer the bias and reference from the output stage. The negative rail allows the output to operate down to 0 volts.

The current limit stage monitors output current through R_{15}. As the potential across R_{15} increases due to load current, Tr_4 conducts and supplies base current for Tr_3, thus diverting part of the output from the ZN424E, via Tr_3 to Tr_5.

Shaping is achieved by the network C_5, R_8 together with the output decoupling capacitors which also maintain low output resistance at frequencies above 100 kHz.

The power supply has the following performance characteristics:

Output noise and ripple (Full load)	<100 μV r.m.s.
Output resistance (0 to 1 Amp)	1 mΩ
Temperature coefficient	±100 ppm/°C

4. Variable Current Source, 100 mA to 2 Amps.

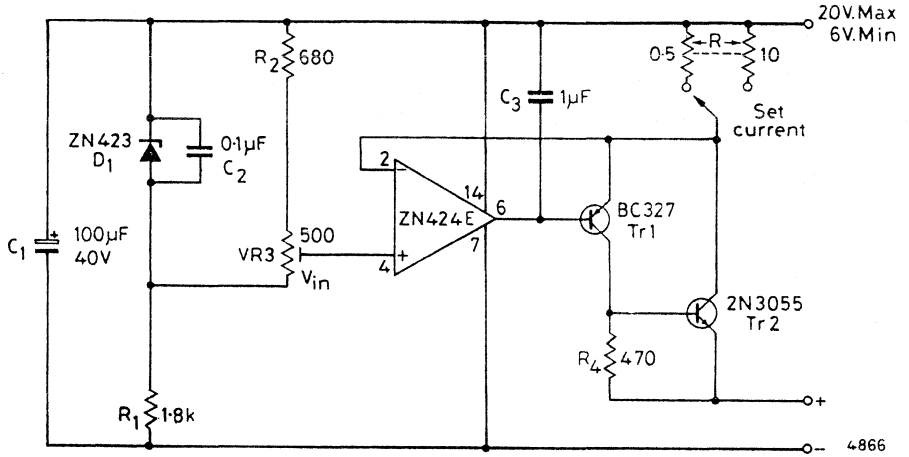


Figure 4.

In this circuit the output current is set by the resistor R in the collector of Tr_2, which may be switched to offer a range of output currents from 100 mA to 2A with fine control by means of VR3 which varies the reference voltage to the non-inverting input of the ZN424E.

The feedback path from the output to the inverting input of the ZN424E maintains a constant voltage across R, equal to $(V_{CC} - V_{in})$ and hence a constant current to the load given by $(V_{CC} - V_{in})/R$.

FERRANTI semiconductors

ZN458, A, B

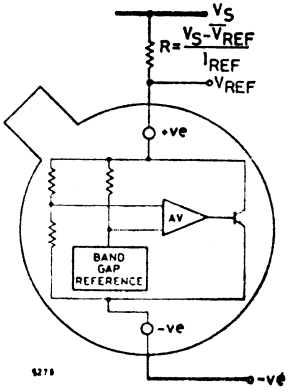
2·45 Volt Precision Reference Regulator

FEATURES

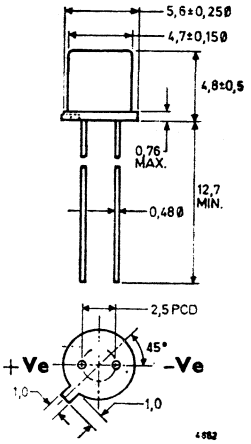
- Guaranteed 5 mV maximum deviation over full temperature range
- Low temperature coefficient 0·003%/°C
- Low slope resistance – 0·1Ω
- Very good long term stability – 10 ppm
- Low noise – 10 μV
- Internally shaped
- Tight tolerance ±1·43%
- Two pin package
- Wide operating current 2 – 120 mA

DESCRIPTION

The ZN458 is a monolithic integrated circuit providing a precise stable reference source of 2·45 volts in a two lead package without the need for an external shaping capacitor.



Circuit Diagram



Pinning Configuration
Dimensions in millimetres

ZN458, A, B

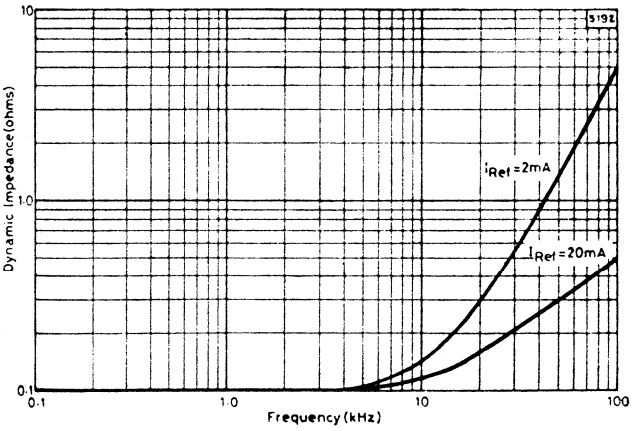
MAXIMUM RATINGS

Dissipation	300 mW
Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−55 to +150°C

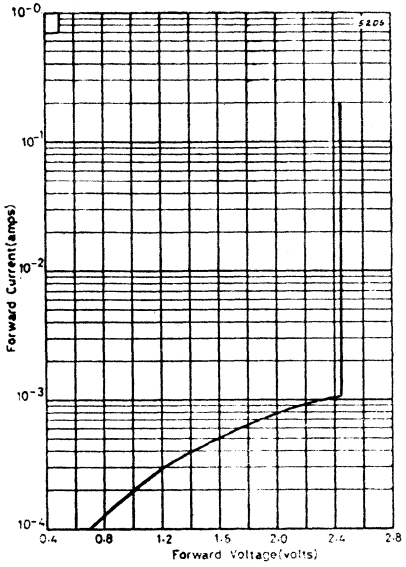
ELECTRICAL CHARACTERISTICS (at 25°C ambient temperature unless otherwise stated).

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage		V_{REF}	2·42	2·45	2·49	V	Measured at 2 mA
Slope Resistance		R_{REF}	—	0·1	0·2	Ω	
Reference Current		I_{REF}	2·0	—	120	mA	
Maximum Change in V_{REF}	ZN458	ΔV_{REF}	—	10	17	mV	0° to +70°C
	ZN458A		—	6	8·5		
	ZN458B		—	4	5		
RMS Noise Voltage 1 Hz to 10 kHz			—	10	—	μV	
V_{REF} Drift at 70°C			—	±10	—	ppm/1000 hours	

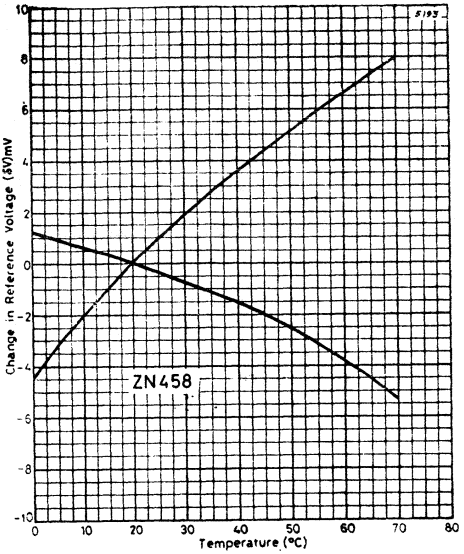
DYNAMIC IMPEDANCE



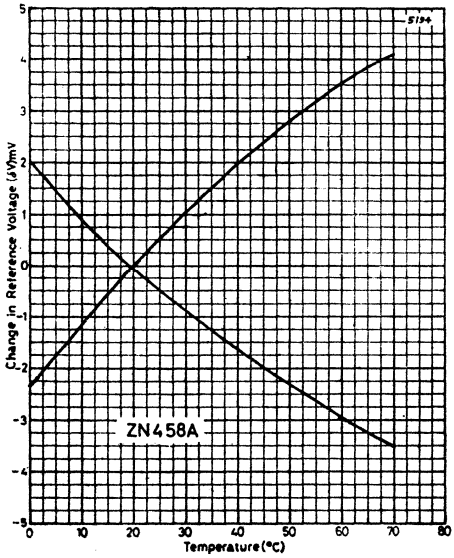
FORWARD CHARACTERISTIC

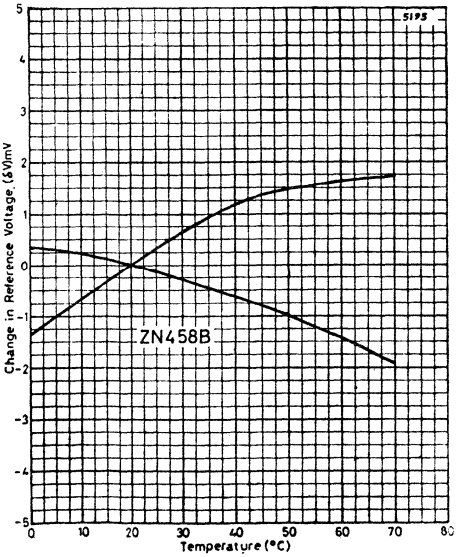


TEMPERATURE CHARACTERISTIC (Typical)

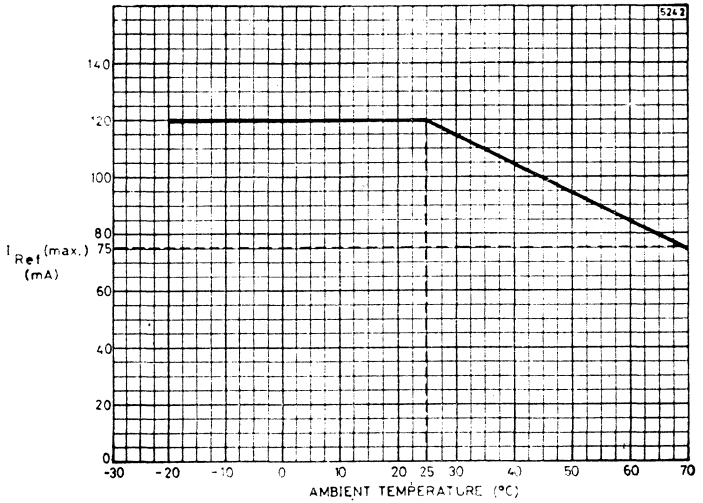


TEMPERATURE CHARACTERISTICS (Typical)





DERATING CURVE



FERRANTI semiconductors

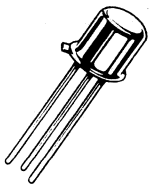
ZNREF SERIES

ZNREF Low Power Precision Reference Sources

ADVANCE PRODUCT INFORMATION

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in three temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available



TO-18 PACKAGE

TO-39 (6 Lead) PACKAGE

DESCRIPTION

The ZNREF series is a range of monolithic integrated circuits providing precise reference voltages from 2.5 volts (ZNREFO25) to 10 volts (ZNREF100).

The range features a knee current of 150 μA and operation over a wide range of temperatures and currents.

The devices are available in transistor packages with one of the pins offering a trim facility whereby the output voltage can be adjusted using the circuits overleaf—(Fig 2 for ZNREF100 and Fig 1 for other voltages).

ZNREF SERIES

Fig 1

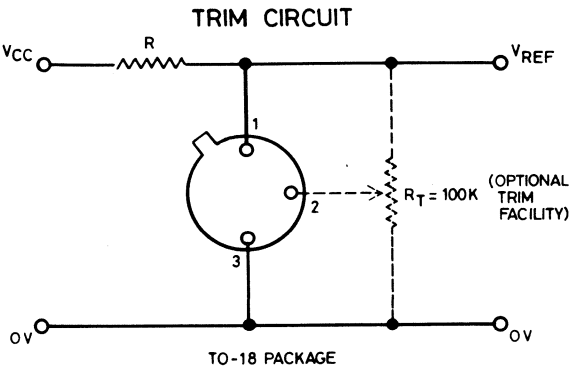
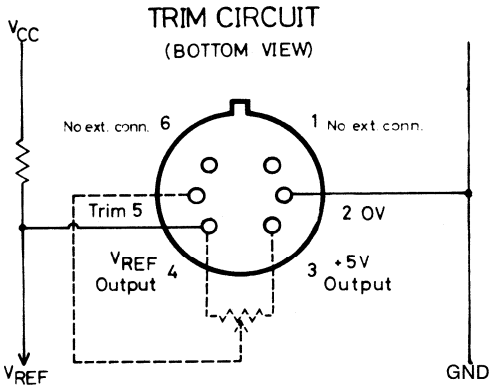


Fig 2



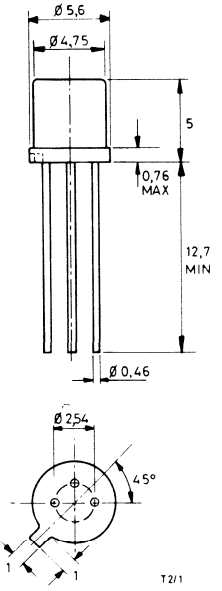
Type Number	Nominal Output Voltage(v)	Maximum Operating Current (mA)	Dynamic Impedance (Ω) Typ	Max	Trim Range	Package
ZNREF025	2.49	10	1.5	2.0	±5%	TO-18
ZNREF040	4.01	75	2.0	3.0	±5%	TO-18
ZNREF050	4.98	60	1.5	2.0	±5%	TO-18
ZNREF062	6.17	50	2.0	3.0	±5%	TO-18
ZNREF100	9.96	50	3.0	4.0	±2.5%	6 lead TO-39

ORDERING INFORMATION

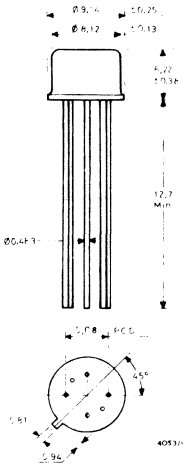
DEVICE	TOL %	T.C. PPm/°C	Temp. Range
ZNREF A1	1	50	−55°C to + 125°C
ZNREF A2	2		
ZNREF A3	3	80	
ZNREF B1	1	30	−20°C to +85°C
ZNREF B2	2		
ZNREF B3	3	48	
ZNREF C1	1	25	0°C to + 70°C
ZNREF C2	2		
ZNREF C3	3	40	

ZNREF SERIES

PACKAGE OUTLINE
Dimensions in mm.
(TO-18)

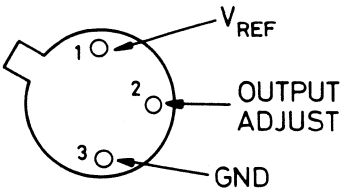


(TO-39)

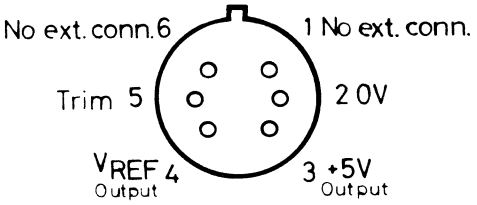


CONNECTION DIAGRAM

TO-18 Metal Can
(Bottom View)



TO-39 Metal Can
(Bottom View)



FERRANTI semiconductors

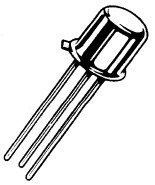
ZNREFO25

2.5 Volt Low Power Precision Reference Source

ADVANCE PRODUCT INFORMATION

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in three temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available

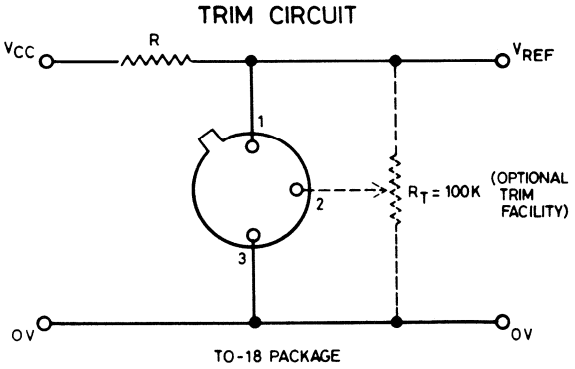


TO-18 PACKAGE

DESCRIPTION

The ZNREFO25 is a monolithic integrated circuit providing a precise, stable reference source of 2.5 volts in a three pin TO-18 metal can transistor package.

The use of the third pin is optional and enables V_{REF} to be trimmed by ±5%. This is useful for taking out system errors or setting V_{REF} to specific values, e.g. 2.500 volts for a standard calibration source or 2.56 volts for binary systems.



ZNREFO25

ABSOLUTE MAXIMUM RATINGS

Reference Current	10 mA
Power Dissipation	300 mW
Operating Temperature Range	See below
Storage Temperature Range	−55° to + 175°C
Soldering temperature for a maximum time of 10s	
within 1/16" of the seating plane	300°C
within 1/32" of the seating plane	265°C

TEMPERATURE DEPENDANT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance	Grade A -55 to 125°C		Grade B -20 to 85°C		Grade C 0—70°C		Units
			Typ	Max	Typ	Max	Typ	Max	
Output voltage change over relevant temperature range (see Note (a))	ΔV_{OT}	1% 2%	16.0	22.5	5.0	7.5	2.7	4.4	mV
		3%	25.0	36.0	7.8	12.9	4.2	7.2	
Output voltage temperature coefficient (See Note (b))	TCV_O	1% 2%	35	50	20	30	15	25	ppm/°C
		3%	56	80	30	48	24	40	

ELECTRICAL CHARACTERISTICS (T_A = 25°C and Pin 2 o/c unless otherwise noted)
(LOAD should be less than 220pF or greater than 22nF)

Parameter	Symbol	Min	Typ	Max	Units	Comments
Output Voltage 1% Tolerance (A1 B1 C1) 2% Tolerance (A2 B2 C2) 3% Tolerance (A3 B3 C3)	Vo	 2.465 2.440 2.415	 2.49 2.49 2.49	 2.515 2.540 2.565	V	I_{REF} = 150μA
Output Voltage Adjustment Range	V_{OR}	—	±5	—	%	R_T = 100 kohms
Change in TCV_o with output Adjustment	TCV_{OR}	—	.8	—	ppm/°C/%	
Turn on or "knee" current	I_{ON}	—	120	150	μA	Over full temperature range
Operating current range	I_{REF}	.15	—	10	mA	See Note (c)
Turn on settling time to within 0.1% of V_o	ton	—	5	—	μSec	Overshoot typically less than 1%
Output voltage noise (over the range 0.1Hz—10Hz)	$^{e}np\text{-}p$	—	50	—	μV	Peak to peak measurement
Dynamic Impedance	R_D		1.5	2.0	ohms	I_{REF} 0.5mA — 5mA See Note (d)

NOTES

a) OUTPUT CHANGE WITH TEMPERATURE(ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$V_{OT} = V_{max} - V_{min}$$

b) OUTPUT TEMPERATURE COEFFICIENT (TCVo)
The ratio of the output voltage change with temperature to the specified temperature range expressed in p.p.m/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

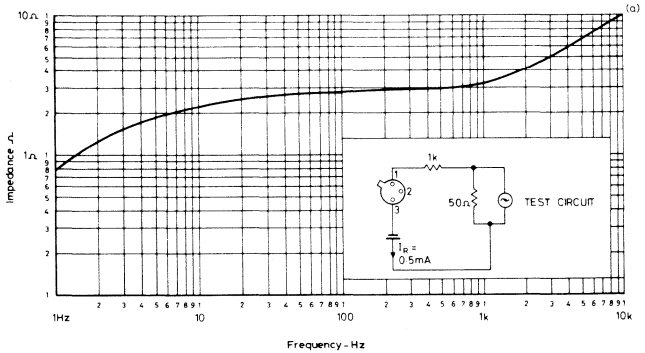
$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA}$ (typically)

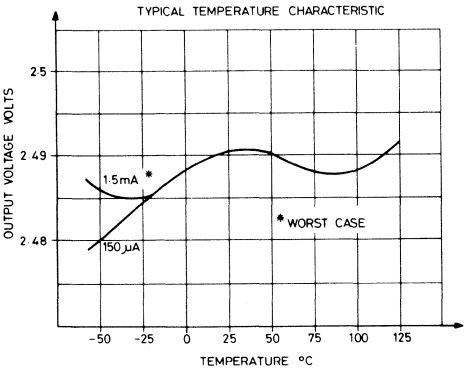
e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

$$\Delta V_{OL} = \frac{R_D \times 100}{V_o \times R_s} \text{ \% /V}$$

R_S = Source resistance.

DYNAMIC IMPEDANCE (TYPICAL)



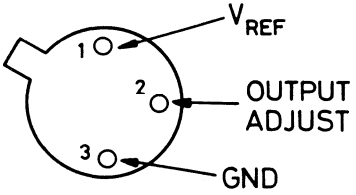


ZNREFO25

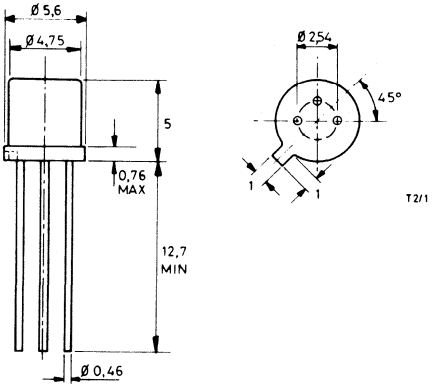
ORDERING INFORMATION

DEVICE	TOL %	T.C. PPm/°C	Temp. Range
ZNREF A1	1	50	−55°C to + 125°C
ZNREF A2	2		
ZNREF A3	3	80	
ZNREF B1	1	30	−20°C to +85°C
ZNREF B2	2		
ZNREF B3	3	48	
ZNREF C1	1	25	0°C to + 70°C
ZNREF C2	2		
ZNREF C3	3	40	

CONNECTION DIAGRAM
TO-18 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-18) Dimensions in mm.



BS.3934
JEDEC

SO-12A
TO-18

FERRANTI semiconductors

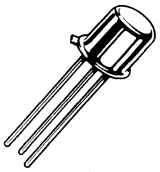
ZNREF040

4 Volt Low Power Precision Reference Source

ADVANCE PRODUCT INFORMATION

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in three temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available
- No external stabilising capacitor required



TO-18 PACKAGE

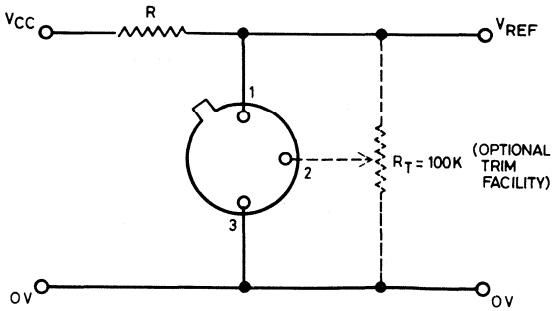
DESCRIPTION

The ZNREF040 is a monolithic integrated circuit providing a precise, stable reference source of 4 volts in a three pin TO-18 metal can transistor package.

The ZNREF040 is unconditionally stable under all load conditions without the need for an external shaping capacitor.

The use of the third pin is optional and enables V_{REF} to be trimmed by $\pm 5\%$. This is useful for taking out system errors or setting V_{REF} to specific values, e.g. 4.000 volts for a standard calibration source or 4.096 volts for binary systems.

TRIM CIRCUIT



TO-18 PACKAGE

ZNREF040

ABSOLUTE MAXIMUM RATINGS

Reference Current	75mA*
Power Dissipation	300mW
Operating Temperature Range	See below
Storage Temperature Range	−55 to +175°C
Soldering temperature for a maximum time of 10s	
within $^1/_{16}$" of the seating plane	300°C
within $^1/_{32}$" of the seating plane	265°C

*Above 25°C this figure should be linearly derated to 25mA at +125°C

TEMPERATURE DEPENDANT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance %	Grade A −55 to 125°C		Grade B −20 to 85°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range	ΔV_{OT}	1 & 2	25.6	36	8	12	4.3	7	mV
(see Note (a))		3	40	57	11	16.5	5.1	8.4	mV
Output voltage temperature coefficient	TCV_o	1 & 2	35	50	20	30	15	25	ppm/°C
(See Note (b))		3	56	80	26	40	18	30	ppm/°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C and Pin 2 o/c unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_O or					
1% Tolerance (A1 B1 C1)	V_{REF}	3.97	4.01	4.05	V	I_{REF} = 150μA
2% Tolerance (A2 B2 C2)		3.93	4.01	4.09	V	
3% Tolerance (A3 B3 C3)		3.98	4.01	4.13	V	
Output voltage adjustment range	V_{OR}	—	±5	—	%	R_T = 100kΩ
Change in TCV_o with output adjustment	TCV_{OR}	—	0.8	—	ppm/°C/%	
Turn-on or "knee" current	I_{ON}	—	120	150	μA	Over full temperature range
Operating current range	I_{REF}	0.15	—	75	mA	See Note (c)
Turn-on settling time to within 0.1% of V_o	t_{on}	—	5	—	μsec	Overshoot typically less than 1%
Output voltage noise (over the range 0.1Hz to 10Hz)	e_{np-p}	—	50	—	μV	Peak to peak measurement
Dynamic Impedance	R_D	—	2	3	Ω	I_{REF} 0.5mA to 5mA See Note (d)

NOTES

(a) OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{OT} = V_{max} - V_{min}$$

(b) OUTPUT TEMPERATURE COEFFICIENT (TCV_o)
The ratio of the output voltage change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C} \qquad \Delta T = \text{Full temperature change.}$$

(c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

(d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

$$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA (typically)}$$

(e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

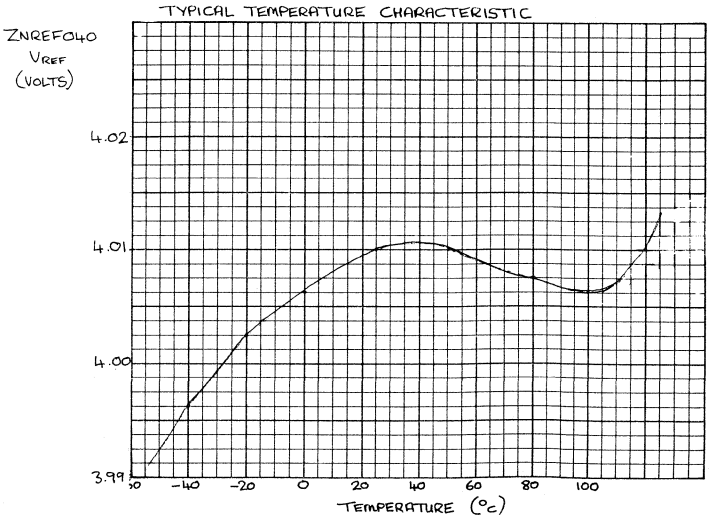
$$\Delta V_{OL} = \frac{R_D \times 100}{V_O \times R_S} \%/V \qquad R_S = \text{Source resistance}$$

DYNAMIC IMPEDANCE (TYPICAL)

DATA NOT AVAILABLE

AT TIME OF PRINTING

TYPICAL TEMPERATURE CHARACTERISTIC

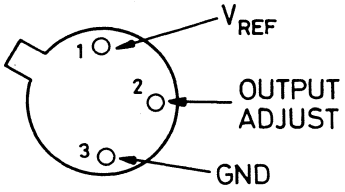


ZNREF040

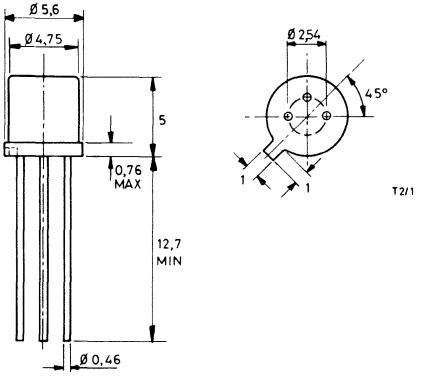
ORDERING INFORMATION

DEVICE	TOLERANCE (%)	T.C. (Max) – ppm/°C	Temperature Range
ZNREF040 A1	1	50	–55°C to +125°C
ZNREF040 A2	2		
ZNREF040 A3	3	80	
ZNREF040 B1	1	30	–20°C to +85°C
ZNREF040 B2	2		
ZNREF040 B3	3	40	
ZNREF040 C1	1	25	0°C to +70°C
ZNREF040 C2	2		
ZNREF040 C3	3	30	

CONNECTION DIAGRAM
TO-18 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-18) Dimensions in mm.



BS.3934
JEDEC

SO-12A
TO-18

FERRANTI semiconductors

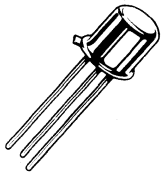
ZNREF050

5 Volt Low Power Precision Reference Source

ADVANCE PRODUCT INFORMATION

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in three temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available
- No external stabilising capacitor required

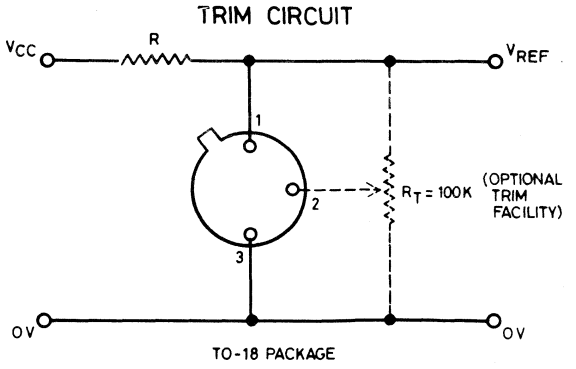


TO-18 PACKAGE

DESCRIPTION

The ZNREFO50 is a monolithic integrated circuit providing a precise, stable reference source of 5 volts in a three pin TO-18 metal can transistor package.
The ZNREFO50 is unconditionally stable under all load conditions without the need for an external shaping capacitor.

The use of the third pin is optional and enables V_{REF} to be trimmed by ±5%. This is useful for taking out system errors or setting V_{REF} to specific values, e.g. 5.000 volts for a standard calibration source or 5.12 volts for binary systems.



ZNREFO50

ABSOLUTE MAXIMUM RATINGS

Reference Current	60 mA
Power Dissipation	300 mW
Operating Temperature Range	See below
Storage Temperature Range	−55° to +175°C
Soldering temperature for a maximum time of 10s	
within 1/16" of the seating plane	300°C
within 1/32" of the seating plane	265°C

TEMPERATURE DEPENDANT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance	Grade A -55 to 125°C		Grade B -20 to 85°C		Grade C 0−70°C		Units
			Typ	Max	Typ	Max	Typ	Max	
Output voltage change over relevant temperature range (see Note (a))	ΔV_{OT}	1% 2%	32	45	10	15	5.4	8.8	mV
		3%	51	72	15.7	25.9	8.4	14.4	
Output voltage temperature coefficient (See Note (b))	TCV_O	1% 2%	35	50	20	30	15	25	ppm/°C
		3%	57	80	30	48	24	40	

ELECTRICAL CHARACTERISTICS (T_A = 25°C and Pin 2 o/c unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Comments
Output Voltage 1% Tolerance (A1 B1 C1) 2% Tolerance (A2 B2 C2) 3% Tolerance (A3 B3 C3)	Vo	 4.93 4.88 4.83	 4.98 4.98 4.98	 5.03 5.08 5.13	V	I_{REF} = 150μA
Output Voltage Adjustment Range	V_{OR}	—	±5	—	%	R_T = 100 kohms
Change in TCV_o with output Adjustment	TCV_{OR}	—	.8	—	ppm/°C/%	
Turn on or "knee" current	I_{ON}	—	120	150	μA	Over full temperature range
Operating current range	I_{REF}	.15	—	60	mA	See Note (c)
Turn on settling time to within 0.1% of V_o	ton	—	5	—	μSec	Overshoot typically less than 1%
Output voltage noise (over the range 0.1Hz−10Hz)	e_{np-p}	—	50	—	μV	Peak to peak measurement
Dynamic Impedance	R_D		1.5	2	ohms	I_{REF} 0.5mA −5mA See Note (d)

ZNREFO50

NOTES

a) OUTPUT CHANGE WITH TEMPERATURE(ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$V_{OT} = V_{max} - V_{min}$$

b) OUTPUT TEMPERATURE COEFFICIENT (TCVo)
The ratio of the output voltage change with temperature to the specified temperature range expressed in p.p.m/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

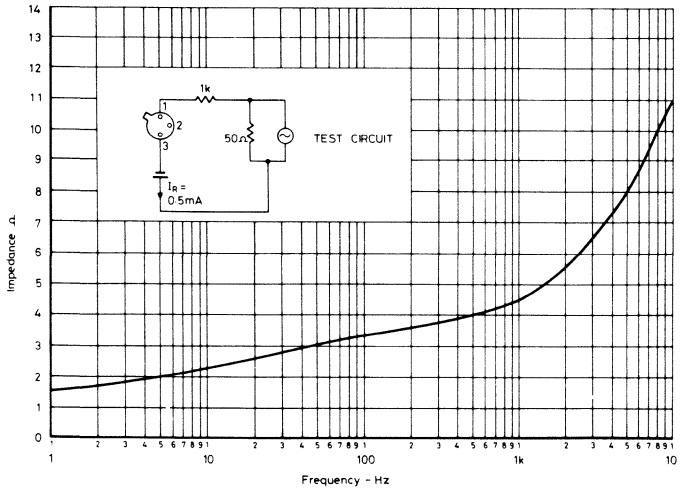
$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA}$ (typically)

e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

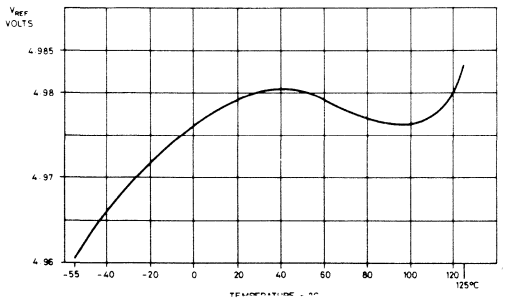
$$\Delta V_{OL} = \frac{R_D \times 100}{V_o \times R_s} \text{ \% /V}$$

R_S = Source resistance.

DYNAMIC IMPEDANCE (TYPICAL)



TYPICAL TEMPERATURE CHARACTERISTIC

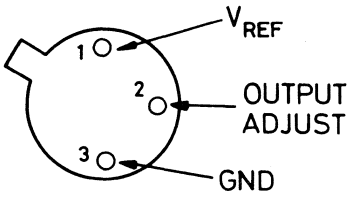


ZNREFO50

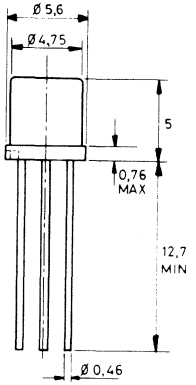
ORDERING INFORMATION

DEVICE	TOL %	T.C. PPm/°C	Temp. Range
ZNREF A1	1	50	−55°C to + 125°C
ZNREF A2	2		
ZNREF A3	3	80	
ZNREF B1	1	30	−20°C to +85°C
ZNREF B2	2		
ZNREF B3	3	48	
ZNREF C1	1	25	0°C to 70°C
ZNREF C2	2		
ZNREF C3	3	40	

CONNECTION DIAGRAM
TO-18 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-18) Dimensions in mm.



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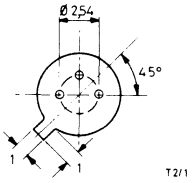


T2/1

SO-12A
TO-18

FERRANTI semiconductors

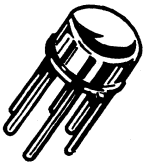
ZNREF100

10 Volt Low Power Precision Reference Source

ADVANCE PRODUCT INFORMATION

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in three temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available
- No external stabilising capacitor required

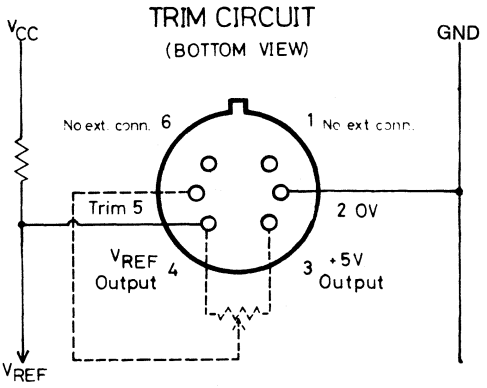


TO-39 (6 Lead) PACKAGE

DESCRIPTION

The ZNREF100 is a monolithic integrated circuit providing a precise, stable reference source of 10 volts in a six pin TO-39 metal can transistor package.
The ZNREF100 is unconditionally stable under all load conditions without the need for an external shaping capacitor.

The use of the third pin is optional and enables V_{REF} to be trimmed by ±2.5%. This is useful for taking out system errors or setting V_{REF} to specific values, e.g. 10,000 volts for a standard calibration source or 10.24 volts for binary systems.



ZNREF100

ABSOLUTE MAXIMUM RATINGS

Reference Current	50 mA
Power Dissipation	500 mW
Operating Temperature Range	See below
Storage Temperature Range	−55° to +175°C
Soldering temperature for a maximum time of 10s	
within 1/16" of the seating plane	300°C
within 1/32" of the seating plane	265°C

TEMPERATURE DEPENDANT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance	Grade A -55 to 125°C		Grade B -20 to 85°C		Grade C 0—70°C		Units
			Typ	Max	Typ	Max	Typ	Max	
Output voltage change over relevant temperature range (see Note (a))	ΔV_{OT}	1% 2%	64	90	20	30	10.8	17.6	mV
		3%	102	144	31	51	16	29	
Output voltage temperature coefficient (See Note (b))	TCV_O	1% 2%	35	50	20	30	15	25	ppm/°C
		3%	57	80	30	48	24	40	

ELECTRICAL CHARACTERISTICS (T_A = 25°C and Pin 2 o/c unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Comments
Output Voltage 1% Tolerance (A1 B1 C1) 2% Tolerance (A2 B2 C2) 3% Tolerance (A3 B3 C3)	Vo	 9.86 9.76 9.96	 9.96 9.96 9.96	 10.06 10.16 10.26	V	I_{REF} = 150μA
Output Voltage Adjustment Range	V_{OR}	—	±2.5	—	%	R_T = 100 kohms
Change in TCV_o with output Adjustment	TCV_{OR}	—	.8	—	ppm/°C/%	
Turn on or "knee" current	I_{ON}	—	120	150	μA	Over full temperature range
Operating current range	I_{REF}	.15	—	50	mA	See Note (c)
Turn on settling time to within 0.1% of V_o	ton	—	5	—	μSec	Overshoot typically less than 1%
Output voltage noise (over the range 0.1Hz—10Hz)	e_{np-p}	—	50	—	μV	Peak to peak measurement
Dynamic Impedance	R_D		3	4	ohms	I_{REF} 0.5mA —5mA See Note (d)

NOTES

a) OUTPUT CHANGE WITH TEMPERATURE(ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$V_{OT} = V_{max} - V_{min}$$

b) OUTPUT TEMPERATURE COEFFICIENT (TCVo)
The ratio of the output voltage change with temperature to the specified temperature range expressed in p.p.m/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

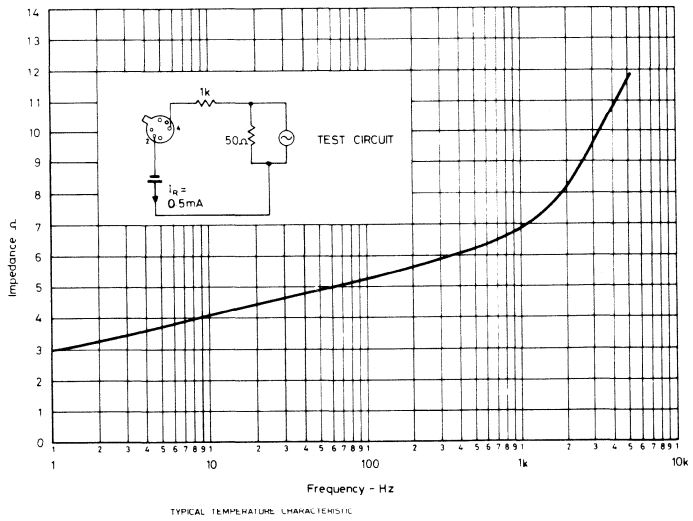
$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA}$ (typically)

e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

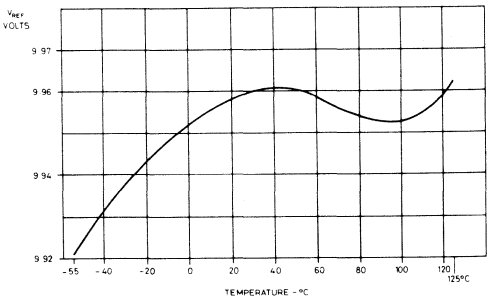
$$\Delta V_{OL} = \frac{R_D \times 100}{V_o \times R_s} \text{ \% /V}$$

R_S = Source resistance.

DYNAMIC IMPEDANCE (TYPICAL)



TYPICAL TEMPERATURE CHARACTERISTIC

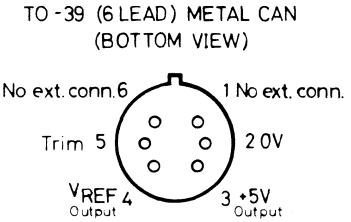


ZNREF100

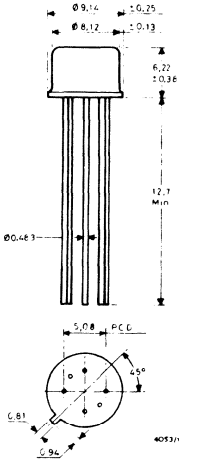
ORDERING INFORMATION

DEVICE	TOL %	T.C. PPm/°C	Temp. Range
ZNREF A1	1	50	−55°C to + 125°C
ZNREF A2	2		
ZNREF A3	3	80	
ZNREF B1	1	30	−20°C to +85°C
ZNREF B2	2		
ZNREF B3	3	48	
ZNREF C1	1	25	0°C to 70°C
ZNREF C2	2		
ZNREF C3	3	40	

CONNECTION DIAGRAM
TO-39 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-39) Dimensions in mm.



TO-39 (6 Lead) PACKAGE

4. Codec Circuits

Contents

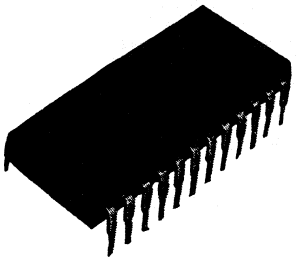
FERRANTI semiconductors

ZNPCM1

A Single Channel Codec Integrated Circuit

FEATURES

- Converts a delta-sigma modulated digital pulse stream into compressed 'A' law pcm and vice-versa.
- Enables realisation of a single channel codec circuit with minimum component usage.
- Pin selectable input/output interface providing either single channel operation at 64K bit/s (2,048 kHz external clock) or up to 2,048K bit/s (2,048 kHz external clock) for multi-channel burst format.
- Encoder and decoder can be clocked asynchronously (useful for pcm multiplex applications).
- Optional alternate digit inversion.
- Electrically and pin compatible with AY-3-9900
- Fully TTL compatible.
- Requires only a single 5V supply.



24-lead D.I.L.

DESCRIPTION

The ZNPCM1 integrated circuit is the result of a joint development programme between the British Post Office and Ferranti Electronics Limited. Designed for use in single channel codec systems the device accepts a delta-sigma modulated pulse stream at 2,048K bit/s (2,048 kHz external clock) and converts it into 8K sample/s compressed 'A' law pcm. In the decode direction the device performs the reverse function. A flexible serial pcm input/output interface is provided allowing operation in a single channel mode at 64K bit/s or at up to 2,048K bit/s (2,048 kHz external clock) for a multi-channel burst format. Digit delay control is provided to compensate for transmission delays. Optional alternate digit inversion is provided and the encoder and decoder can be clocked asynchronously if required for use in pcm multiplex applications.

Designed for use with a 2,048 kHz system clock, when operated with the required delta-sigma modulator and demodulator (see application report 'a single channel codec') The device performance complies with B.P.O. specification RC5549B and CCITT recommendations G711/G712 (1972).

The ZNPCM1 is guaranteed to operate up to 2,048 kHz and will typically operate up to 4 MHz. Operation is from a single 5V power supply with a typical power dissipation of 400 mW. All inputs and outputs are TTL compatible. Available in either a 24-lead ceramic (ZNPCM1J) or moulded (ZNPCM1CE) dual in-line package, the device is designed to operate over the temperature range 0°C to +70°C.

ZNPCM1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7 Volts
Input Voltage, V_{IN} .. .. +5.5 Volts
Operating Temperature Range .. 0°C to +70°C
Storage Temperature Range .. .. –65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
High-level Output Current, I_{OH}	—	—	–400	μA
Low-level Output Current, I_{OL}	—	—	4	mA
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating temperature range).

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		2.5	—	—	V
V_{IL}	Low level input voltage		—	—	0.8	V
V_{OH}	High level output voltage	V_{CC} = Min., I_{OH} = Max.	2.4	3.5	—	V
V_{OL}	Low level output voltage	V_{CC} = Min., I_{OL} = Max.	—	—	0.4	V
I_{IH}	High level input current	V_{CC} = Max., V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low level input current	V_{CC} = Max., V_{IL} = Max.	—	–1	–10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	80	110	mA
t_{vw}	Encoder timing vector pulse width		—	488	—	ns
t_{vv}	Encoding timing vector pulse width with edge variation		—	—	100	ns
t_{ww}	Decoder timing waveform pulse width		10	15.6	—	μs
f_{max}	Operating frequency		2.048	4	—	MHz
t_r & t_f	Rise and fall times	0.4V to 3V Transition	5	—	40	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns
C_I	Input capacitance		—	—	10	pF

PIN CONFIGURATIONS

Pin	Notation	Comments
1	0V	
2	MS	MODE SELECT (Note 1) Logic 0 = External pcm I/O interface timing Logic 1 = Internal pcm I/O interface timing
3	DS1	DECODER SELECT 1 and 2 (Note 2)
4	DS2	A two bit binary word selects required digit delay between encoder and decoder. DS1 DS2 Digit Delay 0 0 0 0 1 1 1 0 2 1 1 3
5	ADI	ALTERNATE DIGIT INVERSION Logic 0 = No. ADI Logic 1 = ADI
6	N.C.	NO CONNECTION
7	0V	
8	V_{CC}	
9	DSMO	DELTA-SIGMA MODULATED OUTPUT SIGNAL
10	SGN	SIGN BIT OUTPUT Sign bit from the encoder, used to operate on the delta-sigma modulator to reduce d.c. offset effects.
11	DSMI	DELTA-SIGMA MODULATED INPUT
12	SRF	SPECTRAL REDISTRIBUTION FUNCTION Output signal used to operate on the delta-sigma modulator to reduce low frequency quantisation noise.
13	PCMO	PCM OUTPUT
14	SGBI	SIGNALLING BIT INPUT Facility for adding signalling bit(s) to the output pcm stream.
15	ETV	ENCODER TIMING VECTOR A pulse defining the beginning of each frame used to maintain encoder timing.
16	PCMI	PCM INPUT
17	SGBO	SIGNALLING BIT OUTPUT Serial output for extracting signalling bit(s) from the incoming pcm stream.

PIN CONFIGURATIONS *(continued)*

Pin	Notation	Comments
18	DTW	DECODER TIMING WAVEFORM A pulse used to indicate to the decoder when the input pcm stream is in the input register (required only when external shift clocks are used).
19	SCE	ENCODER SHIFT CLOCK Used to control the output of serial pcm data from the encoder (when MS is low).
20	CLKD	DECODER MAIN CLOCK
21	CLKE	ENCODER MAIN CLOCK
22	SCD	DECODER SHIFT CLOCK Used to control the input of the serial pcm data to the decoder (when MS is low).
23	N.C.	NO CONNECTION
24	I.C.	INTERNAL CONNECTION Make no external connection to this pin.

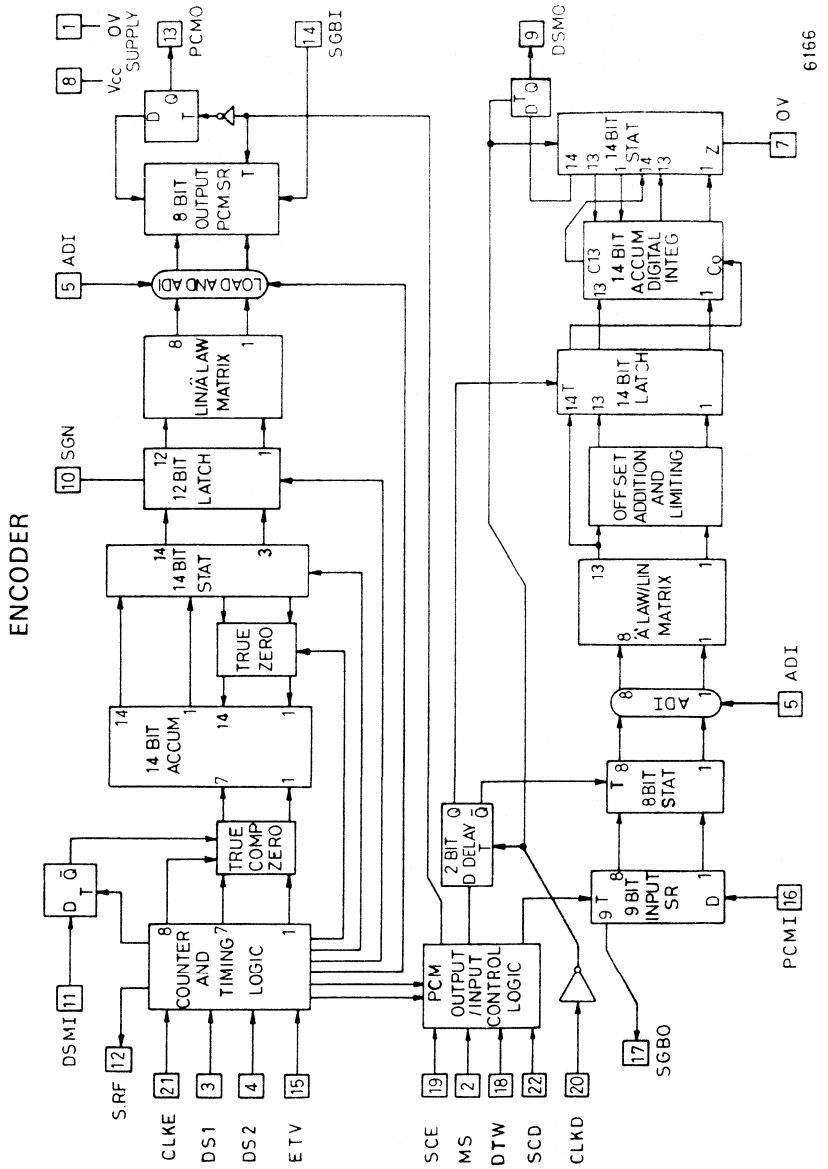
Notes:

1. With MS low (logic 0) serial PCM transmission is under the control of an externally generated shift clock SCE which can vary from 64 kHz to 2,048 kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGB1 input. In the high (logic 1) state the 8 bit PCM codeword will be transmitted at a rate of 64K bit/sec and each codeword will occupy the full 125 μs frame period with the leading edge of the first bit occurring at a time defined by the ETV pulse.

2. Delays through the transmission network, normally under the control of transmission switches, may cause the decoder input pulse stream to be delayed in time by a number of digits from the original transmitted pulse. To compensate for this delay two control inputs, DS1 and DS2, are provided. Consequently when MS is in the high state discrete digit delays of 0 to 3 periods may be selected resulting in a controlled shift of decoder timing in order to re-align Bit 1 in its correct position in the input register.

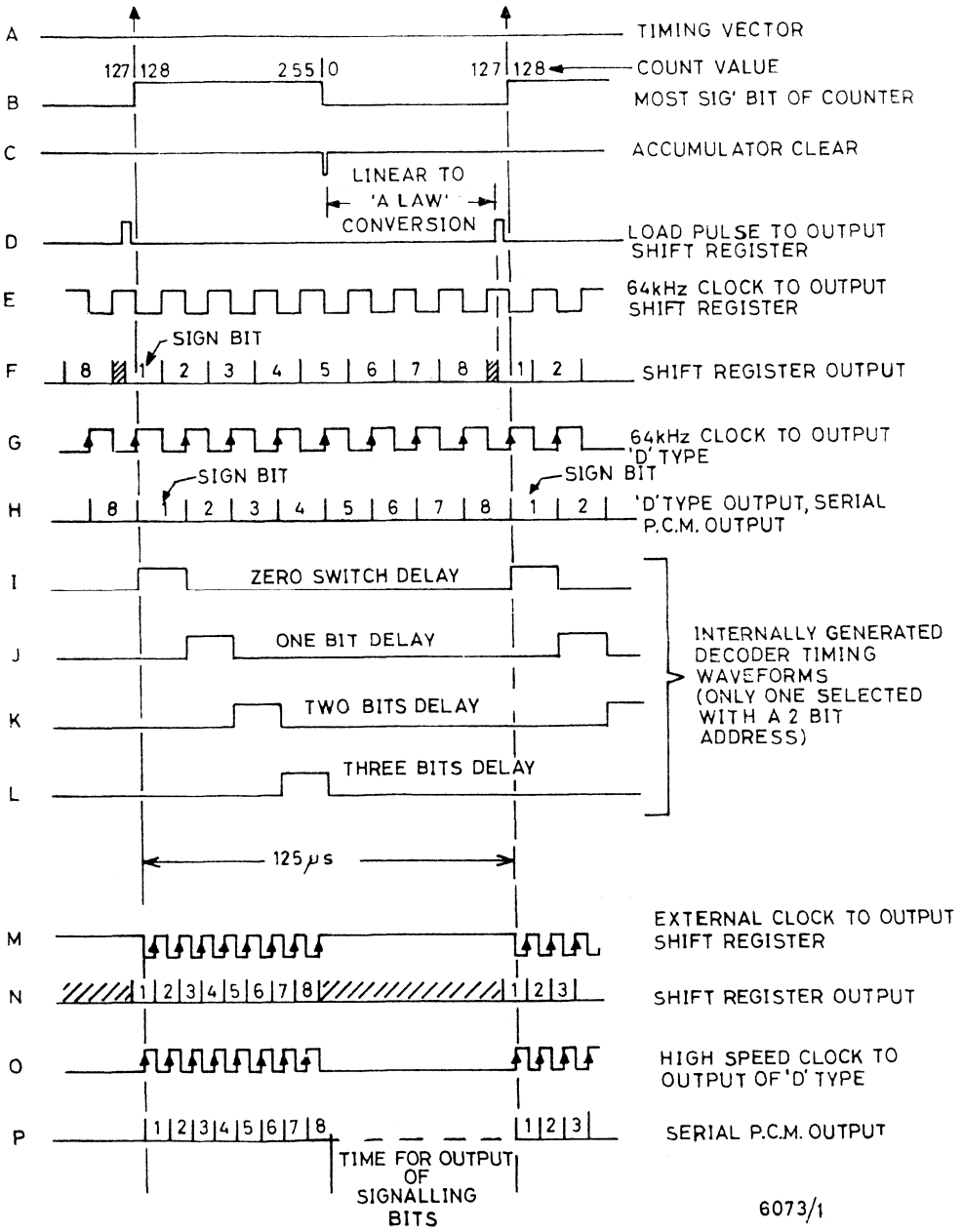
   When using an externally generated clock (i.e. MS in low state) an input shift clock (SCD) and timing waveform (DTW) are required to ensure that Bit 1 of the input codeword occupies its correct position in the input shift register.

FUNCTIONAL DIAGRAM



ZNPCM1

TIMING DIAGRAM
ENCODER



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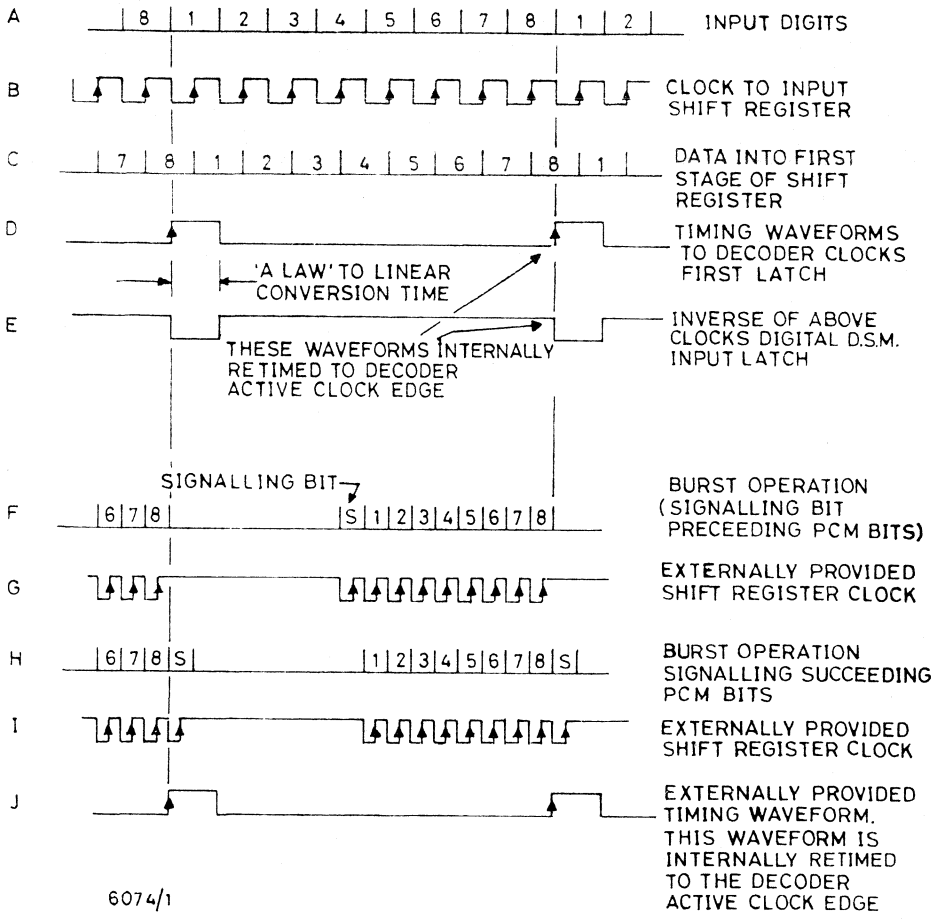
TIMING DIAGRAM

DECODER



ZNPCM1

APPLICATIONS INFORMATION

(a) A Single Channel Codec

Fig. 1 shows a block diagram of a single channel Codec using the ZNPCM1. The circuit accepts a band limited analogue input signal (300 – 3,400 kHz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The dsm bit stream is then converted by the ZNPCM1 into 8-bit compressed pulse code modulation (pcm) code words at the standard rate of 8K samples/sec, which is then converted into serial format for transmission serially at 64K bit/sec. External timing signals can be used to increase the transmission bit rate to 2,048K bit/sec. to allow for multiplexing in a burst format (see application b).

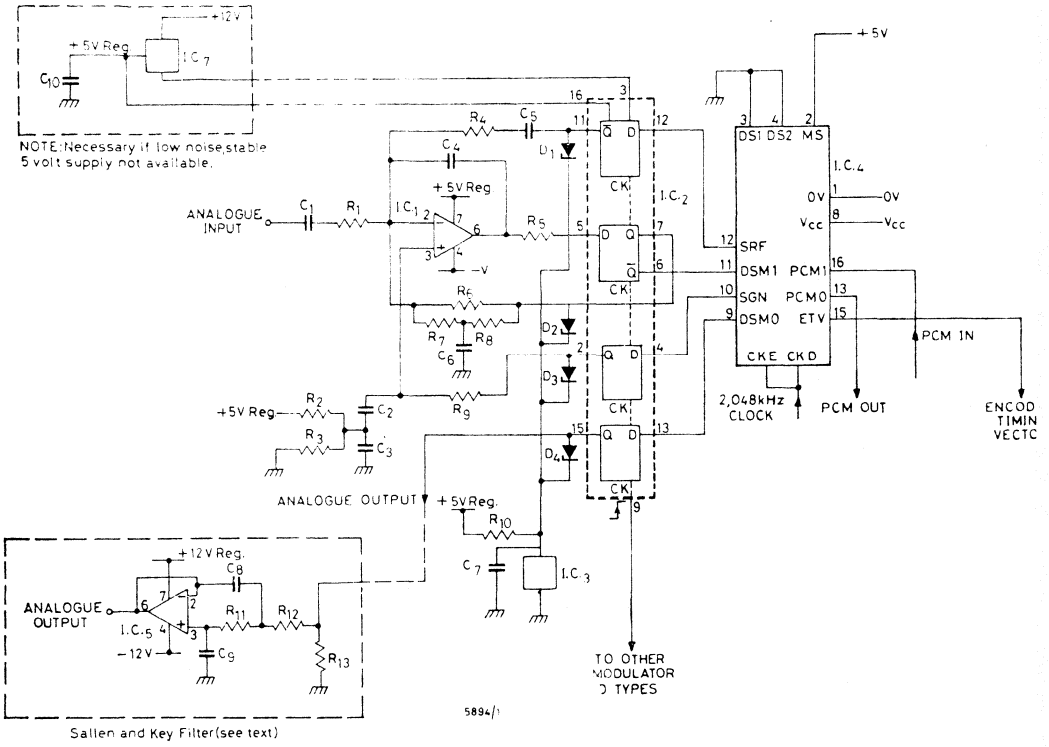


Fig. 1.

The pcm input interface will accept either a 64K bit/sec. bit stream or, by the application of external timing signals, a bit rate of 2,048K bit/sec. in burst format. This is then converted by the ZNPCM1 into a dsm bit stream at 2,048K bit/sec. The dsm demodulator accepts this bit stream and produces one of two precisely defined analogue levels per single bit sample. The analogue waveform can then be recovered via a low pass filter, cutting off just above the highest signal frequency to be recovered (3.4 kHz).

Output voltages of the dsm circuit are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the Codec, and clamping the high state output voltages to a 2.45V reference by the use of Schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, along with a small modulator/demodulator physical size by implementing the resistors and small capacitors as an in-line hybrid. More details of the operation of the dsm circuit are outlined in the Ferranti brochure 'A Single Channel Codec'.

An interesting development, again in co-operation with the British Post Office, is the integrated circuit dsm solution now approaching completion. This will reduce the circuitry surrounding the ZNPCM1 to a single I.C. and seven capacitors, the latter almost certainly to be made available as a single in-line hybrid.

The Codec performance related to CCITT criteria is outlined in Fig. 2.

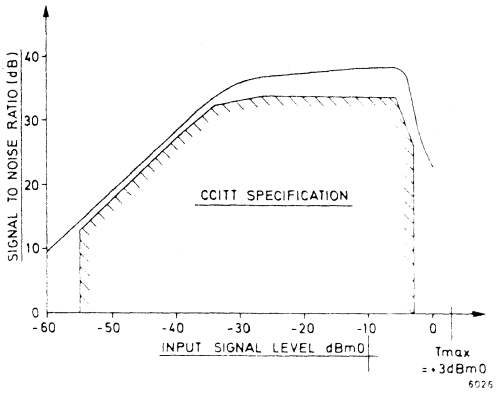


Fig. 2.

(b) A 30 Channel PCM Codec Solution

Traditionally the code conversion process on branch-to-main telephone exchange systems has been performed using multiplexed codecs. Historically the reason for this has been the codec specification where the signal-to-noise and gain-linearity constraints imposed on the systems have resulted in the use of expensive hybrid codecs. It might seem immediately obvious that the use of single channel codecs offers a more attractive solution, however a comparison of one of the major performance criteria is first of all necessary, that of power dissipation. Indeed, an initial comparison using the conventional 30 Channel PCM system shows the single channel codec approach to disadvantage. However, a more detailed analysis, using the single channel codecs in a power switching mode, shows this technique to be compatible with time shared codecs. This is described in section (d).

Let us first of all consider the system approach for using the single channel codecs in a 30 Channle PCM system by looking at Fig. 3.

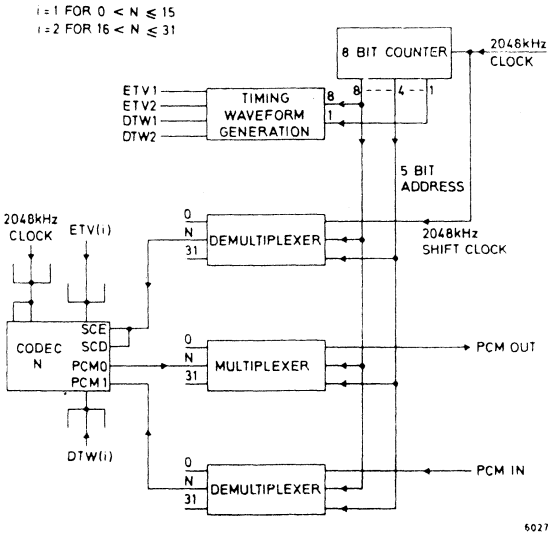


Fig. 3.

Fig. 3 shows how a 32 time slot (Note: A 30 Channel system has in fact, 32 time slots, the two additional ones being for signalling notation and synchronisation), 2,048K bit/sec. multiplex can be formed and decoded using 30 single channel codecs, when the two directions of transmission operate synchronously. Only the Nth codec is shown, connected to the 'Nth' port of the 32 port multiplexer and demultiplexers. When the 5-bit address equals N the 2,048 kHz shift clock is routed through the 'Nth' codec for eight clock pulses as shown in Fig. 4(a). The shift-in and shift-out clock terminals of the codec are commoned together. Since the shift-out terminal uses a negative active clock edge and the shift-in terminal uses a positive active clock edge the pcm digits for the two directions may be in exact time alignment. This is compatible with using the same 5-bit address for the multiplexer and the other demultiplexer.

The Encoder Timing Vector (ETV) and the Decoder Timing Waveform (DTW) may be derived from a counter driven by the 2,048 kHz clock and commoned across a number of codecs. For a 32 time slot multiplex, two sets of ETV's and DTW's should be generated with a half frame displacement as shown in Figs. 4(b) and 4(c). The first pair will supply ports 0 to 15 and the second pair ports 16 to 31, and consequently allowing the shift activity to be kept well clear of the timing waveforms for a given codec.

For a conventional 32 time slot codec ports 0 and 16 correspond to the synchronisation and signalling channels respectively.

Fig. 5 shows a similar arrangement for generating and decoding a 32 time slot multiplex when the two directions of transmission operate asynchronously. The two directions are operated quite independently but using similar principals to those previously discussed. It should again be noted that two sets of ETV's and DTW's should be used.

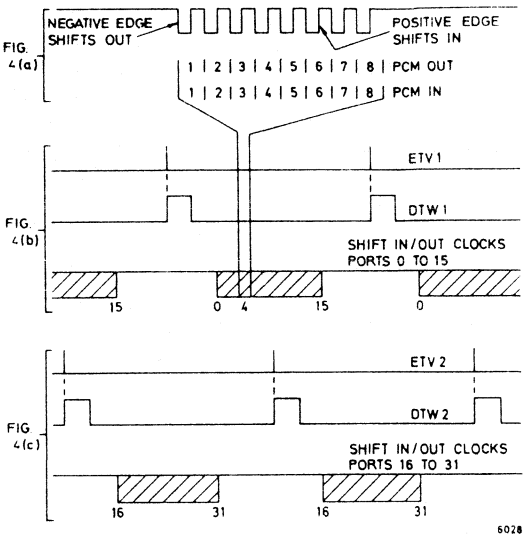
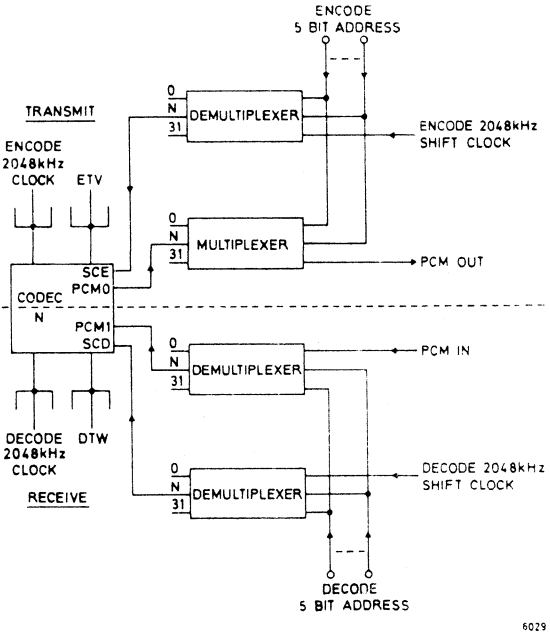

NEGATIVE EDGE SHIFTS OUT
POSITIVE EDGE SHIFTS IN
FIG. 4(a)
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM OUT
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM IN
ETV 1
DTW 1
FIG. 4(b)
SHIFT IN/OUT CLOCKS PORTS 0 TO 15
15
0 4
15
0
ETV 2
DTW 2
FIG. 4(c)
SHIFT IN/OUT CLOCKS PORTS 16 TO 31
16
31
16
31
6028

Fig. 4.


ENCODE 5 BIT ADDRESS
TRANSMIT
ENCODE 2048kHz CLOCK
ETV
0
N
31
DEMULTIPLEXER
ENCODE 2048kHz SHIFT CLOCK
MULTIPLEXER
PCM OUT
SCE
PCM0
CODEC
N
PCM1
SCD
DEMULTIPLEXER
PCM IN
DECODE 2048kHz CLOCK
DTW
RECEIVE
DEMULTIPLEXER
DECODE 2048kHz SHIFT CLOCK
DECODE 5 BIT ADDRESS
6029

(c) Switching Applications

The ZNPCM1 can be used in a variety of ways to satisfy switching applications. One technique is to operate directly on the 2,048K bit/s digit stream produced by the circuit arrangement shown in Fig. 3, where each codec has a defined time slot in the bit stream. An alternative technique would be to derive the address applied to the multiplexer and demultiplexer from the contents of a random access memory (RAM) which defines the codec to be used in a given time slot, in an exchange of PCM codewords between the codec and an intermediate store. In this mode of use the codec interface is effectively used as a time switch store.

The circuit shown in Fig 5 can be used without an intermediate store where again the codec addresses are derived from RAM's. The encode address defines the 'source' and the decode address the 'sink' in a given time slot. The decode address may be delayed with respect to the encode address by an integer number of 2,048 kHz clock periods to take account of any small, fixed switching delay.

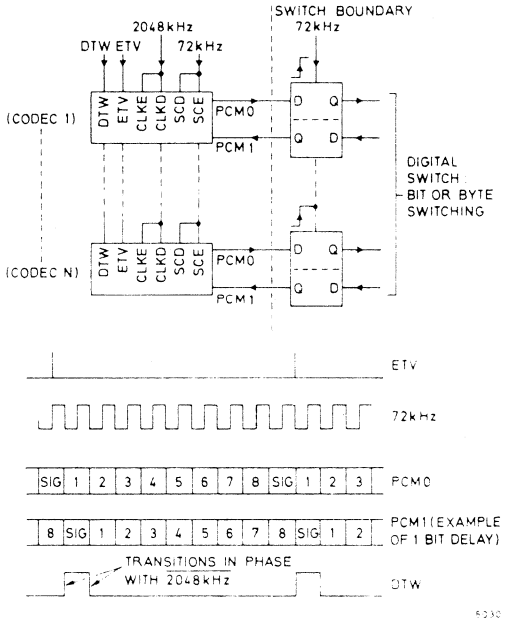


Fig. 6.

Fig. 6 shows an arrangement where the codecs input and output continuously, allowing 9-bits (8 PCM plus 1 signalling) to be exchanged in each 125 μs sample period. All the codecs may be supplied with common ETV, DTW, 2,048 kHz and 72 kHz waveforms. Each bit is retimed in the digital switch using a latch.

The digital switch may be operated using a bit switching arrangement, combined with the extraction and insertion of the signalling bits. Alternatively the bits may be reformatted into bytes and then byte switching performed. If the signalling is handled separately to the pcm codewords then a 64K bit/s rate can be used to and from the codec. This is compatible with using the codecs internal clock mode (MS = 1) in which case the only common timing waveforms required at the codec are the 2,048 kHz clock and the ETV.

(d) Power Switching

Comparisons have previously been made between shared and single channel codecs where these comparisions were reduced to one of power dissipation. Considerable power savings can be made by using the codecs in such a mode that they are only powered-up when required for use.

It is interesting to compare the power dissipation of an eight channel system using in one case eight ZNPCM1s in a power switching mode and, in the other case, one of the more popular time shared codecs which caters for eight channels. One single channel codec dissipates 600 mW and the time shared codec dissipates 1500 mW.

If the channel occupancy is p, then the average power dissipation per channel for the time shared codec is given by

$$W_{TS} = 1 - (1-p)^8 \frac{1500}{8} \text{ mW}$$

This assumes the time shared codec is only powered-up when any of the eight channels are required for use.

The average power dissipation per channel using the single channel codecs is simply given by,

$$W_{SC} = p.600 \text{ mW}$$

Fig. 7 shows a plot of power dissipation versus channel occupancy ; p for both approaches. The busy period average channel occupancies are likely to be in the range 0.2 to 0.15, clearly the lower end of the curves. Taking a figure of p = 0.06, for example, then the single channel codec dissipates only 36 mW per channel, approximately 50% less than the time shared codec. As the graph shows even for very busy exchanges given values for p of up to 0.3 shows the ZNPCM1 system to dissipate less power.

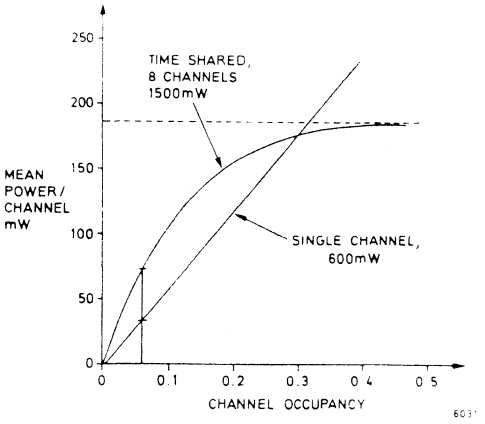
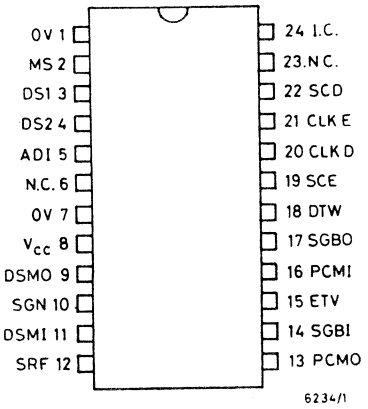


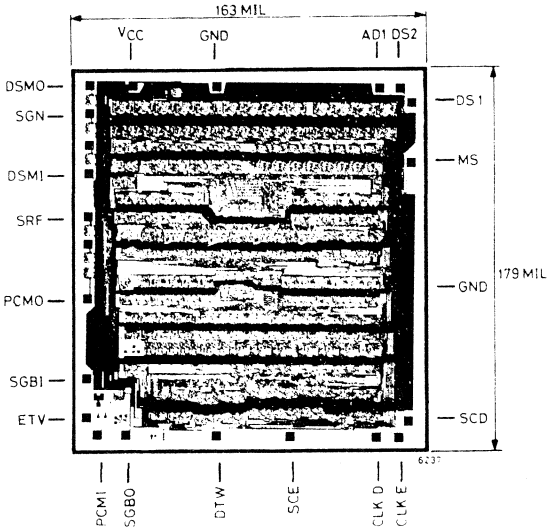
Fig. 7.

ZNPCM1

PIN CONNECTIONS



CHIP DIMENSIONS AND LYAOUT



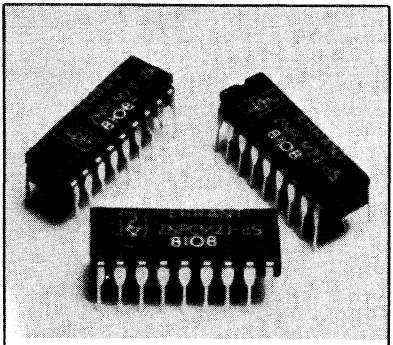
FERRANTI semiconductors

ZNPCM2

Delta Sigma Modulator/Demodulator I.C.

FEATURES

- Converts analogue input signal into delta sigma modulated (DSM) signal to be used as input for ZNPCM1 Codec I.C.
- Converts DSM signal produced by ZNPCM1 into level defined digital pulse stream for conversion to the analogue equivalent signal using low-pass filter techniques.
- High signal-to-noise ratio.
- Monolithic integrated circuit combining digital and analogue circuitry.
- Single 5V supply.
- 18-lead ceramic or modulated D.I.L. package.



18-LEAD D.I.L.

DESCRIPTION

The ZNPCM2 Delta Sigma Modulator/Demodulator (DSM) Integrated Circuit is designed for use in conjunction with the ZNPCM1 (manufactured by Ferranti Electronics Ltd.) or AY-3-9900 (manufactured by General Instruments Ltd.) Codec I.C's as the conversion unit in pulse code modulation communication systems. The ZNPCM2 modulator function converts analogue speech or data signals into a sampled signal having one bit per sample at a high sampling rate. The demodulator function produces an output signal having one of two well defined voltage levels in response to the signal bit per sample input signal. The original signal can then be recovered by low-pass filter techniques.

The ZNPCM2 provides excellent signal-to-noise ratio as a result of innovative circuit techniques developed at the British Post Office Research Centre. A rectangular input waveform designated as a spectral redistribution function (SRF) is provided and this modifies the quantisation noise spectrum, moving the noise components to higher frequencies. By varying the amplitude and phase of the SRF waveform, the net effects on the PCB outputs from the Codec system can be made to be ZERO if the SRF is sampled synchronously within the system. In addition a complex feedback network is utilised in the DSM circuit to provide increased feedback at low frequency which results in the relative attenuation of low frequency quantisation noise components below 32 kHz.

D.C. alignment to better than 0.01% at low signal ampitudes is achieved at the output by use of a feedback loop minimising both the DSM voltage offset and the digital code offset. This technique makes use of the fact that the PCM code words have a sign and magnitude format and the result eliminates the need for component trimming.

ZNPCM2

Designed using the same technology as the ZNPCM1 Codec I.C., the ZNPCM2 combines both linear and digital circuits on the same monolithic I.C. Packaged in an 18-lead ceramic (ZNPCM2J) or moulded D.I.L. (ZNPCM2E), the device is designed to operate over the the temperature range 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... +7 volts
Digital Input Voltage, $V_{IN(D)}$ ..... +5.5 volts
Analogue Input Voltage, $V_{IN(A)}$ ..... 4 volts pk-to-pk
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage	4.75	5.0	5.25	V
High-level Output Current, I_{OH} (Digital Outputs)	—	—	−400	μA
Low-level Output Current, I_{OL} (Digital Outputs)	—	—	4	mA
Analogue Output Impedance, Z_{AO}	—	100	—	Ω
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over the recommended operating temperature range).

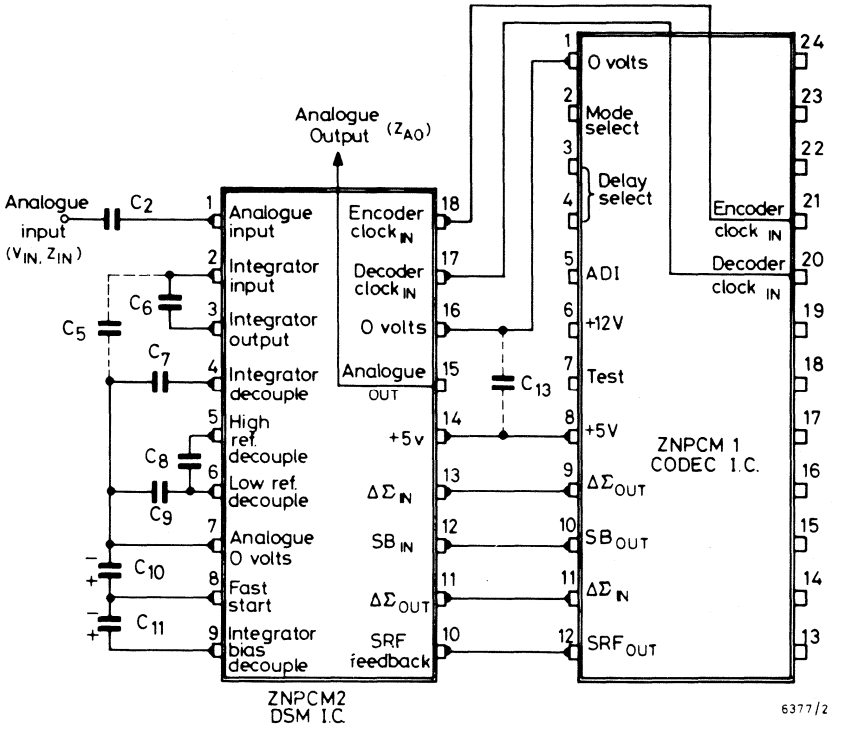
(a) Digital Inputs and Outputs.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2.3	—	—	V
V_{IL}	Low-level input voltage		—	—	0.8	V
V_{OH}	High-level output voltage	V_{CC} = Min, I_{OH} = Max.	2.4	4	—	V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max.	—	—	0.4	V
I_{IH}	High-level input current	V_{CC} = Max, V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low-level input current	V_{CC} = Max, V_{IL} = Min.	—	—	10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	24	—	mA
f	Operating frequency		—	2,048	—	kHz
t_r & t_f	Rise and fall time	0.4V − 3.0V transition	5	—	40	ns
t_{pd}	Propagation delay	Clock $\varnothing_E$ or $\varnothing_D$ to DSM output 2.5V level	—	40	60	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns

(b) Analogue Input and Output.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Analogue Input Voltage for 0dBm0	Peak-to-peak	—	1.4	—	V
Z_{IN}	Analogue Input Impedance	Measured at 1kHz	80	100	—	kΩ
V_C	D.C. Voltage across C_{11}	V_{CC} = Max.	—	±3.0	±3.0	mV

DSM CODEC INTERFACE



NOTES

1 The external high frequency decoupling between pins 5, 6 and 7 should be of minimal impedance (i.e. in the range of 1 to 20 MHz). Low loss capacitors connected via minimal conductor path lengths and inductances are required. Suitable capacitors are 0.22 μF monoblock types. Total connection length and resistance including capacitor leads should be as follows:

Pins 5 to 6 <10mm and <0.1Ω
Pins 6 to 7 <16mm and <0.1Ω

2 Analogue ground pin 7 and digital ground pin 16 must be linked externally. Ideally, this should be their only connection; however, if it is essential that the two 0V systems are connected at a point remote from the ZNPCM2 then pin 16 should remain connected to the analogue ground only.

3 Performance of the ZNPCM1 and ZNPCM2 is layout dependent and an optimum layout is shown on page 6. Capacitor C_5 and C_{13} are optional but may improve performance in some instances.

PERFORMANCE

The codec combination of the ZNPCM1 and ZNPCM2 meets all the performance requirements of the C.C.I.T.T. recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

(1) Idle Channel noise: −70dBm0p (See Fig. 1).
C.C.I.T.T. recommendation = −65dBm0p

(2) Signal-to-noise ratio and gain level linearity: Figs. 2(a) and 2(b) show the results using a 450 − 550kHz pseudo-random noise test.

(3) Intermodulation distortion: measured products are at least 10dB and on average 18dB better than C.C.I.T.T. recommendations.

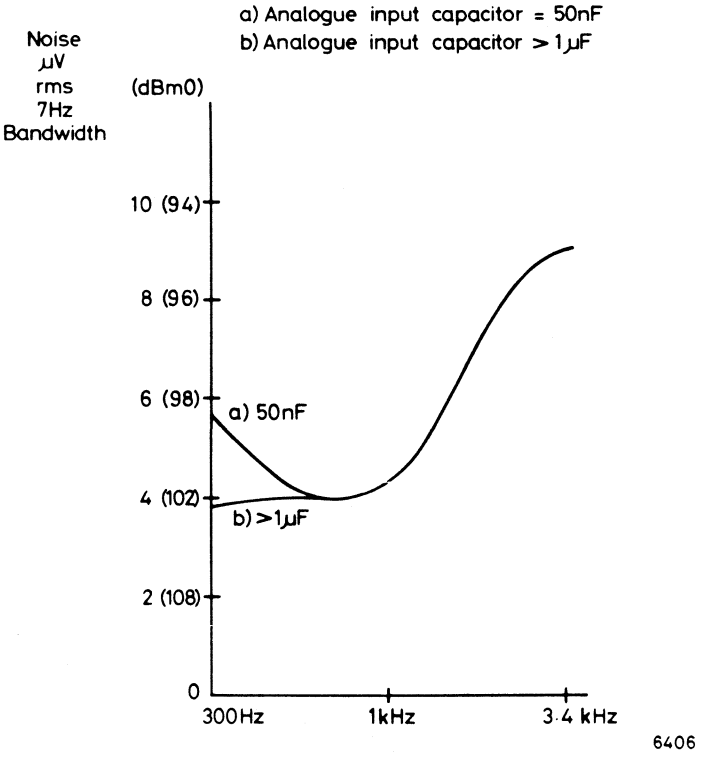


Fig. 1. Idle Channel Noise Spectrum

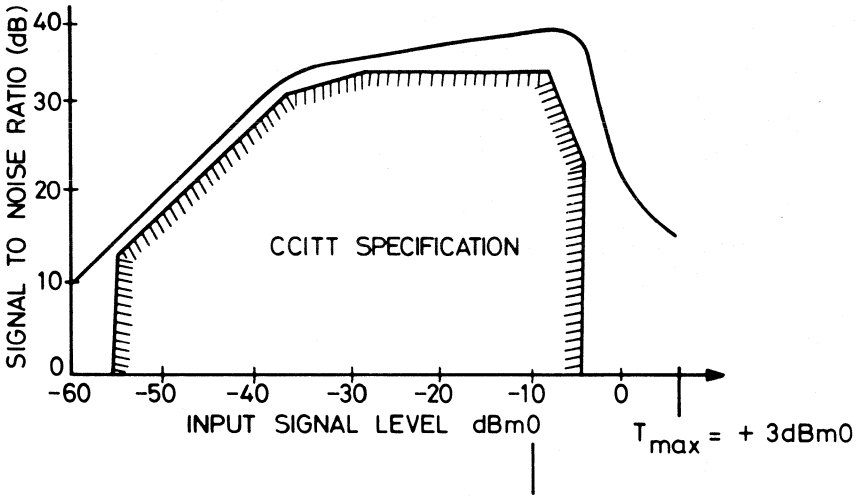


Fig. 2(a). Signal to Noise Ratio 'A Law'

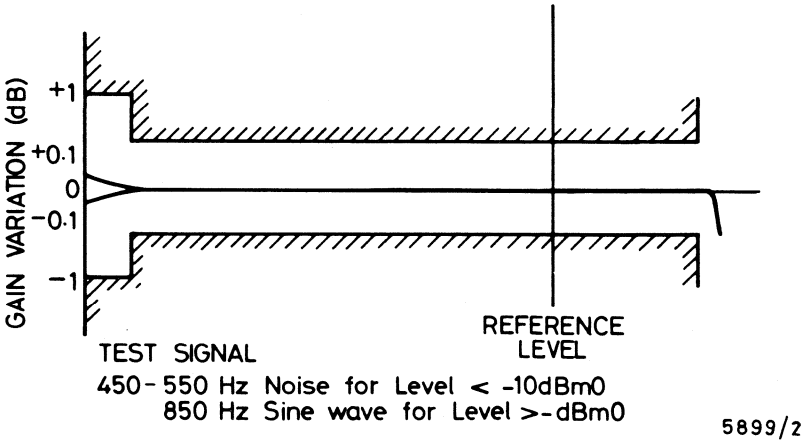
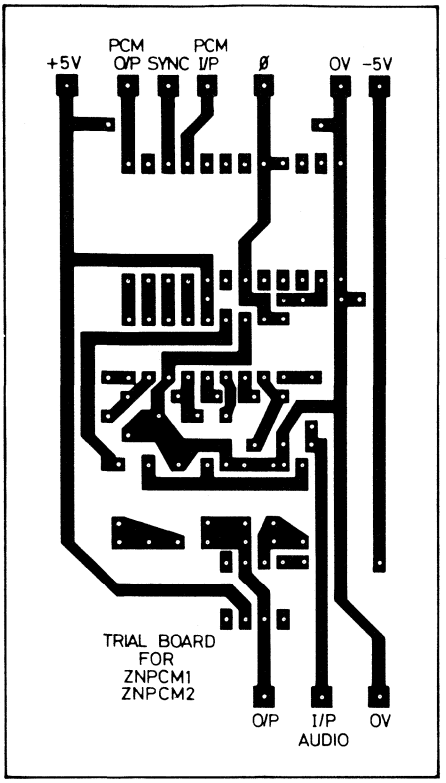


Fig. 2(b). Gain to Signal Level 'A Law'

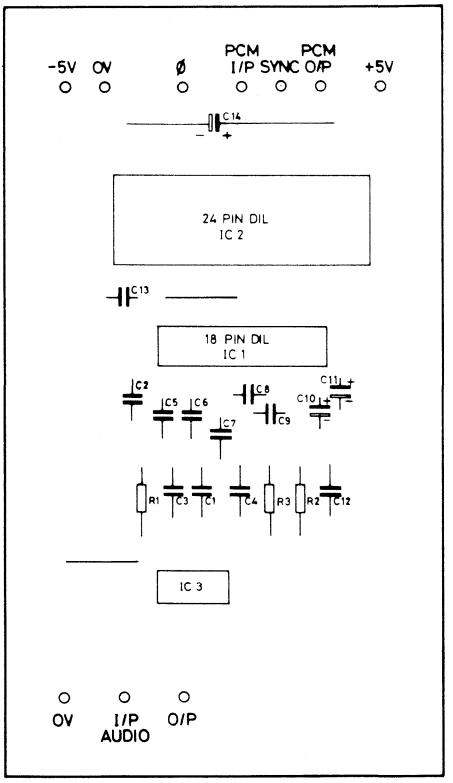
ZNPCM2

BASIC SYSTEM BOARD FOR ANALOGUE TO ANALOGUE PERFORMANCE EVALUATION



6410

P.C. BOARD



6411/2

COMPONENT LAYOUT

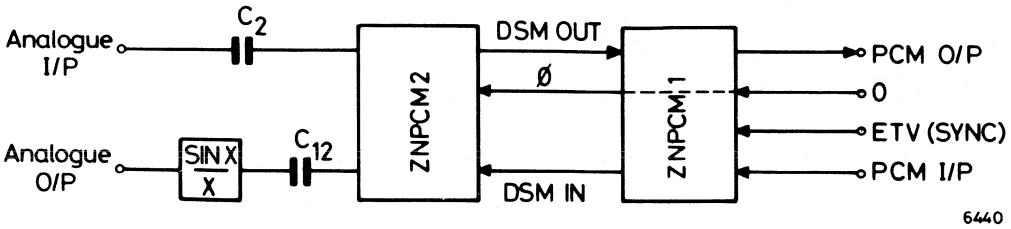
ACTUAL SIZE

ZNPCM1 & ZNPCM2 TRIAL UNIT

Component List (Tolerances ±20% unless otherwise shown)

IC1	ZNPCM2	C6	47pF ±5%
IC2	ZNPCM1	C7	4.7nF ±5%
IC3	741 or Amp	C8	0.22μF
R1	91k0 2%	C9	0.22μF
R2	91k0 2%	C10	10μF, 16V Tantalum Electrolytic
R3	100k0	C11	10μF, 16V Tantalum Electrolytic
C1	0.022μF	C12	47nF
C2	47nF	C13	0.1μF Ceramic
C3	100pF ±2%	C14	6.8μF, 10V Electrolytic
C4	1nF ±2%		
C5	10pF		

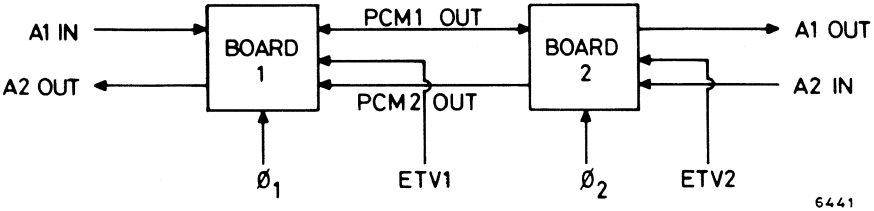
SCHEMATIC



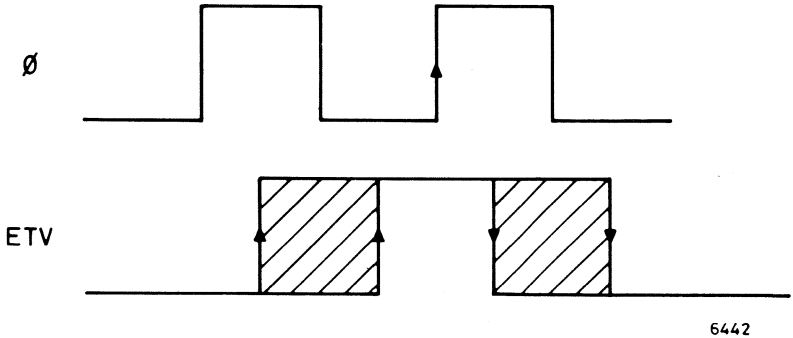
Single Channel Codec System Operating in Internal Mode (PCM at 64K bits/sec. without ADI).

Performance of the ZNPCM1/2 may be simply evaluated by linking PCM O/P to PCM I/P and comparing Analogue O/P to Analogue I/P. No ETV (Sync) signal is required for this.

For a more comprehensive evaluation two boards are required connected on the configuration shown,



$\varnothing_1$ and $\varnothing_2$ must be the same frequency and ETV1 and ETV2 can be common or up to 30 clock periods displaced.



WAVEFORMS SHOWING ETV TOLERANCE

ZNPCM2

PINNING CONFIGURATION

Pin 1 Analogue Input
Pin 2 Integrator Input
Pin 3 Integrator Output
Pin 4 Integrator Feedback Decouple
Pin 5 High-level Reference Voltage Decouple
Pin 6 Low-level Reference Voltage Decouple
Pin 7 Analogue 0V
Pin 8 Centre-level Reference Voltage Decouple
Pin 9 D.C. Feedback Decouple
Pin 10 SRF Input
Pin 11 DSM Output
Pin 12 Sign Bit Input
Pin 13 DSM Input
Pin 14 V_{CC}
Pin 15 Unfiltered Analogue Output
Pin 16 Digital 0V
Pin 17 Decoder Clock
Pin 18 Encoder Clock

5. Quality Assurance Program

Contents

5. QUALITY ASSURANCE PROGRAMME

The quality control procedures at Ferranti Electronics Limited are based on British Standard 9000, the relevant documents being:

BS 9002: Qualified products list for electronic components of assessed quality (including list of approved firms).

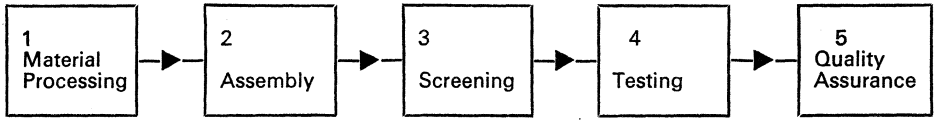
BS 9400: Integrated electronic circuits and micro-assemblies of assessed quality.

BS 9450: Custom-built integrated circuits of assessed quality.

BS 6001: Sampling procedures and tables for inspection by attributes.

The quality emphasis at Ferranti is on process control (as indicated by the use of many monitors and audits) in addition to gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting solely to screen for it.

There are five basic stages in the manufacture of Ferranti data converters, as shown below:



Each of these stages has associated with it a number of quality control checks to ensure that components will meet the standards required by the most stringent environments encountered in the field of electronics.

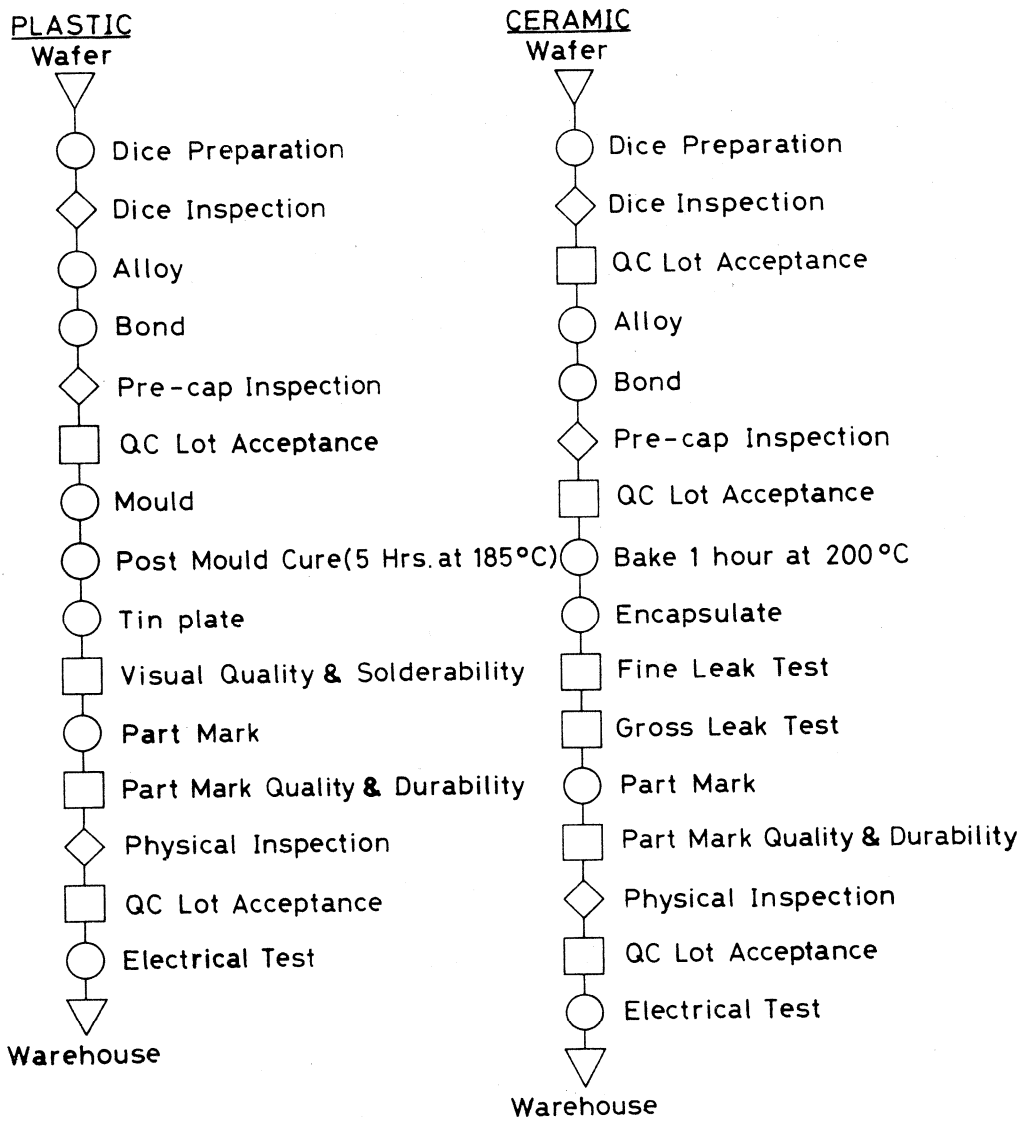
5.1 Processing

The technology used to fabricate the Ferranti range of data converters is a five mask bipolar process (see publication ref. ESA 480673). This process is used to manufacture the whole range of Ferranti LSI products, but is especially suited to converter products since it allows analogue and digital circuits to be fabricated on the same chip, with good yields and high packing densities. The process has full BS 9450 capability approval and is the first bipolar process in the U.K. to receive such approval.

5.2 Assembly

Ferranti data converters are available in either moulded or hermetically sealed ceramic dual in-line (DIL) packages (though certain types are available only in ceramic package). The assembly flow-charts for both types of package are shown in Table 1. All products are manufactured by the same routes and using the same techniques as BS 9000 approved products.

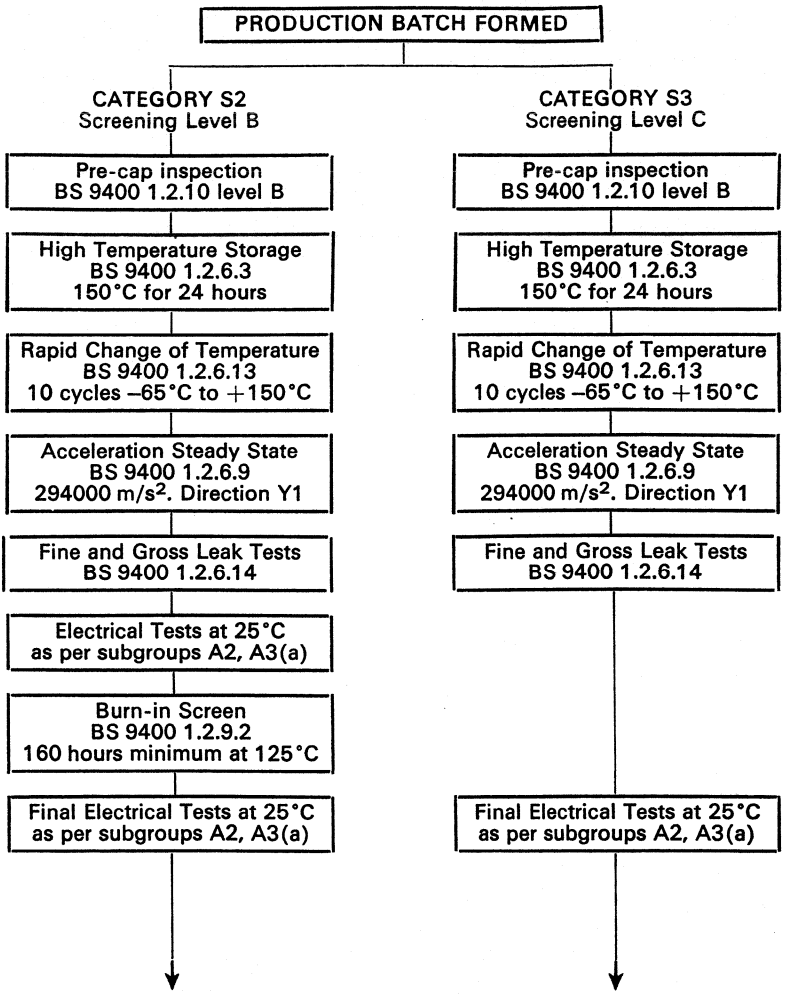
Q A Programme



6083

Q A Programme

TABLE 2



5.3 Screening

In addition to the standard manufacturing cycle, optional screening procedures are available to produce high-reliability products. A full breakdown of the options available, related to their BS 9400 procedures, is shown in Table 2.

5.4 Testing

On completion of assembly all devices are subjected to 100% functional and d.c. testing in addition to either an S4, 2.5% sample or 100% check on a.c. characteristics depending on device type. The d.c. tests are inset to tighter limits than those shown on the data sheet in order to ensure that the device will function within the specified conditions over its full operating temperature range.

In addition to the 100% test already described, devices manufactured to commercial specifications also undergo sample tests to the AQLs in Table 3, including the temperature extreme tests mentioned above.

TABLE 3

Inspected Parameter	Inspection Level	AQL
Visual & Mechanical including major external workmanship and marking permanency	I	1%
Function	II	0.15%
Major Electrical Parameters at $T_{amb} = 25°C$	II	0.65%
Major Electrical Parameters over operating temperature range	II	2.5%

5.5 Quality Assurance

Despite all the measures taken to ensure that commercial product is of a high standard it is inevitable that certain market sectors will require a higher level of quality assurance. These market sectors are predominantly military and telecommunications orientated.

Wherever devices are supplied to these more stringent QA requirements they are re-routed at the end of the assembly cycle through our QA Bond Department. They are subjected, on a lot-by-lot basis, to a more rigorous examination of ther quality using methods laid down in BS 9000 or its equivalent for the specification concerned.

In addition to lot-by-lot testing, long term life testing of product is performed continually. This enables constant monitoring of process stability and any undesirable deviations from the norm are quickly brought to light so that corrective measures may be implemented.

Q A Programme

5.6 Acceptable Quality Levels

As explained earlier the procedures and manufacturing techniques used by Ferranti are consistent with producing an inherently reliable product rather than screening out unreliable product. This is achieved by careful process control combined with numerous gate inspections.

In order for such a system to be effective it is necessary to implement a sampling procedure where the sample size and inspection levels of the various stages are adequate to assure satisfactory quality of the end product whilst remaining cost effective. This can be achieved only after a long history of semiconductor manufacture, which gives an intimate knowledge of the problems likely to arise at each stage of manufacture, and the best methods of inspecting for them.

The sampling procedures used by Ferranti are those outlined in BS 6001. The Acceptable Quality Level (AQL) is the maximum percentage of defective devices that can, for the purposes of inspection, be considered satisfactory as a process average.

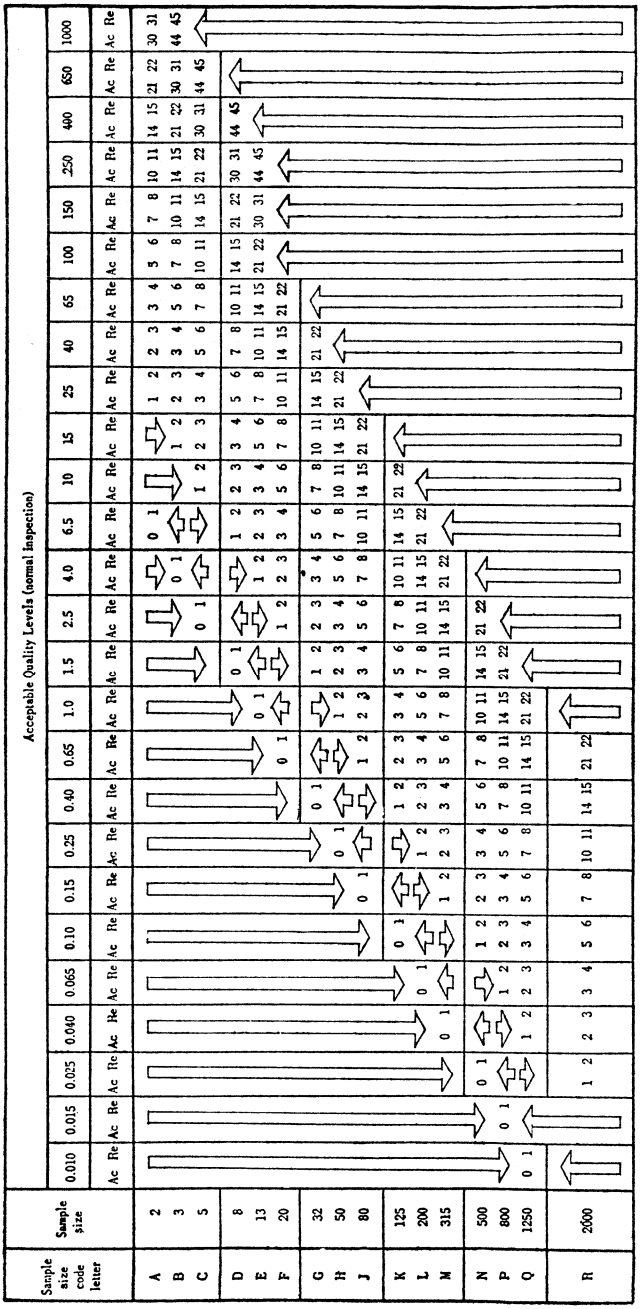
The AQL sample size codes and sampling plan used by Ferranti are reproduced in tables 4 and 5.

TABLE 4

SAMPLE SIZE CODE LETTERS

Lot or batch size			Special inspection levels				General inspection levels		
			S-1	S-2	S-3	S-4	I	II	III
2	to	8	A	A	A	A	A	A	B
9	to	15	A	A	A	A	A	B	C
16	to	25	A	A	B	B	B	C	D
26	to	50	A	B	B	C	C	D	E
51	to	90	B	B	C	C	C	E	F
91	to	150	B	B	C	D	D	F	G
151	to	280	B	C	D	E	E	G	H
281	to	500	B	C	D	E	F	H	J
501	to	1200	C	C	E	F	G	J	K
1201	to	3200	C	D	E	G	H	K	L
3201	to	10000	C	D	F	G	J	L	M
10001	to	35000	C	D	F	H	K	M	N
35001	to	150000	D	E	G	J	L	N	P
150001	to	500000	D	E	G	J	M	P	Q
500001	and	over	D	E	H	K	N	Q	R

Q A Programme – TABLE 4



6. Package Details

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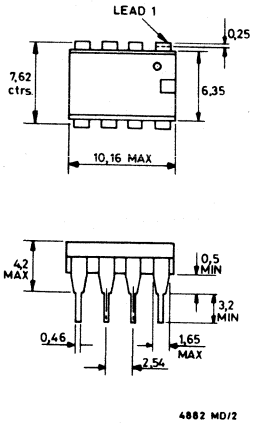
6. Package Details



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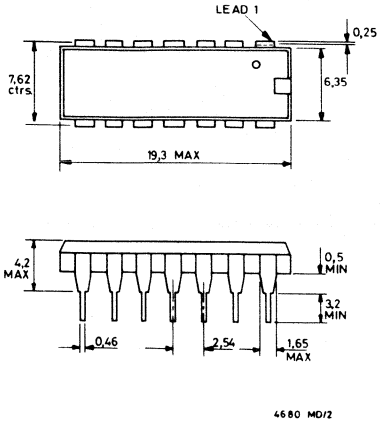

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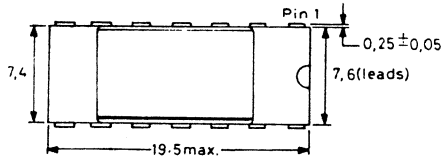
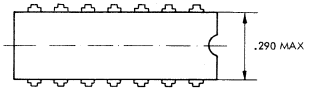
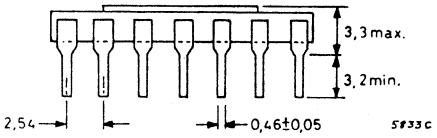
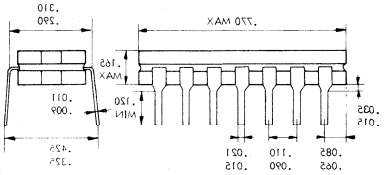






14 LEAD CERAMIC DIL
(SIDE-BRAZED)



14 LEAD CERAMIC DIL
(CERDIP)

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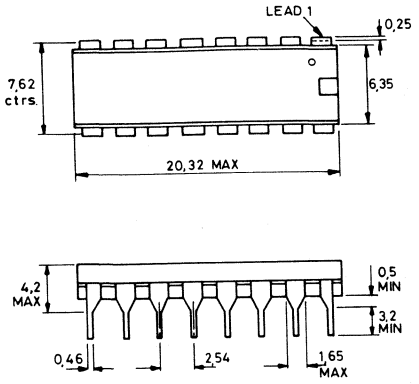

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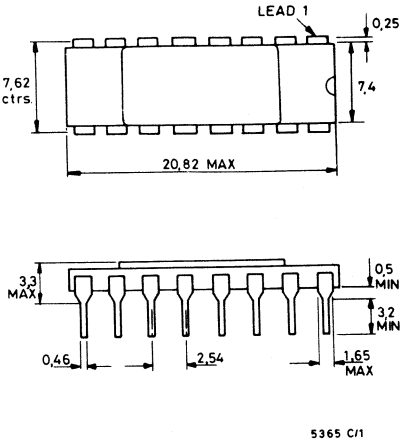

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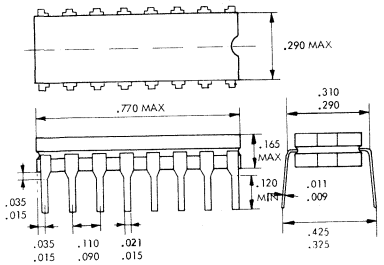

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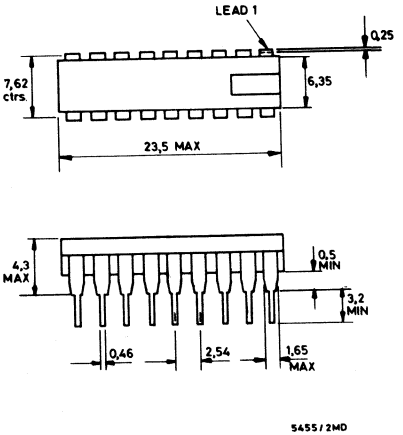

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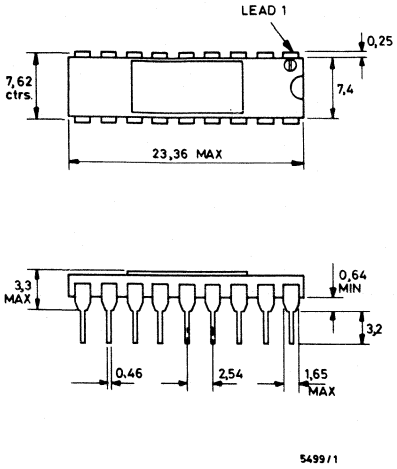

18 LEAD CERAMIC DIL
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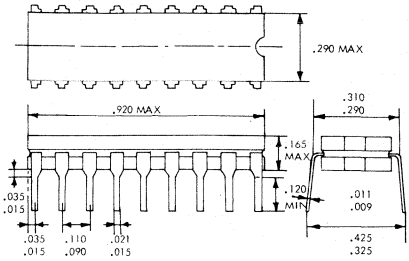

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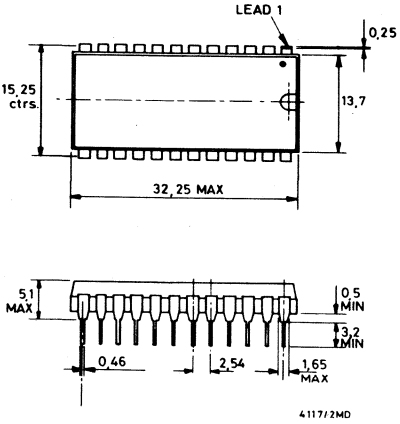
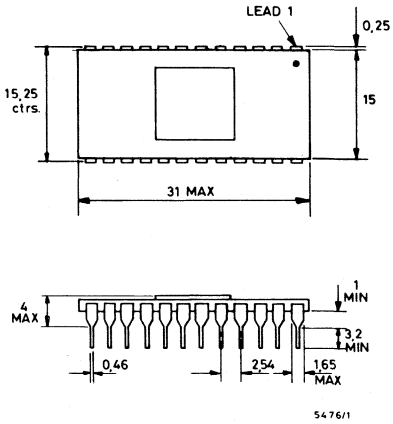


24 LEAD MOULDED DIL



24 LEAD CERAMIC DIL

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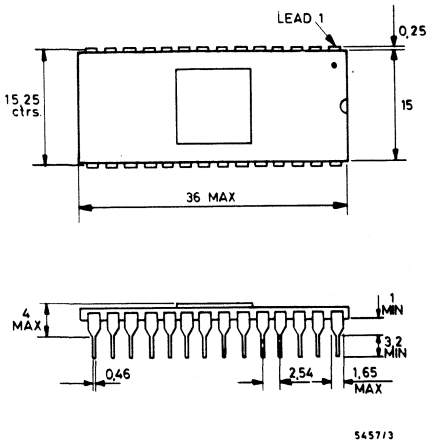

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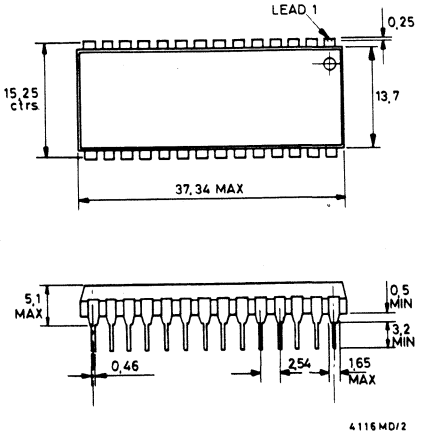

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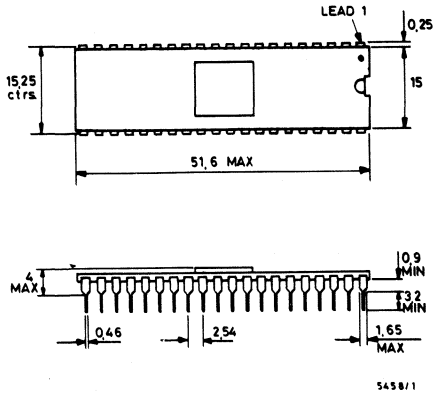

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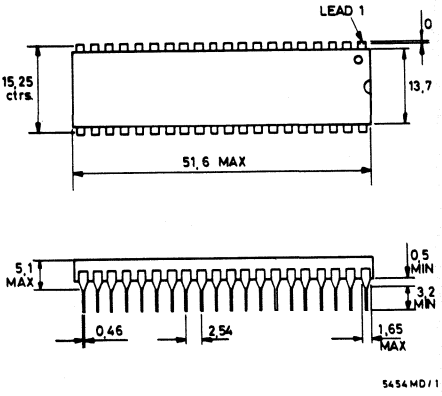
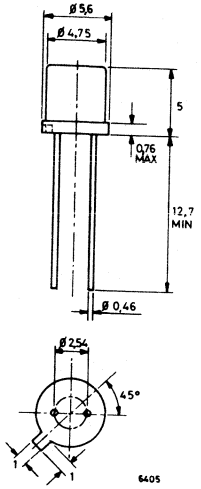
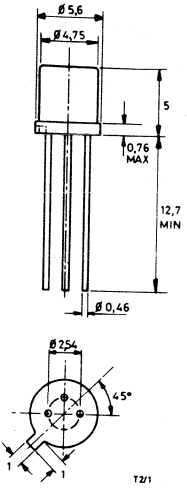


40 LEAD MOULDED DIL

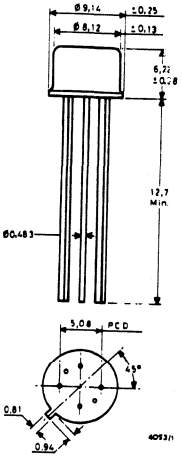
Package Details



TO-18 (2 Lead)



TO-18



TO-39 (6 Lead)

7. Application Notes

Contents

Applications of the ZN425 8 bit A-D/D-A Converter

CONTENTS

1. INTRODUCTION

Digital to analogue, (D-A), and analogue to digital, (A-D), conversion is a specialised field of electronics. It is useful to consider first the general principles of such conversion techniques, and definitions commonly used in the general field of A-D and D-A conversion.

The discussion is limited to 8-bit converters of a type similar to the ZN425E, illustrated in Figure 1a.

Digital information, fed in to the converter, normally as parallel bits, generates an analogue output corresponding to the value of the binary coded number entered at the input. Ignoring errors for the moment, and assuming that the analogue output is a voltage, the output can be expressed as:

$$V_{out} = V_{full\ scale} \times \frac{\text{Binary Input}}{\text{Full scale binary input}}$$

which, in the case of the ZN425E, is

$$V_{out} = V_{REF} \times \frac{\text{Binary Input}}{256}$$

The voltage output is obtained using a resistive ladder network shown in Figure 1b. Switches connect resistors within the network either to the reference voltage or to the ground line according to the state of the binary inputs controlling each particular switch.

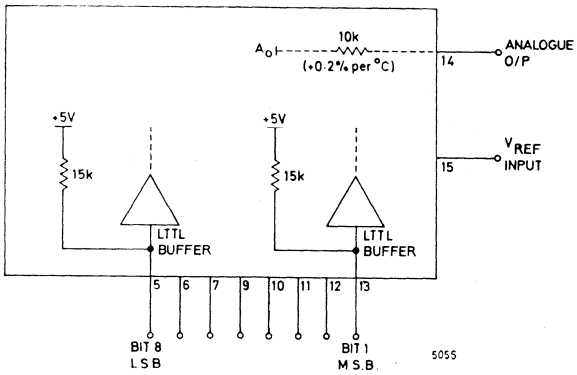


Fig. 1a Basic 8 bit D to A converter

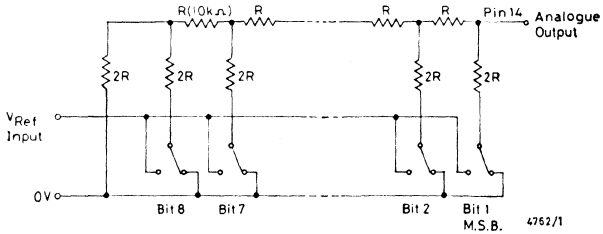


Fig. 1b The R-2R ladder network

The block diagram of the ZN425E circuit is reproduced in Figure 2.

The integrated circuit is fully monolithic, It contains a resistive ladder network, a logic input select switch, voltage switches, an internal reference and a counter. The D-A reference may be connected to the internally generated reference or to an external reference voltage. The inclusion of a counter within the circuit considerably extends its application. A 'staircase' waveform can be very simply generated at the analogue output by feeding a train of clock pulses into the counter.

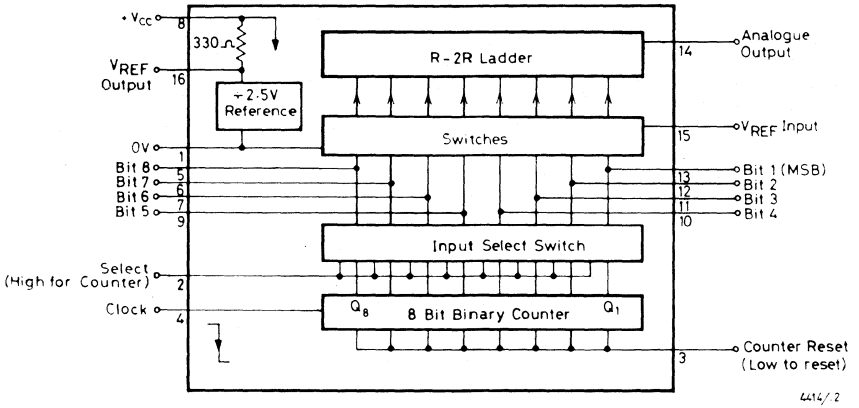


Fig. 2 Block diagram of ZN425E

The ZN425E system operation is outlined in Figure 3. The counter may be clocked by negative going inputs and reset by applying a '0' level to the reset pin.

The digital inputs to the converter may be obtained either from an external source when the 'logic select' pin is at logical '0' ,or from the counter when it is set to logical '1'. In the latter case the state of the counter appears at the digital input terminals as '0' or '1' levels on open collectors with 15 kΩ pull up resistors. In the D-A mode the digital input terminals may be considered as low power TTL inputs.

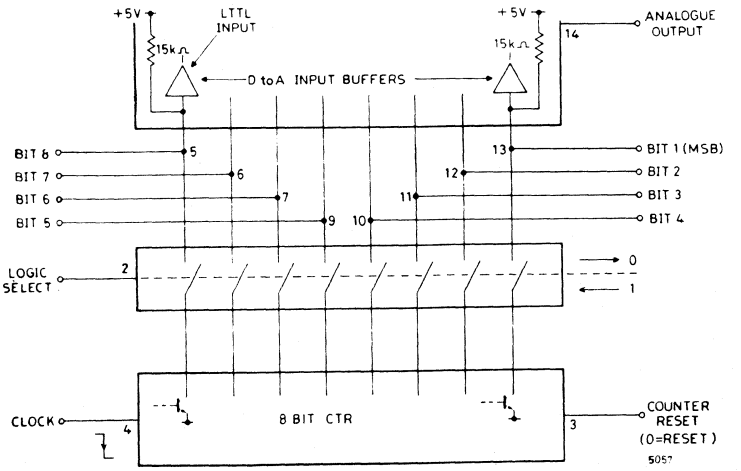


Fig. 3 Outline ZN425E operation

1.1 Definitions

Various terms commonly used when discussing D-A and A-D converter operation are defined below.

Resolution

The resolution is determined by the number of digital inputs, i.e. an 8 bit DAC, (digital to analogue converter), is said to have 8 bit resolution. No particular level of accuracy is implied.

Staircase/Ramp

As the binary code is increased step by step, the analogue output also increases in discrete steps. If the input code increases at a constant rate the resulting output will be a staircase

Since the number of discrete steps is normally large, e.g. 255 for 8 bits, the staircase is frequently termed a ramp, though this is not strictly accurate.

Monotonicity

A DAC is said to be monotonic if an increase in the applied binary coded digital number always produces an increase in the analogue output. Waveforms produced by a D-A 'staircase' generator illustrated in Figure 4a shows the effect of non monotonicity.

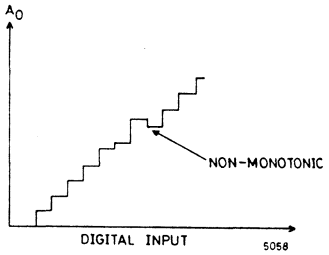


Fig. 4a Non-monotonicity

Ideal DAC Output

The ideal DAC output of a staircase generator is shown in Figure 4b.

The output is defined as a set of points on a straight line between zero and full scale. For an ideal 8-bit DAC:

$$V_{out} = \frac{n}{2^8 - 1} \times V_{FS}$$

$$= \frac{n}{255} \times V_{FS}$$

and $$V_{FS} = \frac{255}{256} \times V_{REFinput}$$

$\therefore$ $$V_{out} = \frac{n}{256} \times V_{REFinput}$$

where 'n' is the number represented by the digital input.

For example $$01101100 = 2^6 + 2^5 + 2^3 + 2^2$$

$$= 108$$

gives an output $$V_{out} = \frac{108}{256} \times V_{FS}$$

$$= \frac{108}{256} \times V_{REFinput}$$

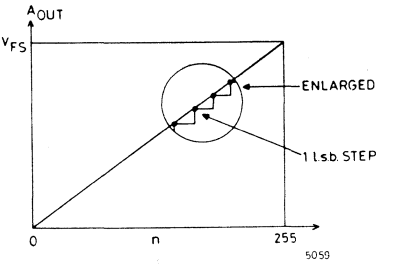


Fig. 4b Ideal DAC output

Linearity Error

A DAC may deviate from the ideal as shown in Figure 4c. The error is usually specified as a maximum deviation of the analogue output, from the ideal output, as a fraction of the 'Least Significant Bit'. The ZN425E has a linearity better than $\pm\frac{1}{2}$LSB, and

$$\tfrac{1}{2}\,\text{LSB} = \tfrac{1}{2} \times \frac{V_{FS}}{255}$$

Relative Accuracy

The error expressed as a percentage of the full scale voltage, V_{FS}, is termed the relative accuracy.

The ZN425E, an 8-bit converter with $\pm\frac{1}{2}$ LSB linearity, has a relative accuracy of $\frac{1}{510} \times 100\%$, i.e. approximately 0.2% accuracy.

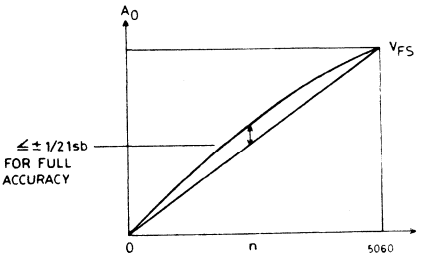


Fig. 4c Error definition

2. D-A and A-D CONVERTER SYSTEMS

2.1 8 bit D-A and Calibration Procedure

The ZN425E gives an analogue voltage output directly from pin 14, so that the usual current to voltage converting amplifier is not required. However, in order to buffer the resistive ladder output impedance, to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Figures 5a and 5b show a typical scheme with either the ZN424P or ZLD741CP as the buffer amplifier. The internal voltage reference source (V_{REFout}) is used, and to minimise temperature drift the source resistance to the inverting input of the buffer amplifier should be approximately 6 kΩ. Calibration procedure is as follows:

(i) Set all bits to LOW and adjust R2 until $V_{out} = 0.000V$

(ii) Set all bits to HIGH and adjust R1 until V_{out} = nominal full scale reading – LSB.

(iii) Repeat (i) and (ii).

e.g. Set F.S.R. to +3.840V – 1 LSB = 3.825V.

$$(1\ LSB = \frac{3.84}{256} = 15\ mV)$$

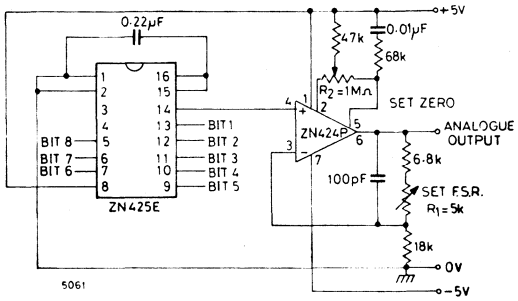


Fig. 5a 8 bit DAC using ZN424P

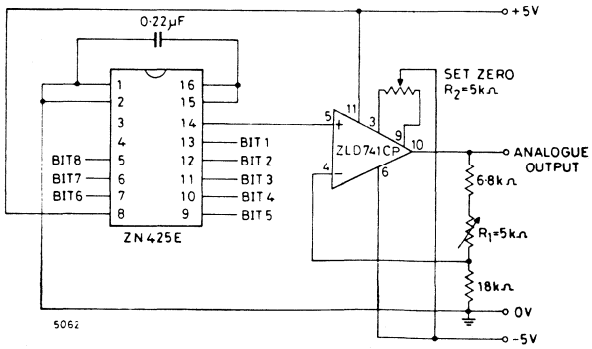


Fig. 5b 8 bit DAC using ZLD741CP

2.2 8 bit A-D and Calibration Procedure

Figure 6 shows the ZN425E in a counter type ADC which comprises a comparator and a latch and requires an external clock. Upon application of a convert command pulse (15 μs minimum) the counter is set to zero and at the same time the state of the latch is altered.

The gate is opened, enabling clock pulses to be fed to the counter input (Pin 4) of the ZN425E. The analogue output of the ZN425E begins to ramp up until its amplitude equals that of the analogue voltage at the non-inverting input of the comparator. At this point the comparator changes state, altering the latch to its initial resting state, thus inhibiting further clock pulses. Hence the digital number stored in the respective bits of the ZN425E is a true representation of the analogue input voltage. The diode is included so that when the comparator changes state, its output is effectively clamped at zero (LOW).

Operating clock frequencies can be as high as 400 kHz. Improved results may be obtained by using narrow clock pulses to avoid the trailing edge affecting ramp settling. At frequencies above 100 kHz a faster comparator than the ZN424 should be used for optimum linearity around zero.

The conversion time is dependent upon the analogue input and for full scale reading (F.S.R.) is given by the clock period multiplied by the number of counts.

$$\text{If } F_{Clock} = 256 \text{ kHz},$$

$$T_{Convert} = \frac{2^8}{256 \times 10^3} \text{ seconds} = 1 \text{ ms}$$

The calibration procedure is as follows:

(i) Apply continuous CONVERT COMMAND PULSES

(ii) Apply full scale minus $1\frac{1}{2}$ LSB to analogue input and adjust F.S.R. pot until the converter LSB just switches between 0 and 1 with all other bits at 1.

(iii) Apply zero $+\frac{1}{2}$ LSB to analogue input and adjust zero pot until the converter LSB just switches between 0 and 1 with all other bits 0.

(iv) Repeat step (ii)

E.g. Full scale = 4 volts.

$$1 \text{ LSB} = \frac{\text{Full Scale}}{256} = \frac{4 \text{ volts}}{256} = 15.63 \text{ mV}$$

Input for zero setting = $\frac{1}{2}$ LSB = 7.82 mV

Input for full scale setting = 4V − $1\frac{1}{2}$ LSB = 3.97656 volts.

After conversion is complete the analogue input is available from the ZN425E in digital and analogue form and therefore the ADC may be used as a sample and hold with infinite hold time. The convert command is replaced by a sample command.

A peak detect circuit may also be constructed using similar techniques, and is described in section 3.4.

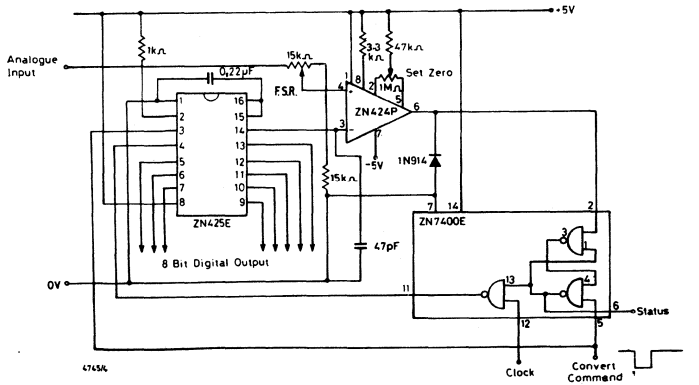


Fig. 6 8 bit Analogue to Digital Converter

2.3 Bipolar Operation

Previous circuits described have entailed the use of a uni-polar buffer amplifier (using ZN424E and ZLD741CP) following a DAC as a means of removing the offset voltage, minimising temperature drift and calibrating the DAC. A natural sequel to this is the derivation of a bi-polar buffer amplifier which fulfils these conditions. This entails buffering the output of a DAC such that the amplified output from the buffer is symmetrical about zero. To effect this, the conditions that have to be satisfied are:

(i) When the DAC output $= \frac{V_{REF}}{2}$ (digital input $=$ 10000000) then the buffer amplifier output $=$ zero.

(ii) Gain can be easily selected and suitable resistor values calculated. Actual gain and offset must be capable of fine adjustment.

The circuit of Figure 7a was first devised as a possible solution.

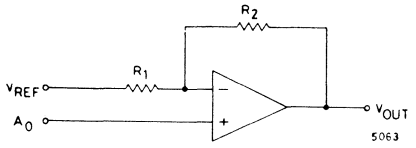


Fig. 7a Bi-polar operation, starting point

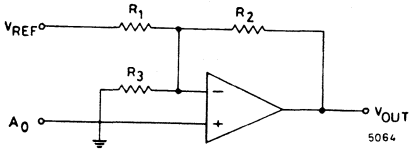


Fig. 7b Bi-polar operation, concept progression

If F_N = non-inverting feedback return $= \frac{R1}{R1 + R2}$ and F_I = inverting feedback return $= \frac{R1}{R2}$

Then V_{out} is given by:

$$V_{out} = \frac{A_O}{F_N} - \frac{V_{REF}}{F_I} = A_O\left(\frac{R1 + R2}{R1}\right) - V_{REF}\frac{R2}{R1} \quad \text{. . . equation 1}$$

If $A_O = \frac{V_{REF}}{2}$ and R1 $=$ R2 then $V_{out} = 0$ satisfying condition (i).

However Gain $\left(\text{defined as } \frac{V_{out}}{A_O}\right) = \frac{R1 + R2}{R1} = 2$ and condition (ii) would not be satisfied since adjusting R1 or R2 would upset the gain on offset. To minimise these disadvantages therefore the circuit of Fig. 7b was devised using an additional resistance, with its Thevenin equivalent of Fig. 7c. Using equation 1 then an expression for the output voltage V_{out} can be shown as:

$$V_{out} = A_O\left[1 + \frac{R2\,(R1 + R3)}{R1\,R3}\right] - V_{REF}\frac{R2}{R1}$$

For $A_O = \frac{V_{REF}}{2}$ (Condition (i)) then $V_{out} = 0$

and $R1 = \frac{R2\,R3}{(R2 + R3)}$ i.e. R1 $=$ parallel combination of R2 and R3.

Substituting this expression for R1

then Gain $G = \left[1 + \left(\frac{2R2 + R3}{R3}\right)\right] = \left[2 + \frac{2R2}{R3}\right]$

If we let say R2 $= \lambda$R3 then $G = 2\,(1 + \lambda)$ and $\lambda = \left(\frac{G - 2}{2}\right)$

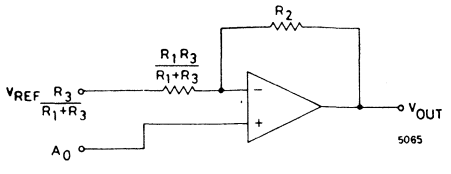


Fig. 7c Thevenin equivalent of Fig. 7b

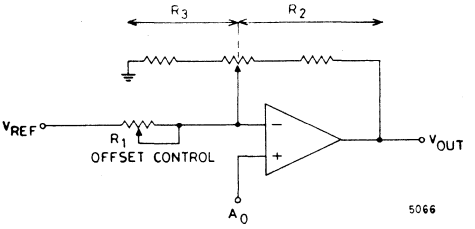


Fig. 7d Bi-polar operation, control schematic

i.e. $G \geqslant 2$ from which $R2 = \left(\frac{G-2}{2}\right) R3$

And $R1 = \left(\frac{R2\,R3}{R2+R3}\right) = \left(\frac{\lambda}{1+\lambda}\right) R3 = \left(\frac{G-2}{2}\right) R3$

Furthermore the buffer amplifier input impedance =

$$\frac{R1\,R2\,R3}{R1R2 + R2R3 + R1R3} = \left(\frac{G-2}{2G}\right) R3$$

All the above expressions and relationships form a basis for development of the circuit of Fig. 7d whereby by defining a certain gain (G) all resistor values can be appropriately calculated as illustrated.

e.g. Let $G = 4$, then $R_{in} = \left(\frac{4-2}{8}\right) R3 = \frac{R3}{4}$

If $R_{in} = 10\ k\Omega$ (the value required for minimum offset taking into consideration R_{out} of ZN425E DAC $\simeq 10\ k\Omega$) then $R3 = 40\ k\Omega$.

$$R2 = \left(\frac{G-2}{2}\right) R3 = \left(\frac{4-2}{2}\right) R3 = R3 = 40\ k\Omega$$

$$\text{And } R1 = \left(\frac{G-2}{G}\right) R3 = \left(\frac{4-2}{4}\right) R3 = \frac{R3}{2} = 20\ k\Omega$$

It has been shown that $R1 = \frac{R2\,R3}{R2+R3}$. The simplest approximation ensuring this relationship is by using a potentiometer as a gain control.

The finalised circuit is shown in Fig. 8.

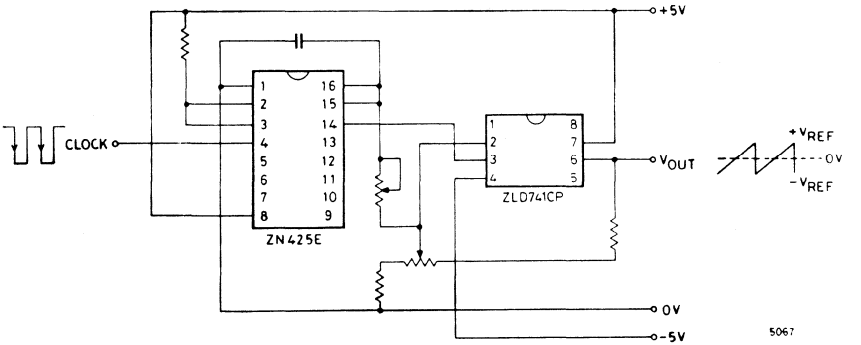


Fig. 8 Bi-polar operation, circuit diagram

2.4 Applications

Applications for the use of the ZN425E in its D-A or A-D mode are those where 8 bit accuracy suffices. This is the majority of transducer applications, particularly as system hierarchy is tending to change with the advent of microprocessors, taking the conversion near to the point of measurement. For example, in data acquisition monitoring say 100 channels, it is feasible and economic to use one D-A per channel and multiplex one A-D per 8 channels using a single microprocessor.

If one reference is required to power several converters, additional source current may be provided by an external parallel resistor from supply to reference providing 1.2 mA per additional converter in excess of three. In this case the additional earth pin current causes an offset due to a pin resistance of around 0.1 Ω

Specific applications of 8 bit A-D are in conjunction with stress or strain gauges, and many temperature applications. 8 bit D-A may be used for driving chart recorders, programmable power supplies and actuators.

3. RAMP GENERATION

The counter in the ZN425E is very convenient for feeding in a clock to generate a staircase. This facility is used in the majority of applications detailed below.

The count rate which may be used to obtain full ramp accuracy, determined by the worst case settling time of 2 μs, is 500 kHz, giving a cycling time of around $\frac{1}{2}$ ms. However, the counters are capable of being clocked at up to 5 MHz, though there will be a loss in staircase accuracy at this speed.

3.1 Continuous

This is illustrated by the circuit of Fig. 9 and is simply accomplished in the normal DAC mode by applying clock pulses to the on chip counter (Pin 4) of the ZN425E, which produces a staircase waveform, When the counter is full it returns to its empty state and counting recommences resulting in a continuous ramp.

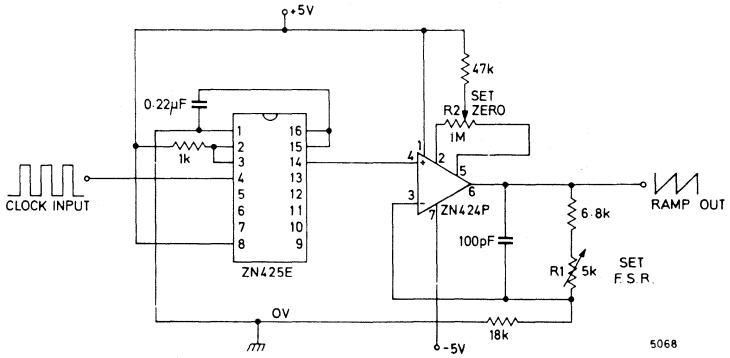


Fig. 9 Precision ramp generator

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary as previously described for the DAC.

The ramp period for 8 bits will be equal to 256 times the clock period, and the maximum amplitude of the ramp from the ZN425E using the internal reference voltage will be $V_{REFout} - 1$ LSB. Therefore, the peak ramp amplitude from the buffer will be this value times the amplifier gain, which, with gain adjustment potentiometer set halfway

$$2.5V \times \frac{3}{2} = 3.75V.$$

A duty cycle drive signal is sometimes required from an input voltage generated by a potentiometer, for example, for actuator drives, or general power control. This may be provided as shown in Fig. 10, where the ZN425E provides a continuous ramp, against which the voltage reference is compared using a ZN424P. The output from the comparator then provides the duty cycle signal directly.

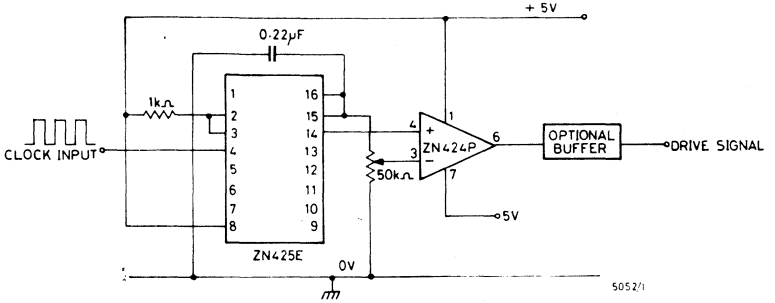


Fig. 10 Duty cycle drive signal

3.2 One Shot

A single one shot ramp can be generated quite simply (Figs 11a and 11b) by using a latch and two capacitors to control the counter reset of a ZN425E DAC. Operation is as follows:

The stationary states of the latch are shown, these being initially determined by the charging times of capacitors C1 and C2 which ensures the counter reset of the ZN425E (Pin 3) is LOW. Upon operating the START button the states of the latch are altered and a HIGH is fed to the counter reset enabling counting of the input clock pulses to commence. The analogue output begins to ramp up until the counter is full at which point the MSB goes LOW altering the latch to its initial resting states. This resets the counter and terminates the ramp. It should be noted that even if the start button is held down at the commencement of the operation, only a one shot ramp results, and not a periodic function.

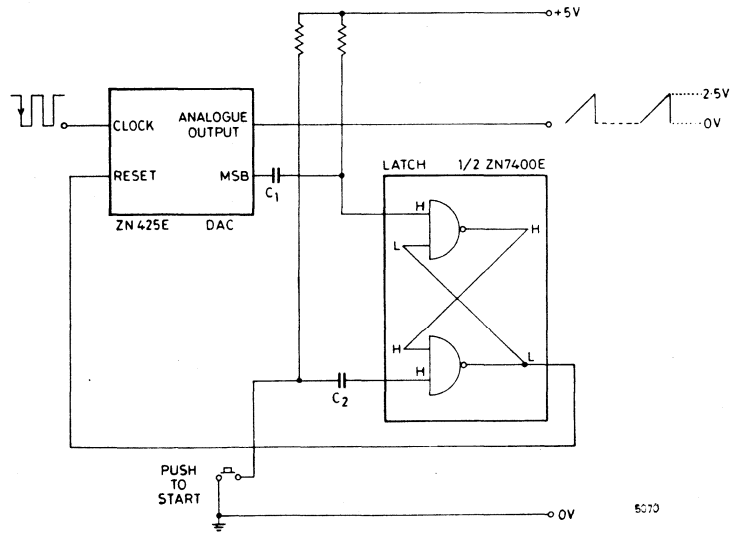


Fig. 11a One shot schematic

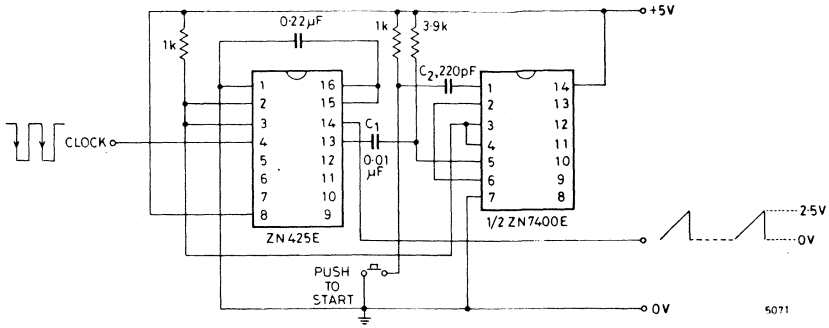


Fig. 11b One shot circuit

A more sophisticated alternative method performing the same function, which replaces capacitors by logic, is outlined in Figs. 11c and 11d. Stationary states of the various logic elements are as indicated. The initial state of the flip-flop is determined by the relative states of the PRESET and CLEAR inputs. Upon switching on the supply the PRESET is held LOW with respect to CLEAR because of the charging time associated with C1 and R1. This results in Q = HIGH, $\overline{Q}$ = LOW, therefore, the counter reset on the ZN425E is LOW.

When the start button is pressed, a pulse from the monostable clears the flip-flop, the counter reset goes HIGH enabling the counting of the input clock pulses to commence. The ZN425E analogue output begins to ramp up until the counter is full, at which point the MSB goes LOW. This is fed to the CLOCK input of the flip-flop which then TOGGLES, reverting to its original state, thereby resetting the counter and terminating the ramp. As with the previous circuit only a one shot ramp will be generated even if the start button is held down.

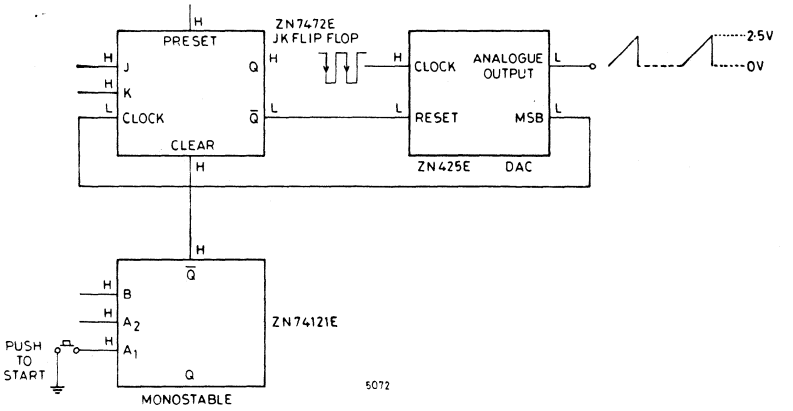


Fig. 11c Alternative one shot schematic

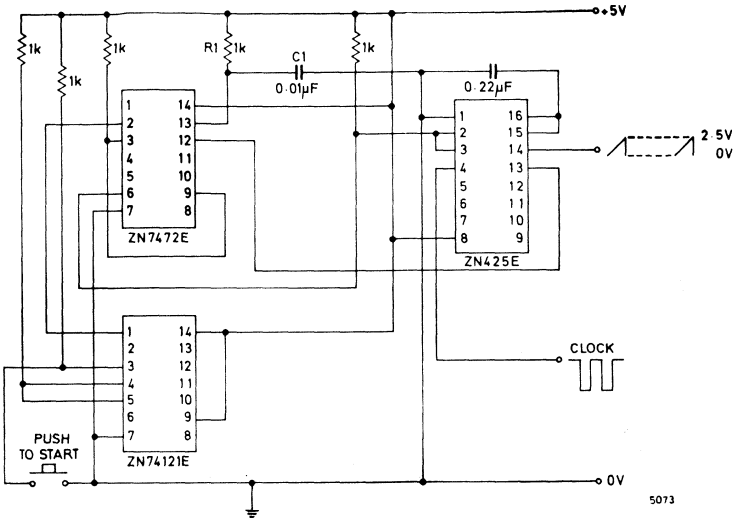


Fig. 11d Alternative one shot circuit

3.3 Weighing System and Auto Zero

The system to be described is intended for either static or on-vehicle load indicating applications and employs integrated circuits from the Ferranti Standard Product range. Variations of the scheme are indicated which increase its range of application. The overall system is shown in the circuit diagrams of Figures 12a to 12e.

The basic measuring function is a $3\frac{1}{2}$ digit DVM using the dual slope analogue to digital converter principle. This displays an analogue input of up to ± 1999 millivolts which is scaled as required. All the DVM digital and control functions are carried out by one C.D.I. integrated circuit from the U.L.A. (Uncommitted Logic Array) range, type ZNA116E.

The DVM input is driven from a separate unity gain summing amplifier which accepts inputs from any number of channels each consisting of transducer and pre-amplifier.

Included in the system is a push button auto-zeroing circuit which automatically sets the output of the summing amplifier to zero. This facility eliminates any small zero errors which may have accumulated in the transducer and pre-amplifier chain or any false zero readings which can appear when on-vehicle systems are operated on uneven ground. For this function the ZN425E 8 bit digital to analogue converter is used. This monolithic integrated circuit also includes an 8 bit binary up-counter and a reference voltage generator and by clocking the counter a voltage ramp of 256 discrete steps is generated. This ramp is level shifted to become symmetrically bipolar with respect to 0V and then applied to the virtual earth of the summing amplifier. This forces the amplifier output through 0V and a comparator circuit detects the 0V condition and inhibits the clock pulses to the counter. The selected ramp output level is therefore held indefinitely unless the auto-zero is switched off when the system reverts to the original zero conditions.

Additional facilities include B.C.D. outputs for data logging purposes and an overload alarm system with warning indication.

The alarm system uses two comparators into which are set two analogue levels, one corresponding to a preset percentage of full load and the other to full load. When the load reaches the first level a 1 Hz square wave output is available and a separate output gives a continuous signal at the second level. These outputs may be wire ORed or used separately to drive visual or audible alarms.

It is not essential for the DVM function to be fully bi-polar in this application because negative readings occur only as small zero errors. A minor modification enables the circuit to display lower accuracy negative readings at the same time eliminating one of the ZN423 reference generators.

Further modification, appropriate for some applications, results in a 3 digit display with a 1 Hz flashing leading zero to indicate a small negative zero error.

This approach, using a mix of standard function integrated circuits gives maximum system flexibility. For example, an on-vehicle application may require separate auto-zero functions on a number of axles or an overload alarm indication may require duplication. By adding the appropriate integrated circuits the system can be tailored to suit a range of vehicle requirements with a minimum of chip function redundancy and therefore minimum cost.

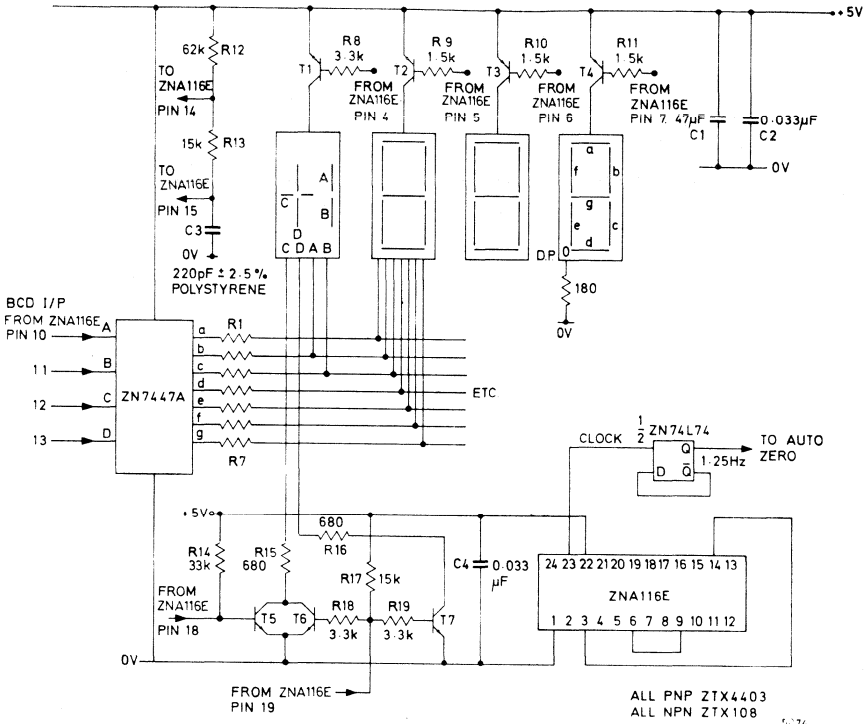


Fig. 12a Display/digital circuit

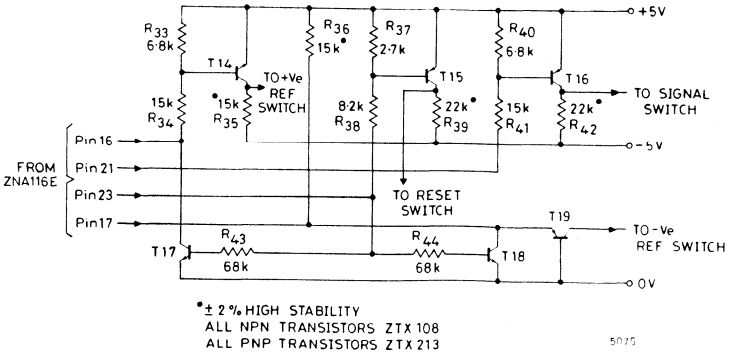


Fig. 12b Analogue switch

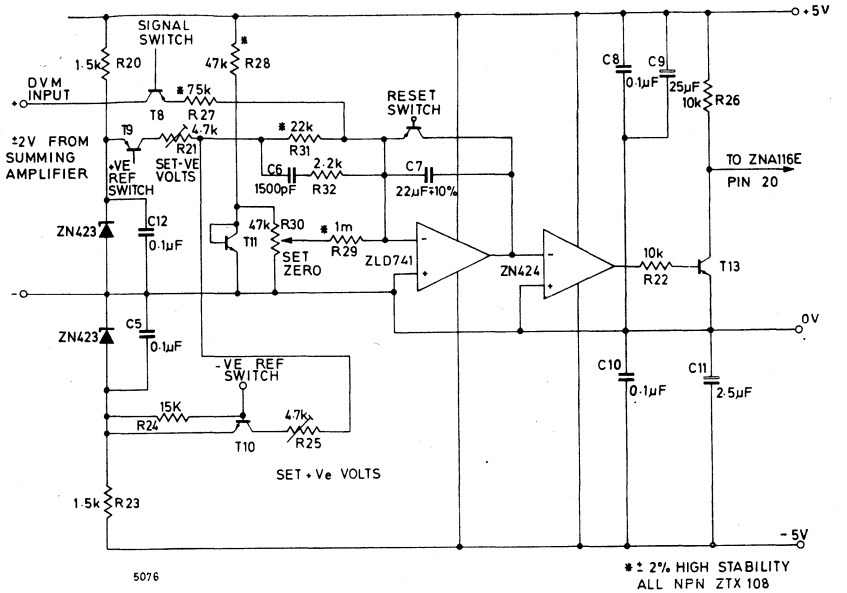


Fig. 12c Dual slope integration circuit

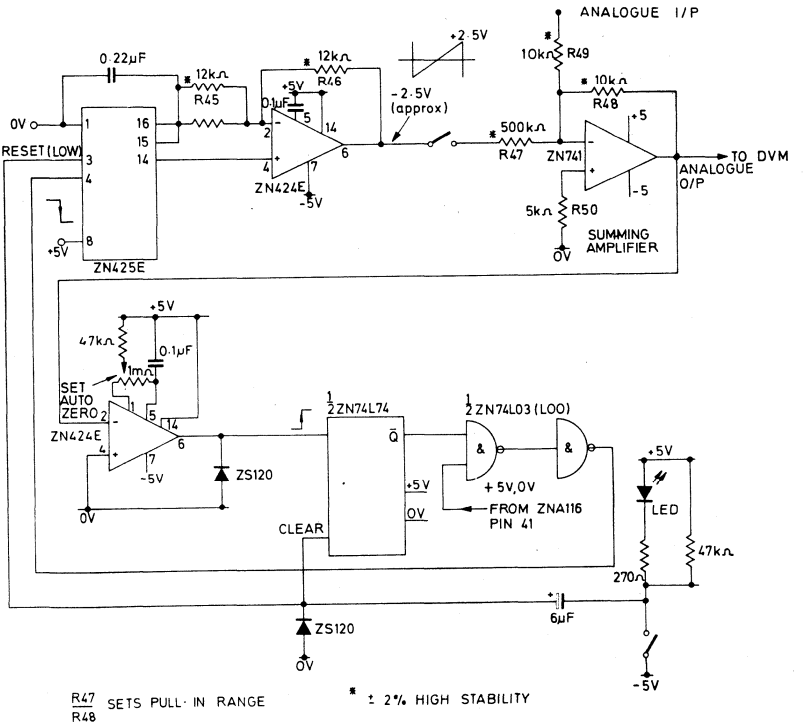


Fig. 12d Auto zero circuit

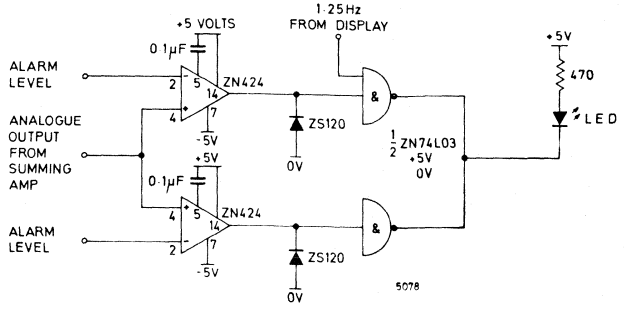


Fig. 12e Alarm circuit

3.4 Peak Detect

A peak detect circuit may be constructed simply using the form of A to D system shown in the schematic of Fig. 13. When left running continuously it will hold the maximum input signal level it is able to track, i.e. peak detect.

After application of a reset pulse, the state of the comparator enables clock pulses from the Schmitt trigger circuit to be fed to the counter of the ZN425E. The analogue output begins to ramp up until it attains the level of the analogue input voltage at which point the comparator changes state and inhibits further clock pulses. Therefore, the analogue output is held and stored digitally in the bits of the converter. It will continue to hold this level until a further increase in analogue input voltage changes the comparator state, enabling the clock, and the sequence is repeated.

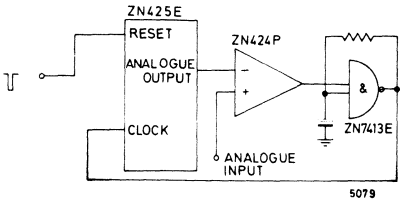


Fig. 13 Peak detect schematic

3.5 Channel Selector

Another interesting application of the A-D principle is for a channel selector in communications, e.g. citizens or amateur band. In effect it replaces a multiway switch, mechanically limited to 24 or 30 channels, by a 10 turn potentiometer which can be used with the system of Fig. 14 to generate many more discrete steps, typically 64 but up to 256.

The ZN425E, with internal counter, provides the A-D conversion function, using a single ZN7400E package for external logic, and a high performance ZN424P op-amp as comparator. A ZN7413E dual Schmitt provides the necessary clock and conversion oscillators, no sync is needed here. Channel selection is by the 10 turn potentiometer 'Main Tune' or, optionally, by preset potentiometers, to preferred channels. Resistance values for the pots are not critical.

The binary output is converted to BCD by the 74185 and latched to provide a steady output signal, i.e. when a particular channel has been selected no jumps occur during cycling. The conversion oscillator periodically checks the state of the input voltage, by a fresh conversion on the ZN425E, and updates the latches when the status command

indicates that the conversion is complete. The BCD signals drive 7-segment indication of channel number and provide the drive outputs for either a modulo-N digital synthesiser, a crystal-bank synthesiser, or a crystal selector. Features of the system are:

1. Bi-directional, quasi-continuous tuning on a single control.
2. Electronic tuning lock.
3. Simple switching between 'tune' and 'preferred channel' operation.
4. Preferred channels selected by preset potentiometers operating through to the synthesiser. Channels are user-alterable.
5. Inherent non-volatile 'memory' on potentiometers.
6. Channel number indication shows channel actually in use, particularly suitable for non-co-channel working, repeaters, etc.

In addition, a scanning facility can be easily added if the receiver used has a squelch switched output.

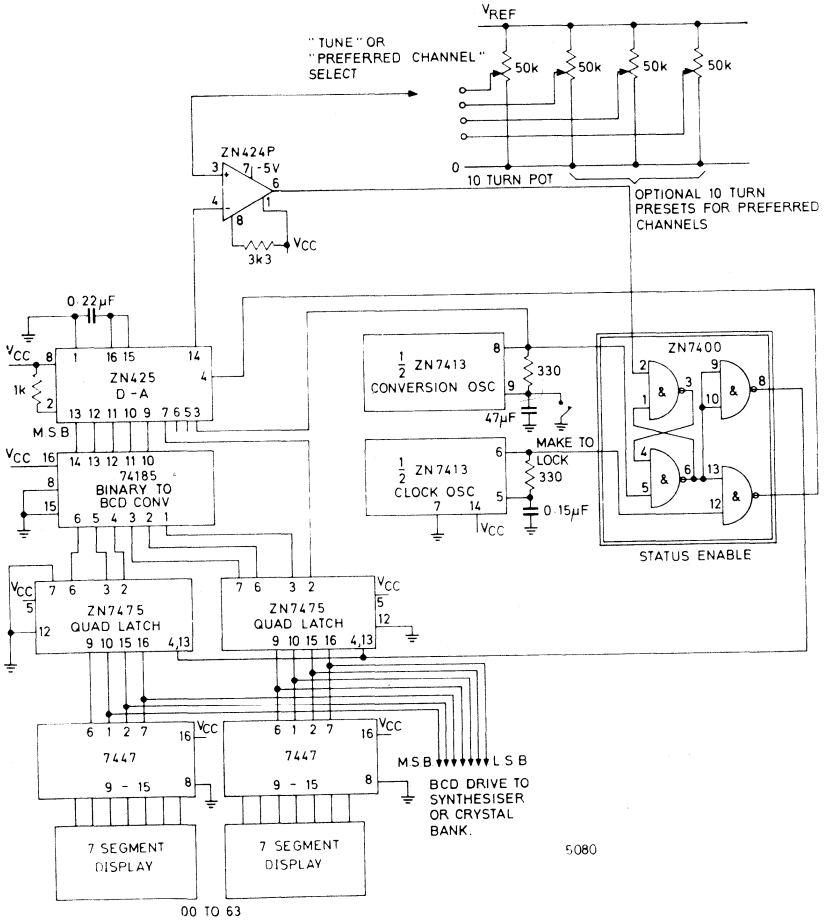


Fig. 14 Channel selector, 64 way

3.6 Bargraph Display Drive System

The ZN425E may be used in its continuous ramp mode very advantageously in conjunction with linear light emitting diode (LED) displays, e.g. Bargraphs. This is because the LED displays lend themselves to being accessed in a matrix fashion using a time sharing or multiplexing technique. This allows a reduction in the number of connections required, to m + n in an array of m n diodes (Fig. 15a) This reduction in connections also allows a simplification of the drive system, as described below.

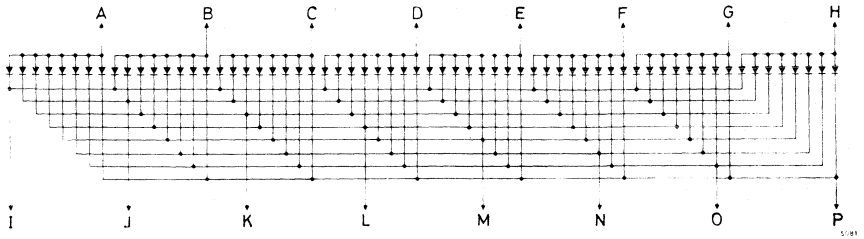


Fig. 15a Diode matrixing connections

The simplest technique for providing for a bar output whose length is proportional to an analogue input is shown in Fig. 15b. The ZN425E is driven in its continuous ramp mode. The six most significant digits from the counter are then decoded into two lots of 1 out of 8 drives. These drives then access the LEDs in a multiplexed fashion, so that the 64 LEDs are accessed once each in turn in a complete scan cycle. A high clock frequency is selected which ensures that the flicker rate is fast enough and thereby indistinguishable to the eye.

At the same time as the LED scan cycle is taking place, the ZN425E provides a staircase analogue output, as shown. This is compared with the analogue input in a comparator, whose output controls the display enable. Thus while the ramp is less than the analogue input, the LEDs being scanned are enabled (the start of the Bargraph line), while once the ramp output is larger than the analogue input, the drives to the LEDs further along the line are inhibited. This, therefore, provides an illuminated bar length proportional to the analogue input.

This system as it stands suffers from a minor disadvantage, in that the duty cycle for accessing each LED is 1/m n, or 1/64 for the case of Fig. 15b. Although the LEDs become more efficient with pulsed operation, 1/64 duty cycle does not provide adequate brightness for some applications.

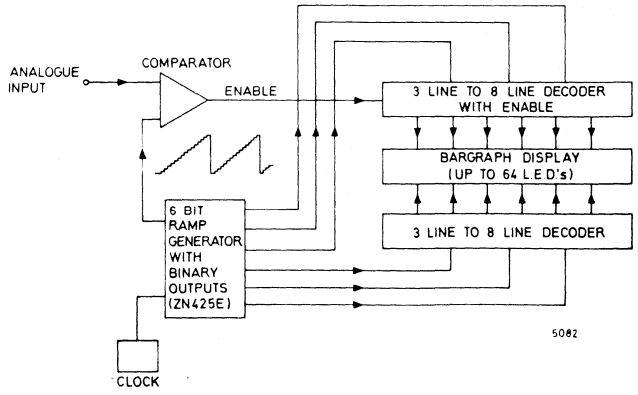


Fig. 15b Simple bar display schematic drive system

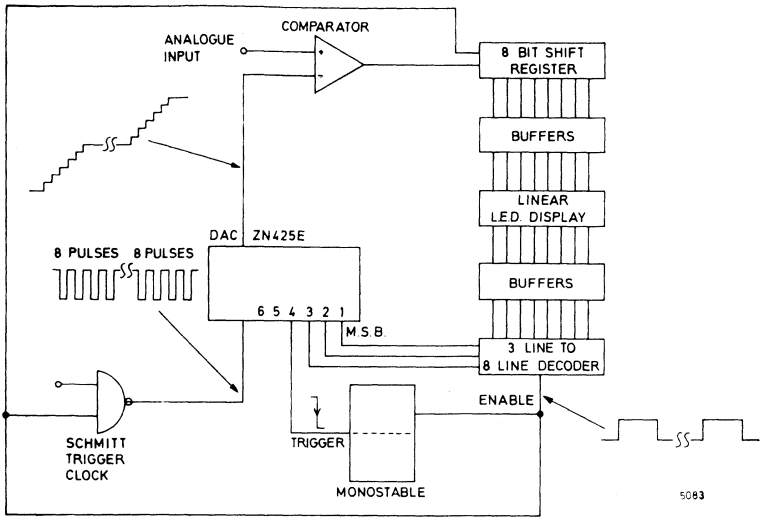


Fig. 15c Improved bar display schematic drive system

A technique to overcome this objection is shown in outline in Fig. 15c. The technique used here is to load a shift register rapidly serially, and subsequently use this register to provide LED multiplex drives in parallel. This means that the duty cycle for accessing the LEDs is improved (for a 64 LED array) from 1/64 to just less than 1/8. This is quite sufficient for acceptable brightness in virtually all applications.

This system operates as follows. While the monostable is in its mode of loading the shift register, the ZN425E staircase output increases in 8 discrete steps. Simultaneously the shift register is loaded with the comparator output to provide serial to parallel conversion. The comparator output is thus effectively changed from serial access to parallel access of the linear LED array.

When the monostable changes over to its (longer period) display mode, the LED array is accessed, and the LEDs are driven or otherwise according to the enable or disable information stored in the shift register. The display is incidentally disabled while the mono is loading the register.

To provide an example of operation, suppose the bar is to have the first 37 LEDs displayed, with the rest blanked. Starting from the ZN425E being reset and the mono in its register load state, operation is as follows.

The mono allows eight clock pulses through the gate to the ZN425E, after which the ZN425E count pulse retriggers the mono. These eight pulses generate the first eight steps from the analogue output, which produce from the comparator a continuous display enable (say logic 1). These are loaded into the shift register which thus finishes with 11111111 in parallel to the LED display.

At this point the mono is tripped into its display mode, and the counter has reached 8 (or 001 000). However the decoder must access the first eight LEDs, so that the second decoder output is connected to the first set of LEDs. These are all illuminated.

During the second register load period, the cycle is repeated, with again all ones being loaded into the register which subsequently brightens up the second eight LEDs (9–16). The same occurs during the third and fourth mono cycles, lighting up the first 32 LEDs.

During the fifth register load period, the analogue output goes up a further eight steps. However after the fifth step the comparator changes over to load zeros for the remainder of this period into the shift register. If loaded from the left the register will then finish up as 00011111. Subsequently during the mono display period LEDs 33 to 37 inclusive will be lit, but 38 to 40 will be blanked off.

The sixth to eighth mono cycles will load zeros into the shift register, blanking off LEDs 41 to 64. The full LED scan cycle is therefore completed with the desired effect.

Typical system clock rates are 400 kHz, and typical monostable periods 500 μs for the values shown

An actual circuit to achieve this is shown in Fig. 16 and it may be seen that this is elegant and simple, The type of display which may be accessed in this way is the Bowmar Microstic R1M-053-66A, which is connected in eights on its common anodes. This has 64 red LEDs and a further two LEDs at the ends, one to show the display is working, and the other for over-range. Similar techniques may be used with the 106 LED version.

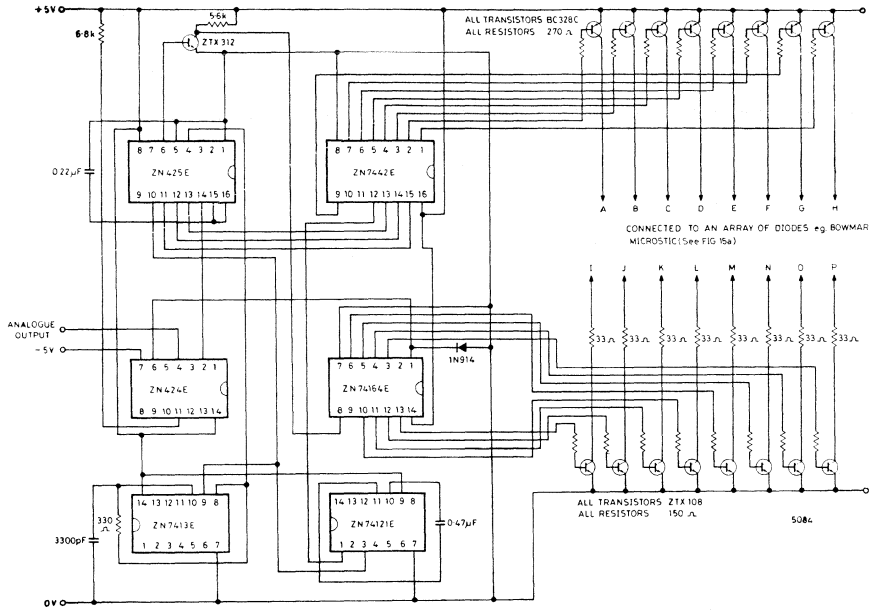


Fig. 16 Column display drive system

3.7 Up Down or Tracking

The counter on the ZN425E is only an up counter, and some systems, e.g. tracking converters or servos, may require an up/down counter. This is conveniently provided externally, e.g. the ZN74193E using the ZN425E purely in its D-A converter mode and ignoring the counter (Fig. 17). While this may appear to be inelegant it is nevertheless economically sound.

4. MULTIPLY/DIVIDE

4.1 Multiplier

The reference supply to the D-A section of the ZN425E has been purposely left on an uncommitted terminal, so as to allow connection either from its own reference or from an external reference. The point about an external reference is that it allows a multiplying effect, in that the analogue output is proportional both to the binary code and the reference voltage. For this reason this type of DAC is called a multiplying DAC.

Practical limits in multiplying voltages are 0V and 3V.

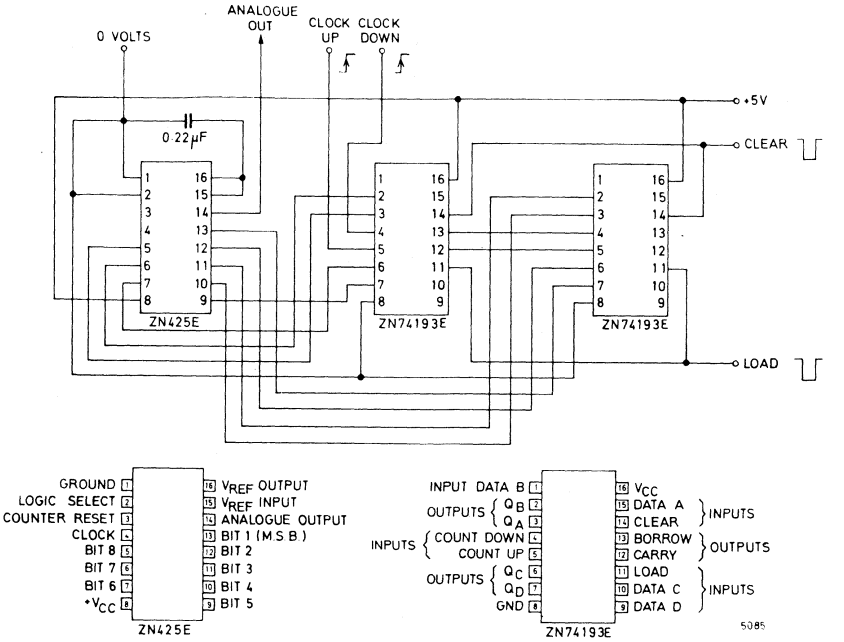


Fig. 17 Up/down counter or tracking DAC circuit

4.2 Variable Frequency Divider

If a ZN425E is operated in its continuous ramp mode in conjunction with a comparator whose output is fed back to the counter reset, a variable frequency divider can be constructed as shown in Fig. 18a. Here an analogue voltage can be used to control the number of steps before reset is applied, the overall effect being to provide variable frequency division under the control of a potentiometer.

4.3 Voltage Controlled Oscillator

The schematic of Fig. 18a may also be used as a voltage controlled oscillator. However the frequency is the inverse of the applied voltage, though the period is, of course, proportional. The corresponding circuit of Fig. 18b gives an output frequency or pulse rate which is inversely proportional to applied voltage as shown in Fig. 18c. It is, however, in some cases more desirable to produce an output frequency directly proportional to applied voltage. This is accomplished by the circuit depicted by Figs. 19a and 19b and involves the use of an inverse scaler described in the next section, for which a brief mention is necessary to understand the basic operation of the V.C.O.

By using a DAC in the feedback loop of an operational amplifier an output voltage is derived which is inversely proportional to a digital input number to the DAC. Clock pulses applied to the DAC counter will produce a repetitive output waveform which is a hyperbolic $\frac{1}{n}$ function. This waveform is applied to the inverting input of a comparator whilst the analogue input voltage to be frequency converted is applied to the non-inverting input. At the instant they become equal the comparator changes state and operates the Schmitt trigger which resets the DAC counter. The result is a train of negative going pulses whose frequency is directly proportional to the applied input voltage. This follows simply because if F_{Clock} = clock frequency to the DAC counter, and F_{out} = output frequency, then $F_{out} = \frac{F_{Clock}}{n}$ where n = digital input number, and analogue input voltage to the comparator $V_{in} \propto \frac{1}{n}$

Therefore, $F_{out} \propto V_{in}$ and the appropriate characteristic is shown in Fig. 19c.

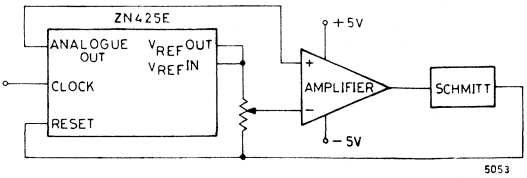


Fig. 18a Variable frequency divider or VCO schematic

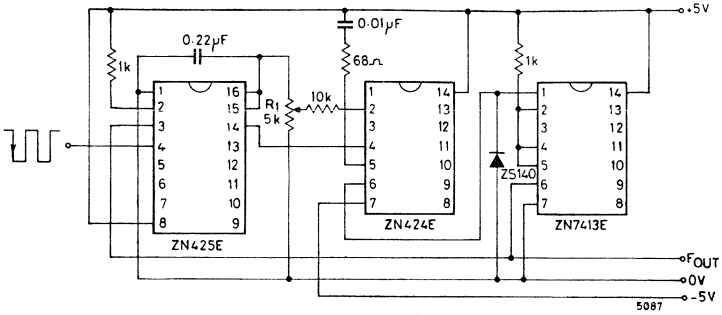


Fig. 18b Variable frequency divider or VCO circuit

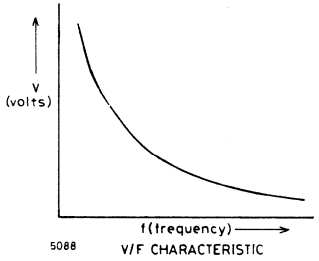


Fig. 18c VCO characteristics

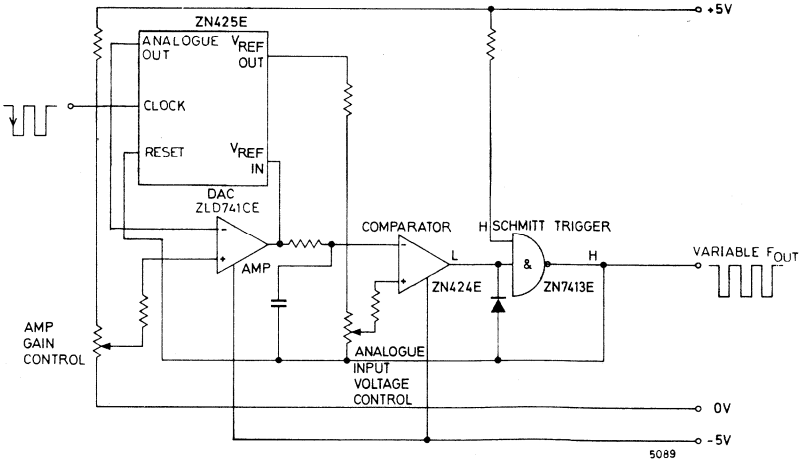


Fig. 19a Schematic of VCO giving frequency proportional to voltage

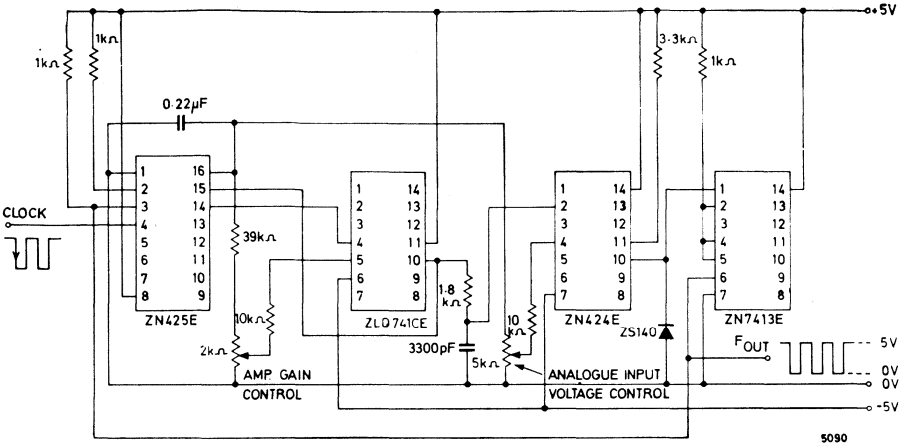


Fig. 19b Circuit of VCO giving frequency proportional to voltage

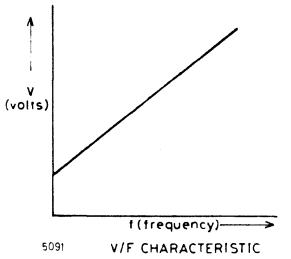


Fig. 19c VCO characteristics

5. FUNCTION GENERATION

By virtue of the multiplying function, the ZN425E may also be used for function generation as described below.

5.1 Inverse Scaler

If a DAC is operated in the feedback loop of an operational amplifier then the amplifier gain is inversely proportional to the input digital number or code to the DAC. The version giving scaling inversely proportional to positive voltage is shown in the schematic of Fig. 20a and the practical circuit of Fig. 20b.

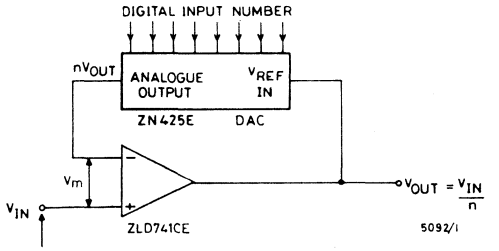


Fig. 20a Inverse scaler schematic

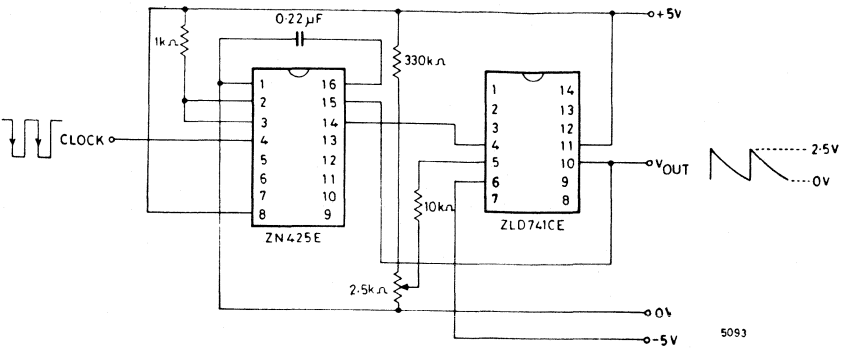


Fig. 20b Inverse scaler circuit

If A = open loop gain of the operational amplifier, and n is a fractional number representing any digital input (00000000 to 11111111 for 8 bits), that is a fractional number between 0 and $\frac{255}{256}$ then from the diagram $V_{out} = AVm$, and $Vm = (V_{in} - n\,V_{out})$

$\therefore\ V_{out} = A\,(V_{in} - n\,V_{out})$ from which $V_{out}\,(1 + An) = AV_{in}$ $\frac{V_{out}}{V_{in}} = \frac{A}{1 + An}$

Since $An \gg 1$, $(A \simeq 100{,}000)$ then $\frac{V_{out}}{V_{in}} = \text{Gain (G)} \simeq \frac{A}{An} = \frac{1}{n}$

For $n = 1\ LSB = \frac{1}{256}$ then the maximum allowable input voltage V_{in} to prevent saturation $(V_{sat} \simeq 4V) = \frac{4}{256} \simeq 15\ mV$.

If n = 0 then G = A and for a fixed input level the amplifier output will normally be equal to the saturation voltage since $A \simeq 100{,}000$.

The complementary mode (scaling inversely proportional to negative voltage) is shown in Fig. 20c (schematic) and Fig. 20d (practical circuit).

$$V_m = \left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{R_I + R_F}\right)\right], \text{ and } V_{out} = -AV_m$$

If $\frac{R_I}{R_F} = F_I =$ inverting feedback return then

$$V_{out} = -A\left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{1 + F_I}\right) F_I\right]$$

From which

$$V_{out} = -\left[\frac{A\,V_{in}}{1 + F_I + nAF_I}\right]$$

If the input voltage V_{in} is negative with respect to ground, then

$$\text{Gain (G)} = \left[\frac{A}{1 + F_I + nAF_I}\right]$$

If we make $F_I = 1$, i.e. $R_I = R_F$ then $G = \left[\frac{A}{2 + nA}\right]$

But $nA \gg 2$ (since $A \simeq 100{,}000$)

and $G = \frac{A}{nA} = \frac{1}{n}$ as with the non-inverting circuit.

Figs. 20a and 20c illustrate both types of inverse scalers, where a repetitive waveform of a $\frac{1}{n}$ function is generated by feeding clock pulses to the counter of the DAC.

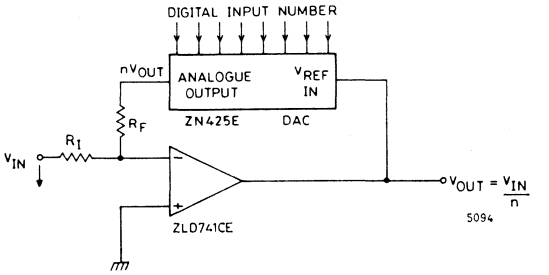


Fig. 20c Complementary inverse scaler schematic

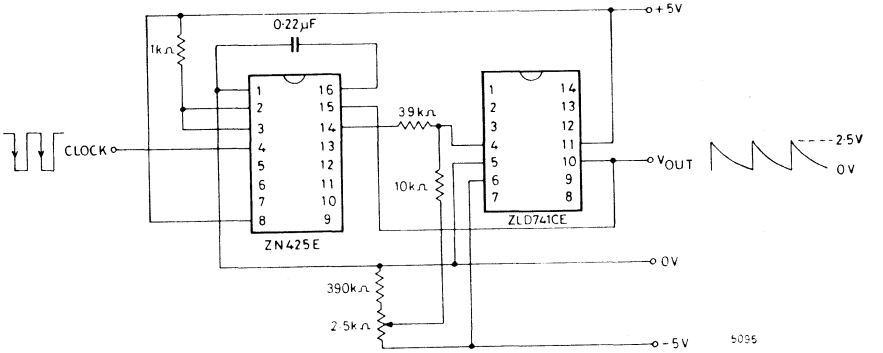


Fig. 20d Complementary inverse scaler circuit

5.2 Parabola

The multiplying action of the ZN425E may be used to generate a parabolic waveform shown schematically in Fig. 21a and a practical circuit Fig. 21b.

Basically the circuit operates as follows:

A continuous ramp output is generated by feeding clock pulses to the counter of a ZN425E DAC using its internal reference which is buffered, level shifted, and finally inverted using two operational amplifiers, so that the inverted ramp starts at a peak amplitude ($V_{1\ REF} = 2.5V$) and decreases linearly to zero. This is then used as an external reference supply for a second ZN425E DAC whose bits are connected to the first DAC for synchronous clocked operation. The resulting analogue output from the second DAC is a repetitive parabolic waveform whose peak amplitude is equal to $\frac{V_{1\ REF}}{4} = \frac{2.5}{4} = 0.625V$.

This follows because,

If N = a fractional number representing the digital input to both DACs then the analogue output voltage from the first DAC = An (where $A = V_{1\ REF} = 2.5V$).

This is then inverted and level shifted to provide the reference voltage to the second DAC = $(A - An) = V_{2\ REF}$.

Therefore the analogue output from the second DAC = $n\ (A - An) = An - An^2$ which is the equation of a parabola about the x axis of the form $y = ax^2 + bx + c$.

Peak amplitude of the parabola occurs when $n = \frac{1}{2}$

for which $V_{out} = \frac{1}{2}\left(A - \frac{A}{2}\right) = \frac{A}{4} = \frac{V_{1\ REF}}{4}$ as stated.

It should be noted that the ramp output from the non-inverting buffer amplifier will inherently have a gain greater than unity, and therefore its peak amplitude will be some factor in excess of $V_{1\ REF}$. However the ramp inverter and level shifter introduces corresponding attenuation to compensate this so that gain and level shift controls provide adequate adjustment in obtaining the desired inverted ramp output of peak amplitude.

$A = V_{1\ REF} = 2.5V.$

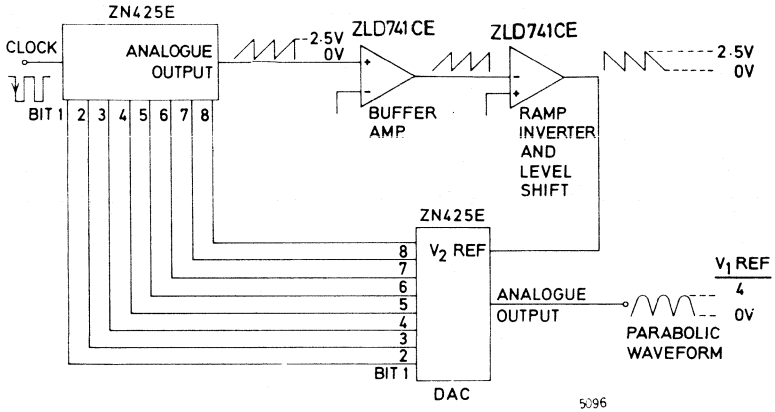


Fig. 21a Parabolic waveform generator schematic

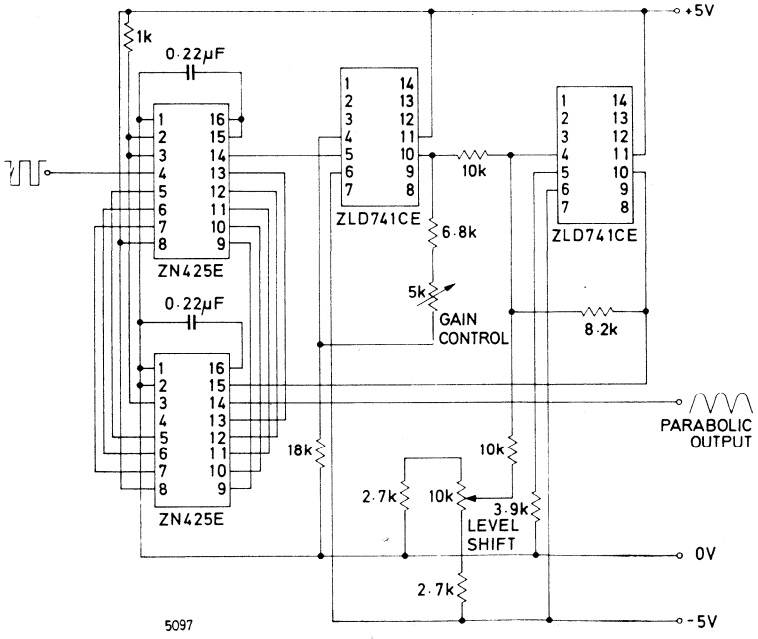


Fig. 21b Parabolic generator circuit

5.3 Log Approximation

A more complex function $y = \log n$ can be performed with the aid of previously described building blocks. A schematic arrangement as shown in Fig. 22a and the corresponding practical circuit of Fig. 22b provides a repetitive logarithmic relationship. The basic method is as follows.

An inverse scaler is used to generate an output voltage which is inversely proportional to a digital input number n to a ZN425E DAC. This voltage is then converted to a frequency or pulse rate using a VCO whose output frequency is proportional to an applied voltage The derived train of pulses of varying mark to space ratio are then fed into the counter of a final ZN425E DAC, these are integrated and a logarithmic output $\int\left(\frac{1}{n}dn = \log n\right)$ is obtained.

The period of the analogue $\frac{1}{n}$ function is dependent upon the input frequency to the inverse scaler. To rapidly convert this function to a pulse train and to generate a sufficient number of pulses for integration during this period, the clock frequency to the VCO derived from the Schmitt trigger must be high. The lower input frequency to the inverse scaler in synchronism with this clock frequency is obtained by using two ZN7493A dividers and, equals the clock frequency divided by 256. For the CR values indicated in the Schmitt trigger $F_{Clock} \simeq 512$ kHz therefore the input frequency to the inverse scaler $= \frac{512 \times 10^3}{256}$ Hz $= 2000$ Hz. And the output repetition frequency of the $\frac{1}{n}$ function $= \frac{2000}{256}$ Hz, for which the period $= \frac{256s}{2000} = 128$ ms.

Some means must be incorporated of resetting the counter on the final ZN425E DAC and thereby the logarithmic analogue output to zero at the completion of a full cycle of input pulses. Otherwise the analogue output would continue to increase with each cycle of pulses until it equalled the internal reference voltage, resulting in a 3 cycle logarithmic waveform. This is accomplished by using the negative going edge from the 4th significant bit which in fact resets the counter on the final DAC before the completion of a full cycle of input pulses. Whereas to be strictly correct resetting should be effected from the MSB ; bit 4 having been selected purely for convenience as it allows the logarithmic characteristic to be more easily displayed on the oscilloscope, since it accounts for a greater proportion of the output waveform, with negligible loss in amplitude.

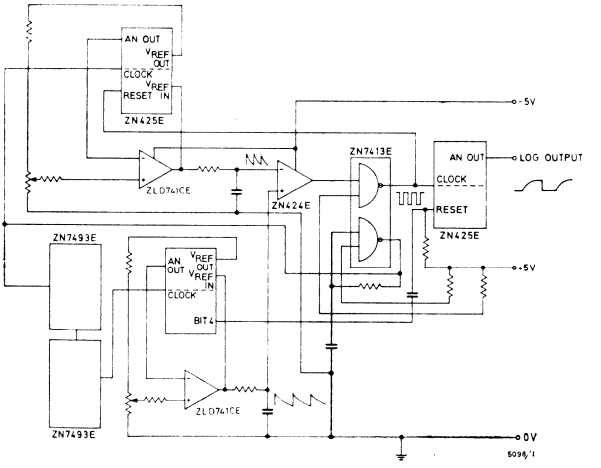


Fig. 22a Logarithmic waveform generator schematic

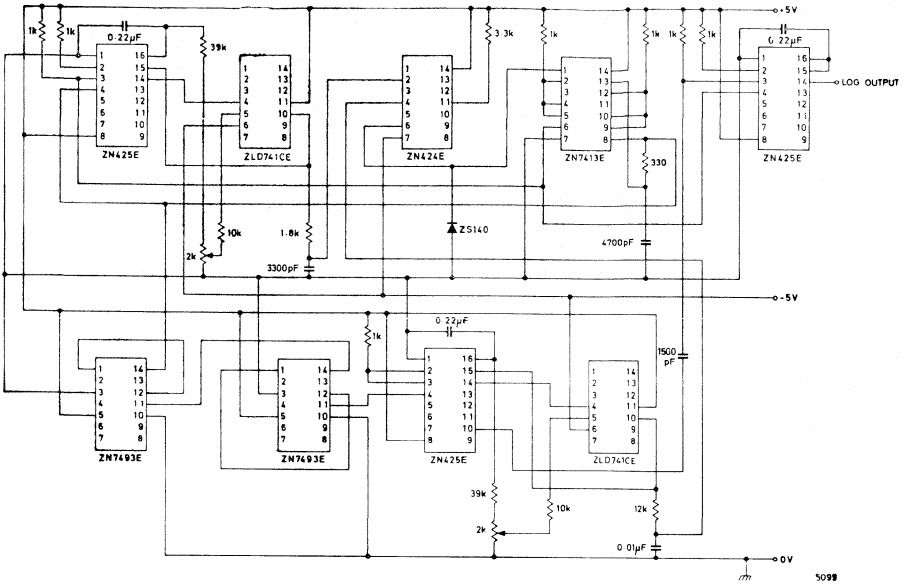


Fig. 22b Logarithmic waveform generator circuit

Microprocessor Interfacing Using The ZN427/ZN428 Data Converters

Analogue I/0 Interface System for the 6800 Microprocessor

Interfacing the ZN427 A to D Converter with the Microprocessor System

Interfacing the ZN428 D to A Converter with the 8085A Microprocessor System

Analogue I/O Interface System for the 6800 Microprocessor

By SCOTT BIRD, Feranti Electronics Ltd.

Conventional Analogue I/O systems for Microprocessars are generally high accuracy, high cost, hybrid module/P.C. board assemblies, available only in one fixed configuration of I/O channels, (i.e. 16 Input and 2 Output channels). This Application Note describes how a low cost Analogue I/O system may be produced for the 6800 microprocessor using FERRANTI ZN427 A/D and ZN428 D/A converters with the 6820/6821 Peripheral Interface Adapter (PIA) I.C. This combination produces a versatile system which can be configured to the designer's particular I/O requirements, and which can also be expanded without major modifications to the hardware. The advantages of interfacing to the microprocessor via the PIA are that it provides a simple, easily expandable system, without additional address decoding and line buffering hardware, and it also simplifies timing problems associated with a direct bus interface.

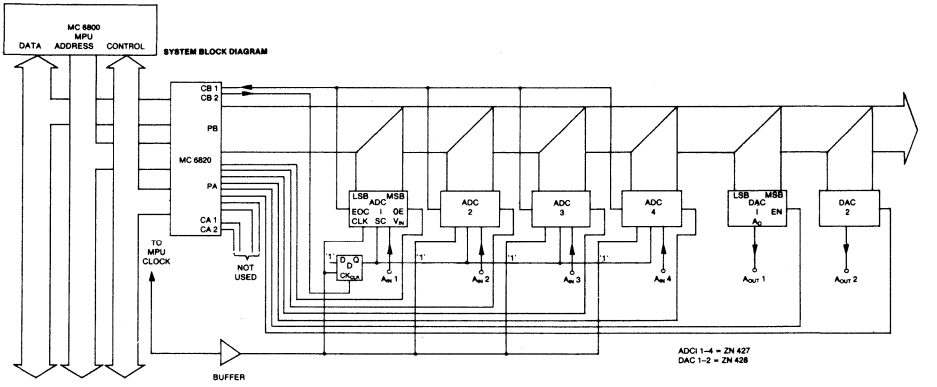


Fig. 1 System Block Diagram

The ZN427 A/D Converter

The ZN427 is an 8-bit, successive approximation A/D Converter. It features fast 15 μs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D/A converter, a 2.5 V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.
Operation of the ZN427 is best described with reference to the timing diagram—Fig. 3. Conversion is initiated by a START CONVERT (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

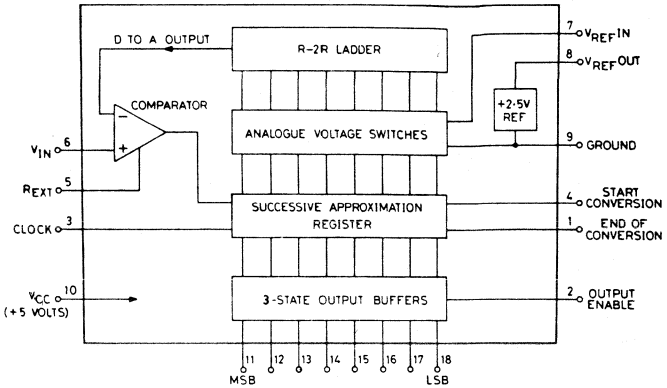


Fig. 2 ZN427 Logic Diagram

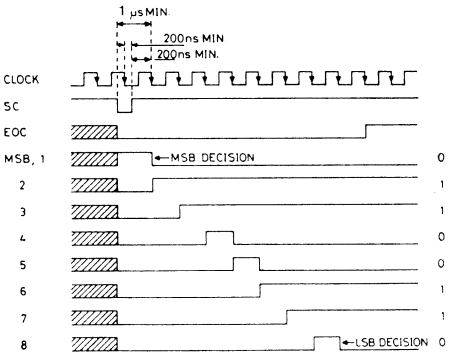


Fig. 3 Timing Diagram

1. The leading edge of the SC–pulse should precede the first active (negative going) edge of the clock (after the trailing edge of the SC pulse) by at least 1.5 μs to allow for MSB setting.
2. The trailing edge of the SC pulse must not occur within ± 200 ns of a negative going edge of the clock.
3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse.
   Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D to A converter of $V_{REF\ IN/2}$.
   This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REF\ IN/2} > V_{IN}$, or else to keep it at '1', Bit 2 is switched to '1' on the same clock edge, and on the next edge a decision is made about Bit 2, again by comparing the D/A output with V_{IN}. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is a valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is an '0' and are enabled when the OE input is taken to '1'.

The ZN428 D/A Converter

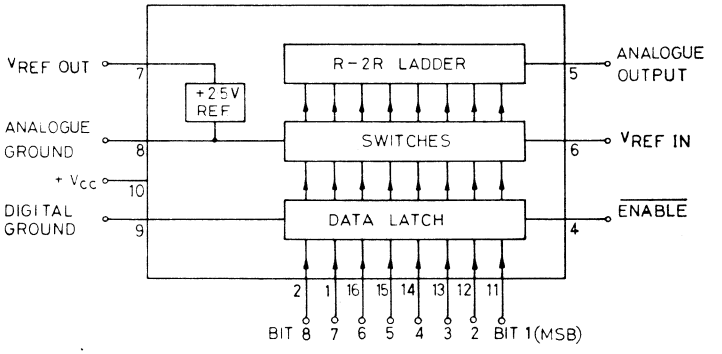


Fig. 4 Logic Diagram

The ZN428 is a monolithic 8-bit D/A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{ENABLE}}$ is at logic '0' and the data is held when $\overline{\text{ENABLE}}$ is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800 ns settling time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0 V to $V_{REF\ IN}$ through a 4 kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 6800 Microprocessor System

It is assumed that the reader is fully conversant with the 6800 microprocessor family, information on which can be found in the Motorola M6800 Microprocessor Applications Manual, so only a brief description is given here.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL the 6800 requires only a single + 5 volt power supply, it features an instruction set of 72 instructions with 7 addressing modes and full 65 k byte memory addressing capability. The microprocessor communicates with its external memory and all I/O devices via an 8-bit bi-directional data bus and a 16-bit address bus.

The 6820/21 Peripheral Interface Adaptor (PIA) provides a flexible means of interfacing byte-orientated peripherals to the microprocessor, through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed to act either as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

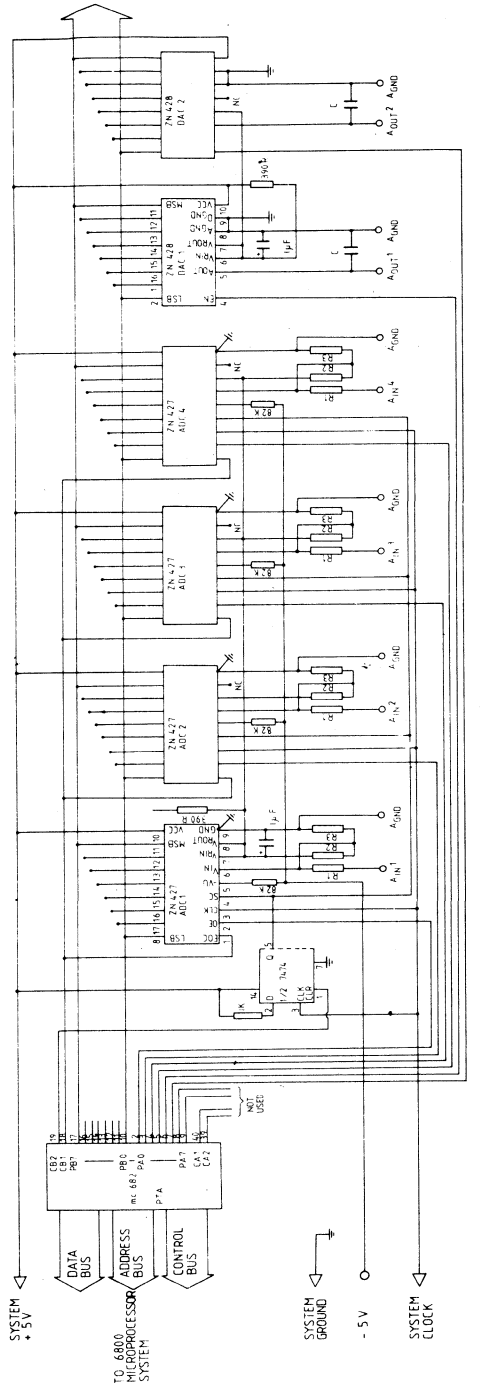
The Analogue I/O Interface

The system described in this application note provides 4 Analogue Input and 2 Analogue Output channels—see the System Block Diagram Fig. 1 and the detailed Circuit Diagram Fig. 5. Other configurations can easily be produced—these are discussed later in this note.

The peripheral data lines PB0—PB7 of the PIA are connected to the binary data outputs of the ZN427s and the data inputs of the ZN428s to produce a common 8-bit data bus for the converters. Peripheral lines PA0—PA5 are programmed as OUTPUTS and provide individual OUTPUT ENABLE and $\overline{\text{ENABLE}}$ signals for the ZN427 and ZN428 respectively. A common, simultaneous START CONVERT signal for the ZN427s is produced from the CB2 control line programmed in the SET/RESET output mode and used in conjunction with a 'D' type flip-flop. The END OF CONVERT outputs from the ZN427s are commoned together and drive the CB1 input of the PIA which can be programmed to generate a microprocessor interrupt signal. In this system configuration, the peripheral lines PA6, PA7 and the control lines CA1, CA2 are not used.

The ZN427 clock signal can be generated either asynchronously from an external source or from the microprocessor clock. If using the MC6871B microprocessor clock device (as supplied with the Motorola MEK6800D2 Evaluation Kit), which produces a 614.4 kHz clock signal, then the ϕ 2 TTL output of this can be used directly. Note that the maximum clock frequency of the ZN427 is specified as 600 kHz, although the device will function up to greater than 1 MHz, but at reduced accuracy due mainly to the response time of the comparator. Therefore, if using a microprocessor with a clock frequency greater than 600 kHz, then this can either be divided down to less than 600 kHz, or it may be used directly up to approximately 1 MHz if some loss of accuracy can be tolerated. The advantage of using the microprocessor clock over an external clock is that it allows an accurate calculation of the conversion time to be made in terms of the microprocessor machine cycles eliminating the need to use microprocessor interrupts.

The START CONVERT pulse is generated using a 'D' type flip flop ($^1/_2$ ZN74L74) in order to meet the timing requirements discussed earlier. A conversion cycle is initiated by outputting a logic '0' followed by a logic '1' from the CB2 line of the PIA. This drives the CLEAR input of the 'D' type and sets the START CONVERT (SC) input of each 427 to a logic '0' via the Q output. The first positive going clock edge after the CLEAR input is returned to a logic '1' will clock the 'D' type and set the SC input of each ZN427 to a '1' allowing the conversion cycle to proceed. Note that while the SC input of the ZN427 is at a logic '0' level the MSB output will be driven to a logic '1' and all other data outputs to a logic '0' and the conversion cycle will be held. On the 9th negative clock edge after the START pulse the END OF CONVERSION outputs will go to a logic '1' signifying the end of the conversion cycle. This can be detected by programming the



NOTE FOR 10 V UNIPOLAR OPERATION -
R1 = 10 K POT + 11 K IN SERIES
R2 = 5 K6
R3 = 1 M POT + 680 K IN SERIES

FIG 5 - SYSTEM CIRCUIT DIAGRAM

PIA to set the microprocessor interrupt input on the positive going edge of the CB1 control line. The EOC outputs of up to four ZN427s can be "wire or'd" together to produce a common interrupt line as shown in Fig. 5. Alternatively, if using the microprocessor clock (at up to 1 MHz), then the EOC output will always occur within 10 microprocessor machine cycles after the instruction setting the CB2 control line back to a logic '1'. A suitable fixed delay can therefore be built into the program to allow for the conversion time.

The binary output data of each ADC can be read by programming the peripheral lines PB0–PB7 as INPUTS and loading the data onto the converter bus by outputting a logic '1' on the appropriate PA peripheral line in order to enable the 3-state output buffers of the ADC. A microprocessor read instruction of the PIA peripheral register 'B' will then transfer the data to the microprocessor. Obviously the program should be so arranged that, in order to avoid bus contention problems, only one ADC is enabled at any one time.

The circuit diagram, Fig. 5 shows the ZN427s connected for a unipolar input range of 0 to + 10 volts. Other ranges, eg + 5 V, ± 10 V and ± 5 V, can readily be obtained by using a simple resistor network as shown in the ZN427 data sheet.
The negative supply shown for the ZN427 is from − 5 volts through an 82 kΩ resistor. By suitable choice of resistor value any negative supply between − 3 and −30 volts may be used. For applications where only a single + 5 volt supply is available, a simple diode pump circuit can be used to generate the negative supply. Further information on the negative supply and a diode pump circuit suitable for up to 5 ZN427s is shown in the data sheet.

Data is outputted from the system by programming the peripheral data lines PB0–PB7 as OUTPUTS and writing the binary data from the microprocessor into the PIA peripheral register 'B'. The $\overline{\text{ENABLE}}$ input of the relevant ZN428 is driven to a logic '0' and back to logic '1' via the appropriate PA peripheral line, which will transfer the data from the converter bus to the input data latches of the ZN428. Again the programmer must ensure during an output data transfer that all the ZN427s and the other ZN428 are disabled.

The Analogue Outputs of the ZN428 are shown, taken directly from pins 5 and 8 which will provide an output range from 0 volts to $V_{REF\ IN}$ through a 4 kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any "glitches" which may be present. The value of this capacitor depends on the system noise and the response time required, however for the minimum specified settling time it should not be greater than 100 pF. An output buffer amplifier was omitted from the ZN428 design in order to allow optimum settling time, flexibility and lowest cost. Both Unipolar and Bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate Analogue and Digital ground pins. These can normally be connected together close to the device and taken to signal ground. However for noisy systems or environments it may be advisable to keep the Analogue ground pins for each individual ZN428 separate from the Digital ground pin, and to connect each Analogue ground to a single common earth point in the system away from sources of digital noise such as clock oscillators, digital buses, etc. The Analogue output ground line or terminal should also be taken direct to this common earth point. (Note: The maximum voltage between Analogue and Digital grounds is limited to 200 mV.)

A common reference voltage can be provided by connecting the $V_{REF\ OUT}$ pin of one converter to the $V_{REF\ IN}$ pins of up to five converters (i.e. either ZN427s or ZN428s). This useful feature saves power and gives excellent gain tracking between converters. Fig. 5 shows the four ZN427s driven from one internal reference and the two ZN428s from another.

Note that in this application the dynamic characteristic of the ZN427/428 (i.e. Enable/Disable delay times, etc.) should not present any problems since they are much less than the microprocessor instruction execution times and need not be considered in the programming.

Program Example

A simple program which illustrates the ease of controlling the ZN427/428 with the PIA is shown on page together with the Flow Diagram, Fig. 6. The object of the program is to read the analogue voltage inputs to ADCs 1 and 2, calculate the mean value and output this on DAC1. A similar operation is performed on the inputs of ADCs 3 and 4 and outputted on DAC2.

It is assumed that the PIA has been reset which has the effect of zeroing all the PIA registers. This sets all the peripheral and control lines as INPUTS and disables the interrupts. Initially the Index Register is loaded with the PIA base address in order that the Indexed Addressing Mode can be used throughout the program to address the PIA. The peripheral lines PA0–PA7 are programmed as OUTPUTS and the Control Registers set so that control line CB2 operates in the SET/RESET output mode and the interrupt Flag bit CRB-7 is set with a positive going edge on control line CB1. All the converters are disabled by outputting 30H on the PA lines which sets the OUTPUT ENABLE inputs of the ZN427s to a logic '0' and the $\overline{\text{ENABLE}}$ inputs of the ZN428s to a logic '1'. A dummy read is made of the B Data Register to clear the Interrupt Flag bit CRB-7.

A START signal is then generated via control line CB2 by toggling bit CRB-3 in Control Register B. The end of the conversion cycle is detected by testing the Interrupt Flag bit CRB-7 and looping at this point in the program until it goes to a '1'. (Note: The microprocessor interrupt request lines $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ are disabled.) The output of ADC1 is now read by driving peripheral line PA0 to a logic '1', and the data is stored in the microprocessor Accumulator B, ADC2 is read in a similar way by setting PA1 line to a logic '1' and storing the data in Accumulator A. The mean value of the readings is found by adding the Accumulators and rotating the result right, one bit through carry, this is equivalent to dividing by 2. The result is saved in the memory location labelled 'TEMP 1'. The process is repeated on ADC3 and ADC4, enabling the ADC outputs by setting lines PA2 and PA3 in turn to a logic '1', and storing the computated result in location 'TEMP 2'.

The Data Direction Register B is now accessed and the peripheral lines PB0–PB7 changed to OUTPUTS. The data stored in 'TEMP 1' is outputted onto the converter bus and DAC 1 enabled by toggling line PA4 in a logic 1-0-1 sequence, which will transfer the binary data from the bus to the DAC input latches and hence to the Analogue Output. A similar sequence is performed on DAC2 with the data from 'TEMP 2', using PA5 line to drive the $\overline{\text{ENABLE}}$ input. The program is terminated with a Software Interrupt, SWI, returning control to the Monitor Program.

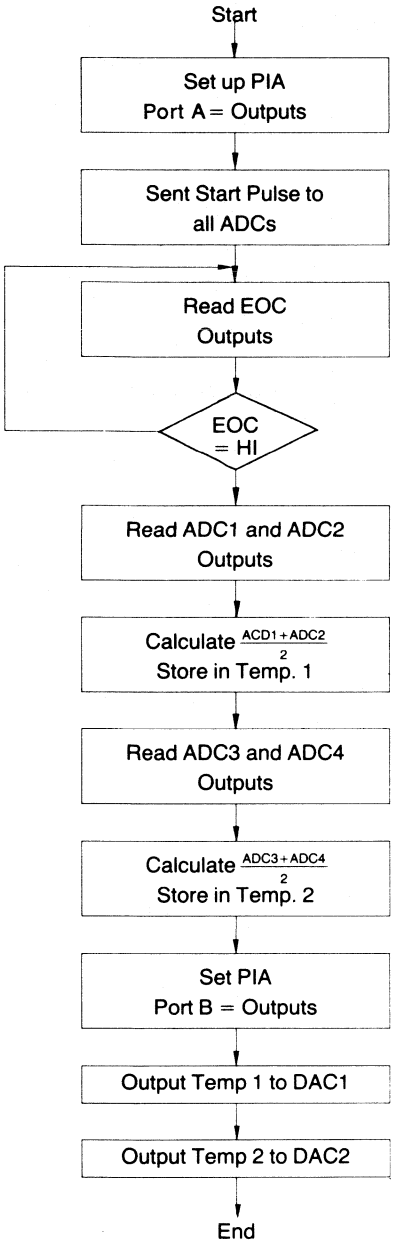


FIG. 6 PROGRAMME FLOW DIAGRAM

PIA PORT ALLOCATIONS

PORT A

PA0	ADC1 OE Input
PA1	ADC2 " "
PA2	ADC3 " "
PA3	ADC4 " "
PA4	DAC1 $\overline{\text{EN}}$ Input
PA5	DAC2 " "
PA6	NOT USED
PA7	NOT USED

PORT B

PB0	BINARY DATA LSB
PB1	" " LSB + 1
PB2	" " LSB + 2
PB3	" " LSB + 3
PB4	" " LSB + 4
PB5	" " LSB + 5
PB6	" " LSB + 6
PB7	" " MSB

CONTROL

CA1	NOT USED
CA2	NOT USED
CB1	COMMON EOC OUTPUT
CB2	COMMON START LINE

PIA ADDRESSES

8004	PERIPHERAL/DATA DIRECTION REG. A
8005	CONTROL REG. A
8006	PERIPHERAL/DATA DIRECTION REG. B
8007	CONTROL REG. B

6800/6820 I/O INTERFACE – PROGRAM EXAMPLE

LOC	OBJ		COMMENT	SOURCE STATEMENT
0000	CE8004		LDX #$8004	Load PIA address to IX
3	86FF		LDA A #$FF	
5	A700		STA A 0, X	Set Port A as outputs.
7	863E		LDA A #$3E	
9	A701		STA A 1, X	Set Control Reg. A
B	A703		STA A 3, X	Set Control Reg. B
D	8630		LDA A #$30	
F	A700		STA A 0, X	Disable Converters
11	A602		LDA A 2, X	Dummy read to Clear Flag
13	8636		LDA A #$36	
15	A703		STA A 3, X	Set CB2 Low to
17	863E		LDA A #$3E	Generate Start Pulse
19	A703		STA A 3, X	Set CB2 High
1B	A603	TEST	LDA A 3, X	Read Control Reg. B
1D	8580		BIT A #$80	Test for CRB-7 High
1F	27FA		BEQ TEST	ie End of Conversion
21	8631		LDA A #$31	
23	A700		STA A 0, X	Enable ADC1 O/Ps
25	E602		LDA B 2, X	Read ADC1 O/P
27	8632		LDA A #$32	
29	A700		STA A 0, X	Enable ADC2 O/Ps
2B	A602		LDA A 2, X	Read ADC2 O/P
2D	1B		ABA	Add ADC1 + ADC2 Readings
2E	46		RORA	Divide by 2
2F	976E		STA A Temp.1	Save x in Temp. 1
31	8634		LDA A #$34	
33	A700		STA A 0, X	Enable ADC3 O/Ps
35	E602		LDA B 2, X	Read ADC3 O/P
37	8638		LDA A #$ 38	
39	A700		STA A 0, X	Enable ADC4 O/Ps
3B	A602		LDA A 2, X	Read ADC4 O/P
3D	1B		ABA	Add ADC1 + ADC2 Readings
3E	46		RORA	Divide by 2
3F	976F		STA A Temp.2	Save y in Temp. 2
41	8630		LDA A #$30	
43	A700		STA A 0, X	Disable ADC O/Ps
45	863A		LDA A #$ 3A	
47	A703		STA A 3, X	
49	86FF		LDA A #$FF	
4B	A702		STA A 2, X	Set Port B as outputs
4D	863E		LDA A #$ 3E	
4F	A703		STA A 3, X	
51	966E		LDA A Temp.1	
53	A702		STA A 2, X	Put x Data on bus
55	8620		LDA A #$20	
57	A700		STA A 0, X	Enable DAC1 I/Ps
59	C630		LDA B #$30	
5B	E700		STA B 0, X	Disable DAC1 I/Ps
5D	966F		LDA A Temp. 2	
5F	A702		STA A 2, X	Put y data on bus
61	8610		LDA A #$10	
63	A700		STA A 0, X	Enable DAC2 I/Ps
65	E700		STA B 0, X	Disable DAC2 I/Ps
67	3F		SWI	End
006E	00		Temp. 1	x data
006F	00		Temp. 2	y data

Summary

The system described in this report is by no means restricted to the configuration shown. Provided that the drive capability of the system components is not exceeded, the number and configuration of ZN427s and ZN428s which can be employed is limited only by the I/O lines available from the PIA, hence providing the Design Engineer with a wide degree of freedom in producing the system that best fulfils his requirements.

The major loading and drive characteristics of the various system components are shown in Table 1. Buffer gates can be employed where necessary to expand the drive capability of the components such as when utilising a long bus with high capacitive loading. Note that the peripheral lines from side B are used for the converter bus since these present a high impedance when programmed as inputs. Also the 6821 PIA is preferred to the 6820 because this has a 2-TTL drive capability on both A and B side peripheral lines. As stated previously up to 4 ZN427 EOC outputs can be wire–or'd together; if using more than 4, then each group can be ANDed together using a ZN7409 TTL gate to produce a single interrupt line.

If required separate START signals can be generated for each ZN427 hence allowing a microprocessor read of one ADC to be in progress while the other(s) are in a conversion cycle. However this configuration does require one peripheral line and one 'D' type flip flop per START signal line. Since only one ZN427 or ZN428 should be enabled at any one time, then it is possible to incorporate one or more Decoder types of I.C. such as the ZN74154, 4 Line to 16 Line Demultiplexer/Decoder in order to expand the system. This device could be connected with the 4 data inputs connected to 4 PA peripheral lines and the decoder enable input driven by CA2 line. Use of two such IC's would provide 32 output lines allowing an Analogue I/O system with a combination of up to 32 analogue input and output channels to be produced.

As a result of the low converter cost, low external component count and flexibility of this type of system, designs based on using one converter per analogue channel will be both a practical and economical solution to microprocessor data acqusition problems. This approach should find many new applications in areas which have previously been limited by the necessity of having to use the traditional data acqusition methods involving a single, high cost hybrid A-D converter utilising sample/hold and multichannel multiplexing techniques.

TABLE 1

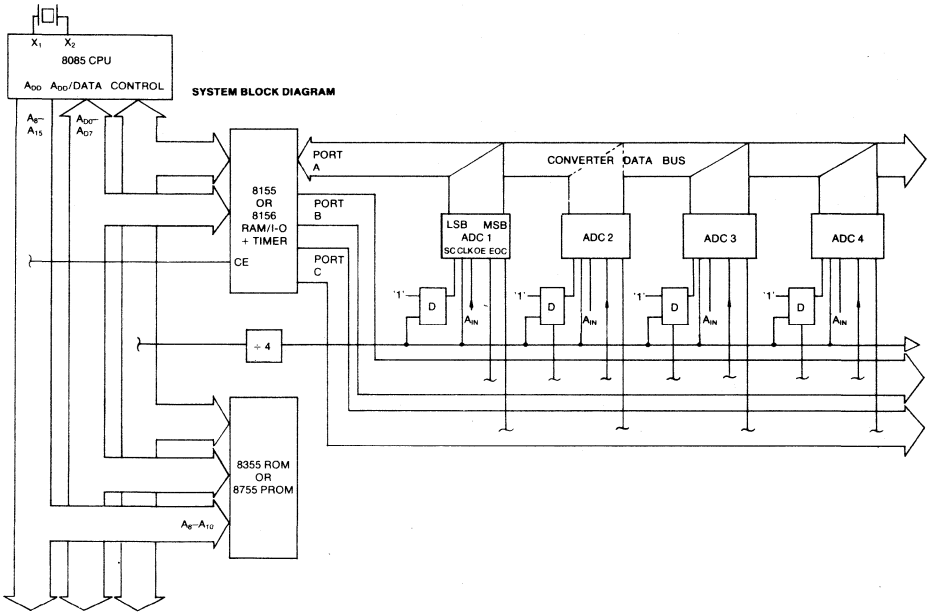
MC6820	PA0 - PA7 / CA2	PB0 - PB7 / CB2	CA1/CB1
I_{IL} I_{IH}	-1.6mA max -100μA min	)) 10μA max)	) 2.5μA max) (at V_{IN} = 0 to 5.25V))
I_{OL}	1.6mA min	1.6mA min	
I_{OH}	-100μA min	-100μA min	
MC6821			
I_{IL} I_{IH}	-2.4mA max -200μA min	)) 10μA max)	) 2.5μA max) (at V_{IN} = 0,5... 5,25 V))
I_{OL}	3.2mA min	3.2mA min	
I_{OH}	-200μA min	-200μA min	
ZN427			
I_{IL}	-5μA max		
I_{IH}	15μA max		
I_{IH} (Clock)	30μA max		
I_{OL}	1.6mA min		
I_{OH}	-100μA min		
I_{OHX} (Off state leakage)	2μA max		
ZN428	All Inputs		
I_{IL}	-5μA max		
I_{IH}	20μA max		

NOTE Currents specified at 0.4 V and 2.4 V unless otherwise stated.

Interfacing the ZN 427 A to D Converter with the 8085A Microprocessor System

by SCOTT BIRD, Ferranti Electronics Ltd.

The growth of microprocessors has lead to a demand for low cost, fast 8 bit A/D and D/A converters to interface between the real world of analogue values and the digital world of the microprocessor. Converter systems have, until recently, been mainly high cost, multiplexed, sample and hold systems usually built around a 12 bit A/D converter. The system described in this report is a low cost, expandable, one converter per channel system, based on the ZN427 8-bit A/D Converter interfaced directly to the I/O Ports of the 8155 2K bit static 'RAM', which forms part of the basic 8085A microprocessor system.



The ZN427 A/D Converter

The ZN427 is a monolithic 8-bit, successive approximation A/D Converter designed for microprocessor compatibility. It features fast 15 μs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D/A converter, a 2.5 V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

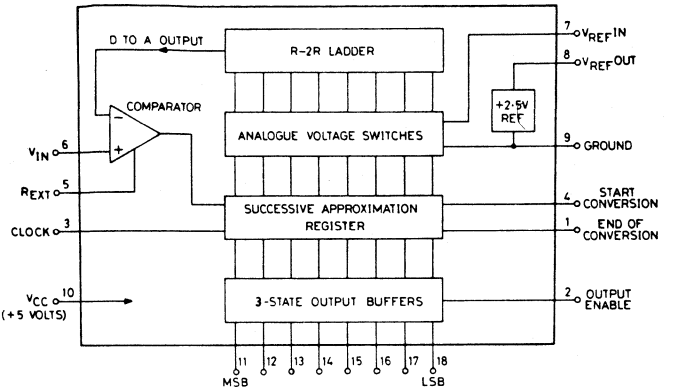


Fig. 2—ZN427 Logic Diagram

Operation of the ZN427 is best described with reference to the timing diagram.—Fig 3. Conversion is initiated by a Start Convert (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

1. The leading edge of the SC—pulse should precede the first active (negative going) edge of the clock (after the trailling edge of the SC pulse) by at least 1.5 μs to allow for MSB setting.
2. The trailing edge of the SC pulse must not occur within ± 200 ns of a negative going edge of the clock.
3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse.
   Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D to A converter of $V_{REFIN}/2$. This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REFIN}/2 > V_{IN}$, or else to keep it at a '1'. Bit 2 is switched to a '1' on the same clock edge, and on the next edge a decision is made about bit 2, again by comparing the D/A output with V_{IN}. This process is

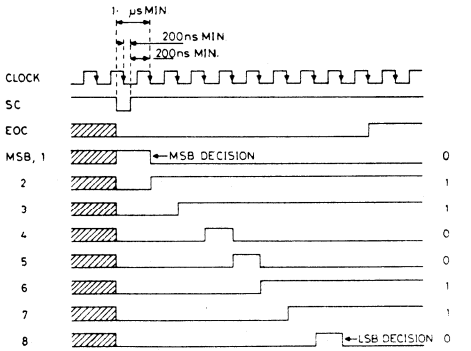


Fig. 3—Timing Diagram

repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is a '0' and are enabled when the OE input is taken to a '1'.

The 8085A Microprocessor System

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 USERS MANUAL, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085 microcomputer system can be built from just three chips—the 8085A CPU, a 8355 or 8755 ROM or PROM, and a 8155 or 8156 RAM/TIMER/I-O chip. The 8155/8156 provides, in addition to 2k bits of Static RAM, two programmable 8-bit I/O Ports, one programmable 6-bit I/O Port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH.)

The ZN427 Interface

This application note describes how up to 4, ZN427 ADCS can be connected to the I/O Ports of one 8155 RAM to provide 4 Analogue Input Channels to the microprocessor system. Since most 8085 based systems including the SDK-85 System Design Kit will incorporate one or more 8155s, then the addition of Analogue Input Channels would involve minimum additional hardware and design effort. An advantage of using the 8155 I/O Ports is that no additional address decoding or bus demultiplexing and buffering hardware is necessary.

For existing systems, if spare I O Ports are available then analogue inputs can easily be added without any major modifications to the hardware. Also the expansion of the number of input channels to a system by addition of extra 8155s should be easily implemented since this device is directly bus compatible with the 8085A.

The 8155 I O Ports are allocated as shown in the Logic Diagram, Fig. 1. Port A is programmed as INPUTS and provides an 8-bit data bus which connects to the three-state binary data outputs of each ZN427. Port B is programmed as OUTPUTS, the lower 4-bits provide the start convert and the upper 4-bits provide the Output Enable Signals to each ZN427. The END OF CONVERT output of each ZN427 is connected to a Port C pin, which are programmed as INPUTS to provide the individual BUSY FLAGS for each ZN427. Note that only 4- of the 6-bits available from Port C are used.

The ZN427 clock can be supplied either from an external source or from the 8085A CLOCK OUTPUT. Since the 8085A clock will normally be at 3 MHz, it will be necessary to divide this down by at least a factor of 4. This is achieved in the circuit, see Fig. 4, by means of a dual JK Flip Flop (7473) connected as a 2-bit binary counter. (Note: This will provide a clock frequency of 750 kHz which is a little higher than the ZN427 clock freqency spec. minimum of 600 kHz. However, for most practical applications the loss in accuracy due to this will be minimal.) An external clock could be used for the ZN427 but the advantage of using the microprocessor clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the microprocessor CLOCK CYCLES (or 'T' STATES).

(Note: To avoid confusion, future reference to 'clock' will mean the ZN427 clock signal unless specifically stated otherwise.)

The START CONVERT pulse is generated using a 'D' type Flip Flop ($\frac{1}{2}$ 7474) in order to meet the timing requirements discussed earlier. A conversion cycle is started by outputting a '0' followed by a '1' from the appropriate Port B output to the CLEAR input of the 'D' type which sets the SC input of the ZN427 to '0'. The first positive going clock edge after the CLEAR input is returned to a '1' clocks the 'D' type and sets the SC input to '1'. This sequence is illustrated in the Start Pulse Timing Diagram, Fig. 5.

On the 9th negative clock edge after the Start Pulse the END OF CONVERT output goes to a '1' signifying the end of the conversion process, this can be detected by an I/O read on Port C. However, when generating the ZN427 clock from the microprocessor clock as shown, the EOC output will always occur within 35 microprocessor clock cycles after the OUT instruction returning the SC input to a '1'. In this case it is not

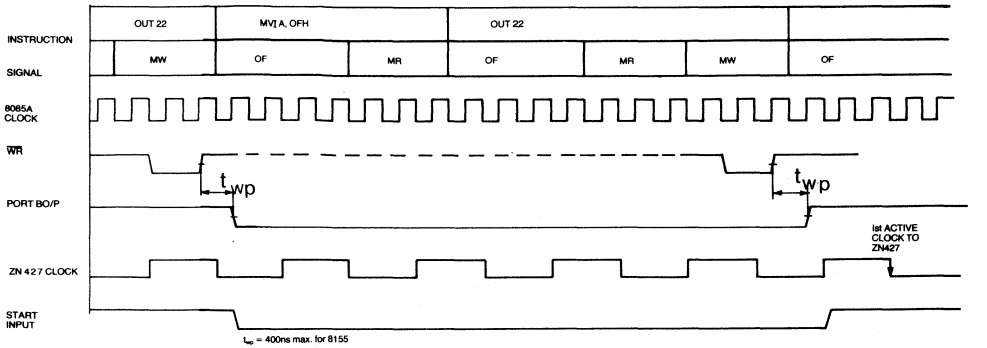


FIG. 5 START PULSE TIMING DIAGRAM

necessary to poll the EOC outputs, the ZN427 data outputs can be read after a suitable fixed delay in the programme. For application where processor time is at a premium or if immediate response is required to an EOC output, a microprocessor interrupt can be generated by connecting the EOC output direct to one of the 8085A restart inputs. The EOC outputs of to 4-ZN427s can be 'wire-OR'd' to produce a common interrupt line. Usually, however, the fast conversion time of the ZN427 (15 μs) will make it not worthwhile to employ microprocessor interrupts since the conversion time takes less than 6/7 typical microprocessor instructions.

The binary output data is applied via the converter data bus to Port A of the 8155 by driving the OE output to a '1' from the appropriate Port B bit. Obviously the programme should be arranged so that the outputs of only one ZN427 are enabled at any one time, in order to avoid bus contention problems. Note that in this application the Output Enable and Disable switching times (which are specified at 250 ns max.), need not be considered since they are much less than the instruction execution times.

The circuit diagram, Fig. 4 shows the ZN427s connected for a unipolar input range of 0 to + 10 V. Other ranges, e.g. + 5 V, ± 10 V, and ± 5 V can be readily obtained by using the appropriate resistors as shown in the ZN427 data sheet. Note also that the reference, $V_{REF\ IN}$, of up to five ZN427s may be driven from one internal reference. This useful feature saves power, discrete components, and gives excellent gain tracking between the converters.

In the circuit the negative supply to the ZN427s is through an 82K resistor from − 5 V. By suitable choice of resistor any negative supply of − 3 to − 30 volts may be used. For applications where only a positive 5 volt supply is available, a simple diode pump circuit suitable for up to 5-ZN427s is shown in the ZN427 data sheet.

Programme Example

A simple programme is given on page 9 together with the flow diagram in Fig. 6, which illustrates the ease of controlling and reading the ZN427 with the 8155 I/O Ports.

Following the flow diagram it is seen that after initialisation of the stack pointer the I/O Ports of the 8155 are defined—Ports A and C as INPUTS, Port B as OUTPUTS. A simultaneous START CONVERT pulse is sent to all the ADCs by outputting logic '0' folowed by logic '1' to the lower 4-bits of Port B. The EOC outputs of the ADCs are then read via Port C and tested for a logic '1/ to check if the conversion process has finished. The microprocessor will loop on this part of the programme until the EOC output of all the ADCs go to '1'. When this occurs the programme proceeds by enabling the outputs of each ADC in turn and reading the binary data via Port A. The ADC outputs are enabled in turn by outputting a logic '1' to each of the upper 4-bits of Port B (keeping the other 3-bits at '0' and the lower 4-bits at a '1'). The data from each ADC is stored in consecutive memory locations, starting at the address labelled 'DATA'. The H and L register pair hold the memory address at which data is to be saved; these are incremented for each read of an ADC.

This programme could easily be modified to act as a sub-routine for another main programme. As mentioned previously a fixed delay could be substituted for the programme loop which tests the EOC outputs. Also instead of generating a simultaneous START pulse separate START signals may be sent to each ADC at different times in a control cycle.

Summary

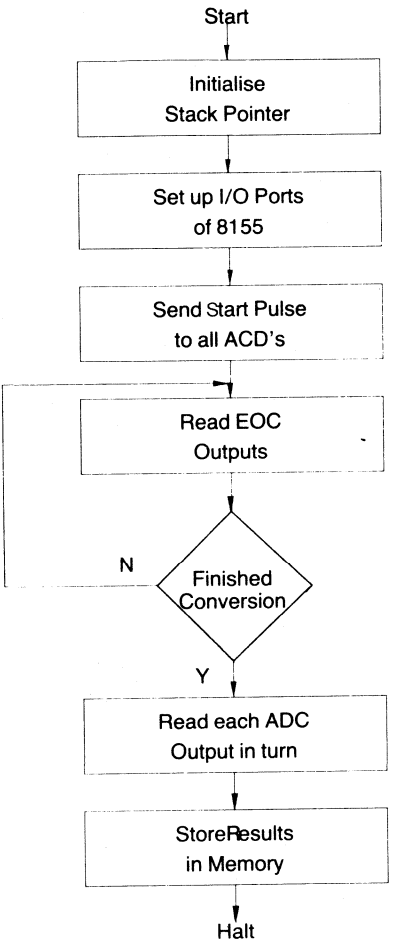
The system described in this report should be suitable for most applications since it allows complete control of each individual ADC. However, the configuration can easily by changed for particular requirements,—a few ideas are briefly described below.

1. If a simultaneous START pulse is adequate, then the START CONVERT inputs of the ZN427s can be commoned together and driven via one 'D' type from one Port output.
2. The EOC outputs of up to 4-ZN427s can be commoned and either taken to one Port input or used as a microprocessor interrupt signal.
3. Adoption of methods 1 and/or 2 above would use less 8155 Port bits and hence allow more ZN427s to be connected to each 8155.
4. Instead of generating the START pulse from the 8155 it could be asynchronously produced externally by a process timer, photo transistor or proximity detector circuit etc., the only timing requirement being that the pulse width fed to the CLEAR input of the 'D' type is at least half a clock period. (i.e. 640 ns with a 320 ns microprocessor clock) or 1.5 μs, whichever is smaller.
5. If D/A channels as well as A/D are required in one system then ZN428, 8-bit D/A Converters can be mixed on the same converter data bus as the ZN427. This will allow a designer to tailor a system to his specific A/D and D/A requirements. (See FERRANTI APPLICATION NOTE ANO11 for details of interfacing the ZN428 to the 8155.)

It is hoped that after reading this application note, the reader will have a much better insight into the operation and versatility of the ZN427, and into how it can easily be interfaced to a microprocessor system.

In order to avoid duplication only the relevant ZN427 characteristics were discussed in this report. For a full description and specification of the ZN427 please refer to the data sheet.

FIG. 6 PROGRAMME FLOW DIAGRAM



8155 PORT ALLOCATIONS

PORT A

PA0	Binary Data LSB
PA1	Binary Data LSB + 1
PA6	Binary Data MSB - 1
PA7	Binary Data MSB

PORT B

PB0	ADC1 SC Input
PB1	ADC2 SC Input
PB2	ADC3 SC Input
PB3	ADC4 SC Input
PB4	ADC1 OE Input
PB5	ADC2 OE Input
PB6	ADC3 OE Input
PB7	ADC4 OE Input

PORT C

PC0	ADC1 EOC Output
PC1	ADC2 EOC Output
PC2	ADC3 EOC Output
PC3	ADC4 EOC Output

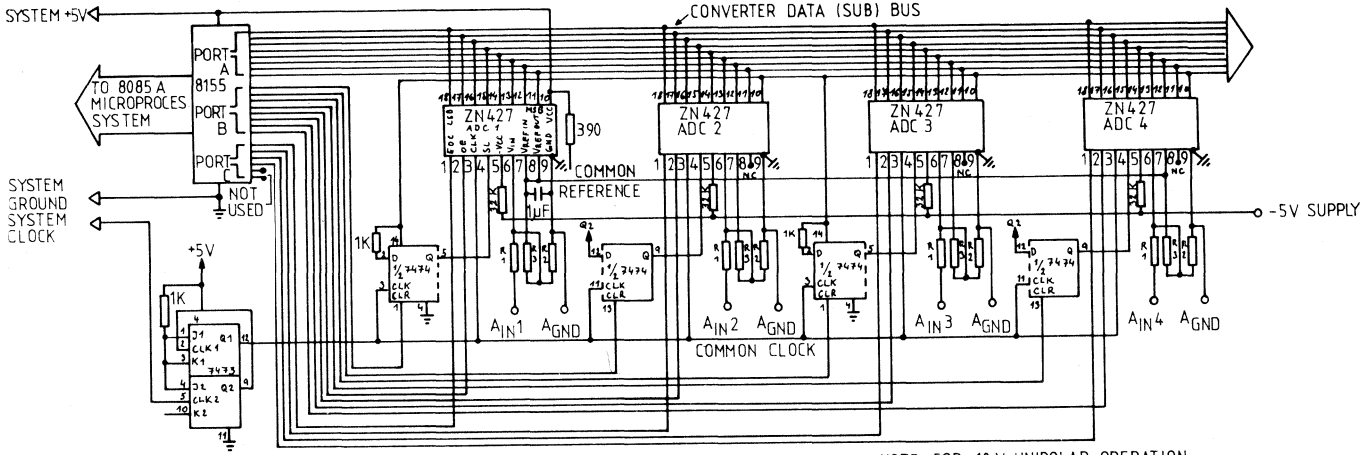
I/O PORT ADDRESSES

20	Command/Status Reg
21	RAM Port A
22	RAM Port B
23	RAM Port C

ZN427 – 8085A PROGRAMME EXAMPLE

```
LOC     OBJ       SOURCE STATEMENT
-------------------------------------------------------------------
2000    31C820            LXI SP, 20C8      Initialise Stack Pointer
2003    3E02              MVI A, 02H        Define I/O Ports
2005    D320              OUT 20
2007    3E00              MVI A, 00H
2009    D322              OUT 22            Send Start To All  ACD s
200B    3EOF              MVI A, OFH
200D    D322              OUT 22
200F    060F              MV1 B OFH
2011    DB23      LOOP:   IN 23             Read EOC s
2013    AO                ANA B             Strip Upper 4 Bits
2014    B8                CMP B             Test If All EOC s
2015    C21720            JNZ LOOP          Are A '1'
2018    213B20            LXI H, DATA
201B    3EIF              MVI A, 1FH
201D    D322              OUT 22            Enable ADC 1
201F    DB21              IN21              Read ADC 1
2021    77                MOV M, A          Save In Loc, DATA
2022    23                INX H             Increment Pointer
2023    3E2F              MVI A 2FH
2025    D322              OUT 22
2027    DB21              IN21              Read ADC 2
2029    77                MOV M, A          Save In LOC. DATA + 1
202A    23                INX H
202B    3E4F              MVI A 4FH
202D    D322              OUT 22
202F    DB21              IN 21             Read ADC 3
2031    77                MOV M,A           Save In Loc DATA + 2
2032    23                INX H
2033    3E8F              MVI A 8 FH
2035    D322              OUT 22
2037    DB 21             IN 21             Read ADC 4
2039    77                MOV M, A          Save In Loc. DATA + 4
203A    76                HLT

203B            DATA:
203C
203D
203E
```



NOTE: FOR 10 V UNIPOLAR OPERATION
R1 = 10 K POT + 11K IN SERIES
R2 = 5.K6
R3 = 1 MΩ POT + 680 K IN SERIES

Interfacing the ZN 428 D to A Converter with the 8085A Microprocessor System

by SCOTT BIRD, Ferranti Electronics Ltd.

The growth of the microprocessor has led to a demand for low cost, 8-bit A/D and D/A converters to interface between the real world of Analogue values and the Digital world of the microprocessor. This report values a simple, low cost, expandable multichannel D/A system based on the ZN428, 8-bit D/A converter interfaced directly to the I/O Ports of the 8155, 2K bit static RAM, which forms part of the basic 8085 microprocessor system.

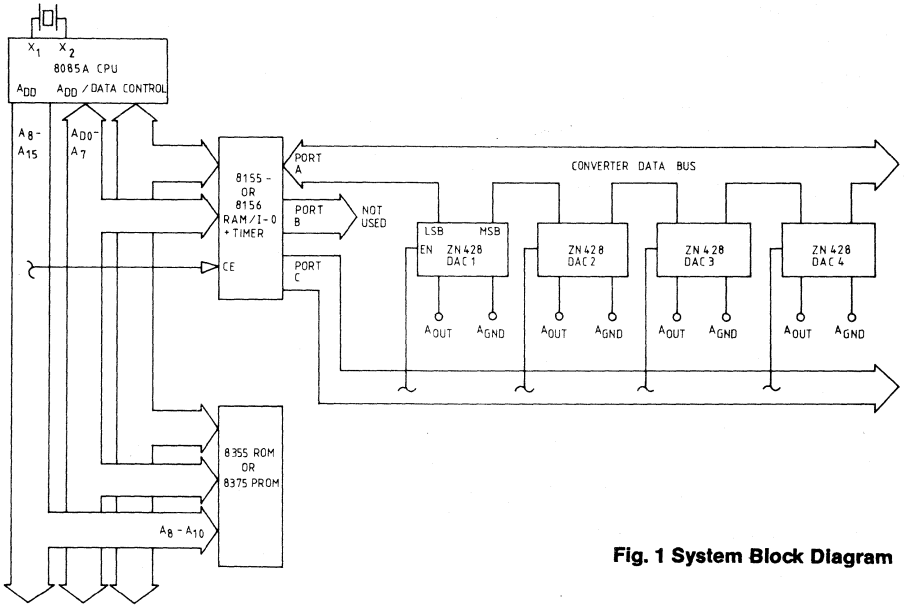


Fig. 1 System Block Diagram

The ZN428 D/A Converter

The ZN428 is a monolithic 8-bit D/A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{ENABLE}}$ is at logic '0' and the data is held when $\overline{\text{ENABLE}}$ is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800 ns setting time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

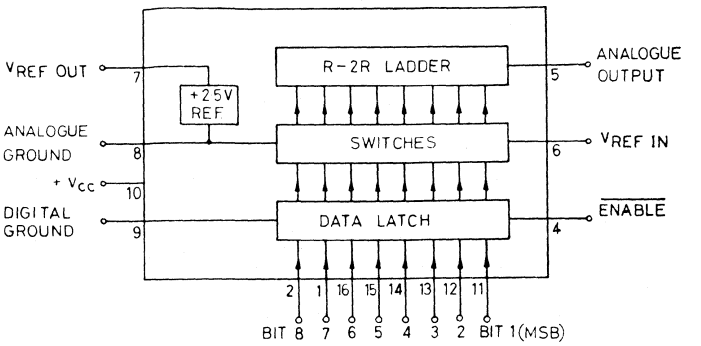


Fig. 2 ZN428 Logic Diagram

The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or V ref IN by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0 volt to $V_{REF\ IN}$ through a 4 kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 8085A Microprocessor System

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 USERS MANUAL; so only a brief description is given here.

The 8085A is a complete 8-bit, parallel central processing unit. A minimum component 8085A microcomputer system can be built from just three I.C.s—the 8085A CPU, an 8355 or 8755 ROM or PROM, and a 8155 or 8755 RAM/TIMER/I-O I.C. The 8155/8156 in addition to 2K Bits of Static RAM, provides two programmable 8-bit I/O Ports, one programmable 6-bit I/O Port and a programmable 14-bit binary timer counter. (The difference between the 8155 and 8156 is simply that on the 8155 the CHIP ENABLE is active LOW and on the 8156 it is active HIGH.)

The ZN428 Interface

This application report describes how one or more ZN428 DACs can be connected directly to the I/O Ports of an 8155 RAM to provide analogue output channels from the microprocessor system.

Since most 8085 based systems, including the SDK-85 System Design Kit, will incorporate one or more 8155s then the addition of Analogue output channels can be made with the minimum of extra hardware and design effort. An advantage of using the 8155 I/O Ports is that no additional address decoding or bus multiplexing and buffering hardware is necessary. For existing systems, if spare I/O Ports are available then analogue outputs can easily be added without major modifications to the hardware.

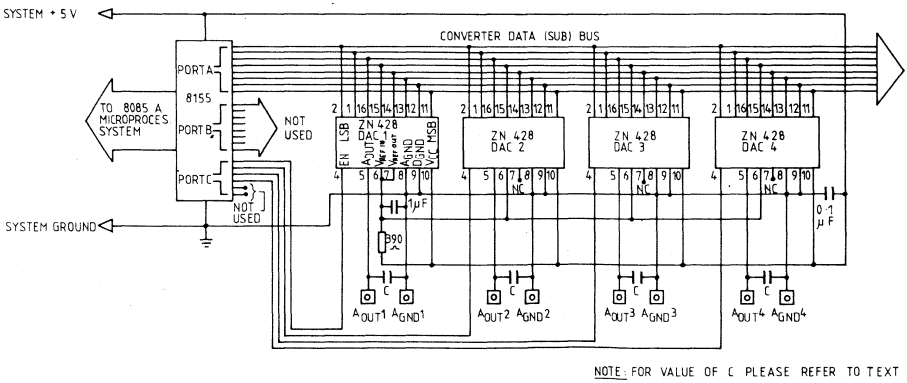
Also expanding the number of output channels by means of addition of extra 8155s should be easy to implement, since the 8155 is directly bus compatible with the 8085A. Figure 3 shows 4–ZN428s connected to the I/O Ports of one 8155. Port A is programmed as OUTPUTS and provides a common 8-bit data bus which is connected to the binary data inputs of each ZN428. The $\overline{\text{ENABLE}}$ inputs of each ZN428 are connected to separate pins on Port C which is also programmed as OUTPUTS. Note that in this configuration only 4 of the 6 Port C pins are used and Port B is also unused.

The reference voltage of all converters is provided by connecting the V_{REF} OUT pin of one ZN428 to the V_{REF} IN pins of all the ZN428s as shown. This useful feature saves power, components and gives excellent gain tracking between converters. Up to five ZN428s may be driven from one internal reference in this way.

The circuit, Fig. 3, shows the outputs of the ZN428s taken directly from pins 5 and 8. This will provide an output range of 0 volt to V_{REF} IN through a 4 kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any "glitches" which may be present. The value of this capacitor depends on the noise in the system and the response time required, however, for the minimum settling time it should not be greater that 100 pF. The output buffer amplifier was omitted from the ZN428 in order to allow greatest system speed, flexibility and lowest cost. Both Unipolar and Bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate Analogue and Digital ground pins. These can be connected together close to the I.C. pins. However, for noisy systems or environments it may be better to keep the Analogue ground pins for each individual ZN428 separate from the Digital ground, and to connect each Analogue ground to a single common earth point in the system, away from sources of digital noise such as clock oscillators, digital buses etc. The Analogue ground output line or terminals should also be taken direct to this common earth point. (Note: The maximum voltage between Analogue and Digital grounds is limited to 200 mV.)

Data is fed to a converter simply by outputting the binary data onto the common bus from Port A of the 8155. The appropriate output from Port C is then driven to a logic '0' level then back to a logic '1'. This will transfer the binary data on the bus into the input latches of the ZN428. The $\overline{\text{ENABLE}}$ inputs of converters which are not being updated are held at logic '1'. The data from Port A can now be changed and the next converter updated as and when required as determined by the controlling programme of the microprocessor. Note that in this application the Data Set-up and Data Hold times and Enable pulse widths need not be considered since they are much less than the microprocessor instruction execution times.



NOTE: FOR VALUE OF C PLEASE REFER TO TEXT

Programme Example

A simple programme is given on page 6 together with the flow diagram in Fig. 4, which illustrates the ease of controlling the ZN428 in conjunction with the 8155 I/O Ports.

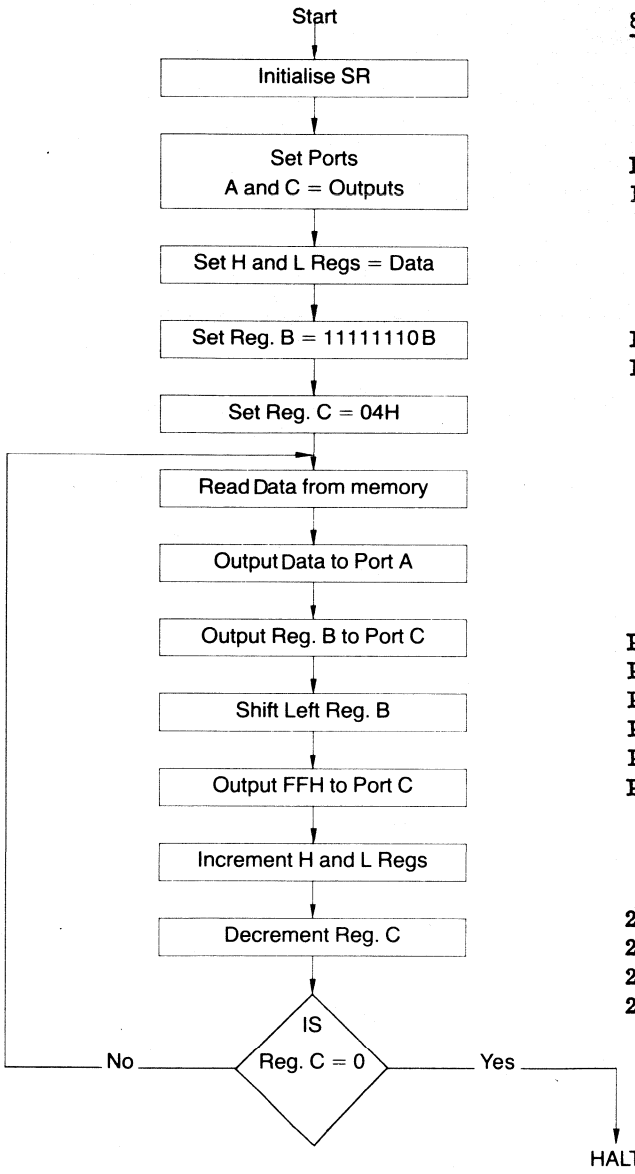
The object of the programme is to read the binary data from four successive memory locations and to output this data sequentially to each of the four DACs. In practice this programme would probably act as a sub-routine outputting data derived from some external source and operated on by the main programme.

With reference to the flow diagram Fig. 5 it is seen that after initialisation of the stack pointer the I/O Ports A and C are defined as OUTPUTS. The H and L register pair are loaded with the starting address in memory of where the data to be outputted is stored. Register B determines which DAC is to be enabled, this is set initially to 11 111 110; while Register C, which acts as a loop counter is set to 4. Data is then read from memory into the Accumulator using the H and L registers in the Register Indirect addressing mode. This data is outputted onto the converter data bus via Port A by sending the contents of the **Accumulator** directly to the 8155 with the 'OUT' instruction. DAC 1 is now enabled by transferring the contents of Register B to the Accumulator and outputting this via Port C. The Accumulator contents are rotated one bit left before being transferred back to Register B, ready to enable the next DAC. Next $\overline{\text{ENABLE}}$ is removed by outputting all 1's via Port C, H and L are incremented to address the next data byte and Register C is decremented and tested for zero. In this case Register C will contain 03 and the programme will branch back to the address labelled 'LOOP' via a conditional jump instruction, and the next data byte will be read into the Accumulator. Since Register B was shifted one bit left the new data will be loaded into DAC 2 on this cycle of the loop. The programme cycles round the loop 4 times, reading the data from memory and outputting it to each DAC in turn until Register C is decremented to zero, at which point the programme halts.

ZN428 – 8085A PROGRAMME EXAMPLE

LOC	OBJ	SOURCE STATEMENT	COMMENT
2000	31C820	LXI SP, 20C8	Initialise SP
2003	3E0D	MVI A, 0D	Define I/O Ports
2005	D320	OUT 20	
2007	212020	LXI H, DATA	Set H & L = Data
200A	06FE	MVI B, FEH	
200C	0E04	MVI C, 04H	
200E	7E	LOOP: MOV A,M	Read Data
200F	D321	OUT 21	Put Data on Bus
2011	78	MOV A,B	
2012	D323	OUT 23	Set $\overline{\text{Enable}}$ low
2014	07	RLC	Rotate left for next DAC
2015	47	MOV B,A	
2016	3EFF	MVI A, FF	Set $\overline{\text{Enable}}$ high
2018	D323	OUT 23	
201A	23	INX H	
201B	0D	DCR C	
201C	C2 0E 20	JNZ Loop	Jump IF C = 0
201F	76	HLT	
2020	-	DATA :	
2021			
2022			
2023			

FIG. 4 PROGRAMME FLOW DIAGRAM



8155 PORT ALLOCATIONS

PORT A

PA0	Binary Data LSB
PA1	Binary Data LSB + 1
PA6	Binary Data MSB - 1
PA7	Binary Data MSB

PORT B

NOT USED

PORT C

PC0	DAC1 $\overline{\text{Enable}}$ Input
PC1	DAC2 $\overline{\text{Enable}}$ Input
PC2	DAC3 $\overline{\text{Enable}}$ Input
PC3	DAC4 $\overline{\text{Enable}}$ Input
PC4	Not Used
PC5	Not Used

I/O PORT ADDRESSES

20	Command/Status Reg
21	RAM Port A
22	RAM Port B
23	RAM Port C

Summary

The system described in this report should be satisfactory for most applications, however, this configuration is by no means rigid, but is only intended as one example to demonstrate how easily the ZN428 can be used with the 8085A microprocessor system. A few ideas and notes are briefly described below, and it is hoped that these will help the Design Engineer to produce the most efficient system for his particular requirements.

1. The 8155 I/O Ports can be allocated as dictated by system requirements and availability. In the example all of Port A and four of the six Port C I/O pins are used. Port B could have been used equally as well either for the converter data bus or to provide the $\overline{\text{ENABLE}}$ signals.
2. If I/O Port pins are limited and only one DAC needs to be enabled at any one time, then a Decoder I.C. (i.e. 8205, 1 out of 8 binary decoder) can be used to drive the $\overline{\text{ENABLE}}$ inputs. For Example 4 I/O Port pins, 3 for the address code and 1 for the decoder enable would drive 8 DAC ENABLE inputs.
3. In order to update 2 DACs simultaneously but with different data, then the binary inputs of one (or more) DACs could be connected to Port A and the other DAC to Port B. The relevant data could then be outputted on Ports A and B and then the $\overline{\text{ENABLE}}$ inputs of both DACs driven to logic '0' together, either by commoning the two inputs to one Port C pin or by using separate I/O pins from Port C but programming both bits to go low together.
4. The number of ZN428s which can be connected to a common data bus is limited only by the bus capacitance and the drive capability of the 8155 I/O Ports. Note the low inputs currents of the ZN428–
   $I_{IH} = 20\ \mu A$ at 2.4 V, $I_{IL} = -5\ \mu A$ at 400 mV.
5. When the ZN428 $\overline{\text{ENABLE}}$ input is held at logic '0' the input latches are held open and the data is transferred directly to the ladder switches. Therefore, if repeatedly updating only one DAC the $\overline{\text{ENABLE}}$ input can be held at logic '0' instead of returning to logic '1' after each update.
6. If A/D channels as well as D/A are required in one system, then ZN427, 8-bit A/D Converters can be mixed on the same converter data bus as the ZN428. This will allow the design engineer to tailor a system to his specific A/D and D/A requirements. (See FERRANTI APPLICATION NOTE AN 010/OSB for details of interfacing the ZN427 to the 8155.)

It is hoped that after reading this application note the reader will have a much better insight into the operation and versatility of the ZN428, and into how it can easily be interfaced to a microprocessor system. In order to avoid duplication only the relevant characteristics of the ZN428 were discussed in this report. For a full description and specification of the ZN428 please refer to the data sheet.

Direct Bus Interfacing Using The ZN427/ZN428 Data Converters

INTRODUCTION

The rapid growth of the microprocessor coupled with its diminishing cost has opened up many potentially new applications in the measurement, control and data acquisition fields of the electronics industry. This growth has, however, been so fast that a vacuum has been created in the data conversion market for low cost, microprocessor compatible converters which can interface the digital microprocessor with the real analogue world. Without some form of interface to the outside world a microprocessor is simply a non-entity. No matter how powerful and fast the microprocessor itself is, if it cannot communicate efficiently with the world around it then its usefulness is limited and its power wasted. It is to meet this requirement that two fast, low-cost, microprocessor compatible data converters have been introduced by Ferranti Electronics Ltd. This application note introduces these two converters and describes how they can easily be interfaced directly to most of the popular types of microprocessor with particular reference to the 6800 and 8085A.

THE ZN427 A to D CONVERTER

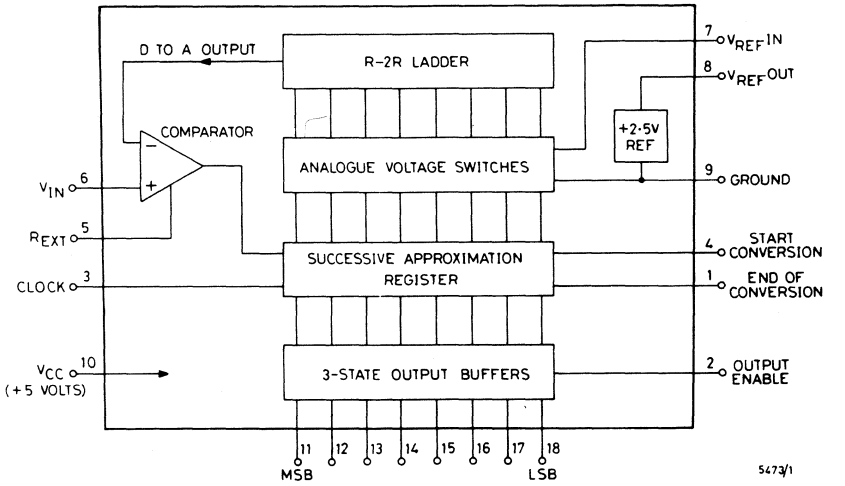


Fig. 1. ZN427 LOGIC DIAGRAM

The ZN427 is an 8-bit successive approximation A to D converter (ADC).

It features 3-state output buffers to permit bussing on to common data lines, fast 15 μs conversion time and no missing codes over its full operating temperature range. The ZN427 contains a voltage switching D to A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5 volt precision band-gap reference.

The use of the on chip reference is pin optional to retain flexibility, an external fixed or varying reference for ratiometric operation may, therefore, be substituted. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a resistor from the R_{EXT} pin 5 to the negative supply rail.

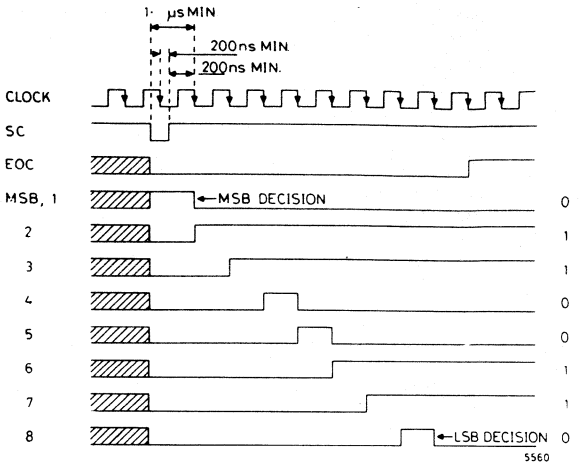


Fig. 2. ZN427 TIMING DIAGRAM

The conversion cycle is initiated by a negative going pulse applied to the START CONVERSION (SC) input, this sets the END OF CONVERSION (EOC) output to a logic '0' indicating that the converter is busy, see Fig. 2. On the ninth negative clock edge after the start pulse the EOC output goes back to a logic '1' signalling that the cycle is complete. The binary output data is latched until the next start pulse. The three-state data outputs are switched OFF (high impedance state) when the OUTPUT ENABLE (OE) input is at a logic '0' .and they are enabled when the OE input is taken to a logic '1'.

THE ZN428 D to A CONVERTER

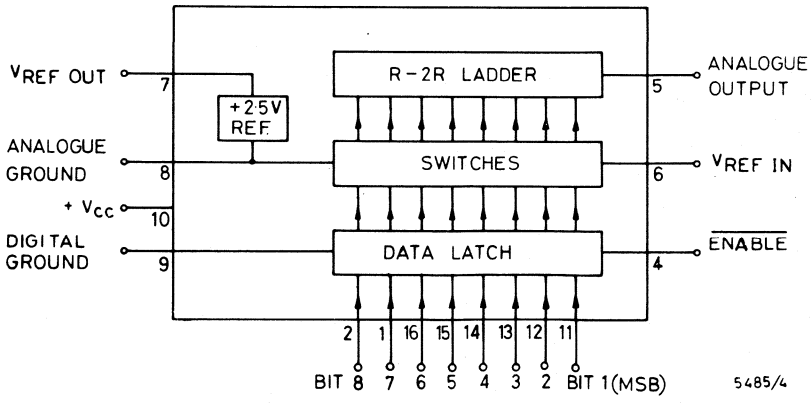


Fig. 3. ZN428 LOGIC DIAGRAM

The ZN428 is a monolithic 8-bit D to A converter (DAC), with input latches to facilitate updating from a microprocessor data bus. The latch is transparent when the ENABLE ($\overline{EN}$) input is at a logic '0' and the data is held when $\overline{EN}$ is taken to a logic '1'.

The ZN428 features single +5V supply requirements, fast 800 ns settling time and is guaranteed monotonic over its full temperature range. It contains a pin optional 2.5V precision band-gap reference identical to the ZN427. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor logic switches especially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network, the nominal range being $0 - V_{REF\ IN}$ volts with a 4 kΩ resistance. Other output ranges can readily be obtained by the use of an external amplifier allowing complete versatility in its application.

THE ZN427 MICROPROCESSOR BUS INTERFACE

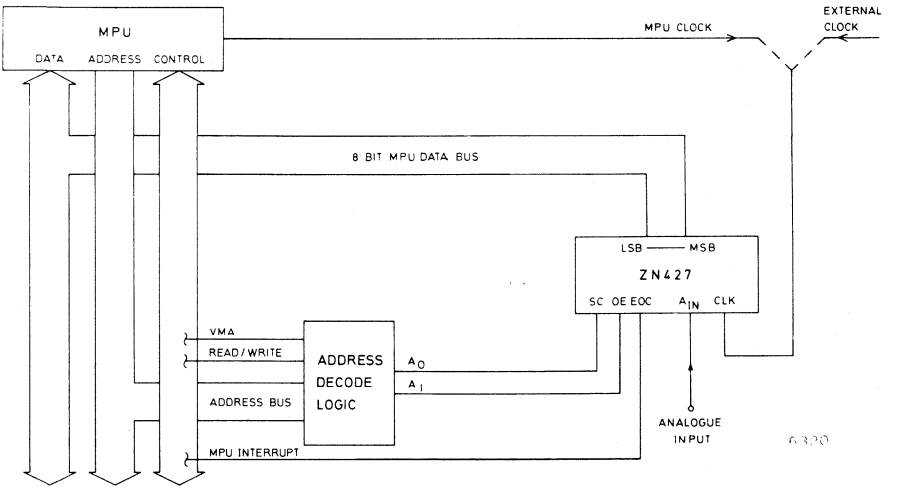


Fig. 4.

Peripheral devices can be connected to a microprocessor system by two basic methods. The first and usually the simplest from the point of view of design effort required is to use a Peripheral Interface I/O device usually found as a support IC in most of the MPU families. With this method the peripheral device is simply connected to the I/O lines of the Peripheral Interface device and generally no considerations have to be made in terms of bus buffering, bus timing or address decoding.

The second method is to connect the peripheral device directly to the microprocessor data bus. This method is termed "Memory Mapped I/O" which as its name implies is to make each peripheral I/O function appear to the MPU as a normal memory location, in which case the MPU cannot tell whether it is addressing memory or I/O. This allows the full set of memory reference instructions to be used for I/O data transfer, but it does imply that the peripheral device must be capable of responding at least as fast as the MPU memory and hence it should be compatible with the bus timing characteristics. The disadvantages of Memory Mapped I/O are that it usually requires additional address decoding logic, and also, since the I/O device will be addressed as memory, then there will consequently be fewer addresses available for actual memory.

It is with this second method of interfacing that this Application Note is primarily concerned. The Peripheral Interface I/O method of interfacing the ZN427 and ZN428 is covered in Application Notes AN010 – AN012.

A variation of Memory Mapped I/O, sometimes known as "I/O Mapped I/O" is available on some MPUs which overcomes the last disadvantage referred to. This allows a defined range of memory address also to be used for I/O by means of separate I/O instructions. A special control line is required to inform the memory and I/O device whether the address of the current READ or WRITE cycle refers to memory or to I/O. This technique however does restrict the freedom of the programmer to the use of these I/O instructions which normally only operate on data in the microprocessor accumulator.

Figure 4 shows the basic Memory Mapped interface for the ZN427 where the 8 binary outputs of the ADC are connected directly to the MPU data bus. The control inputs, START CONVERSION and OUTPUT ENABLE are shown driven from address decoder logic, the function of which is to drive the appropriate input when the address which has been allocated to that particular input is present on the address bus and the control bus signals indicate a valid memory read or write operation. Note that the level of address decode logic used must ensure that the three-state data outputs of the ZN427 are disabled at all times except when the actual ADC data is required on the data bus, otherwise bus contention problems may occur with other devices using the bus. The END OF CONVERSION output can be connected directly to an MPU interrupt input to signal the completion of the conversion cycle by the ADC. The ZN427 clock can be derived either from the MPU clock or from an external source. If however the former method is employed, it may simplify the design of the interface with regard to the timing criteria of the SC input. (This is covered in more detail later in this report).

THE ZN428 MICROPROCESSOR BUS INTERFACE

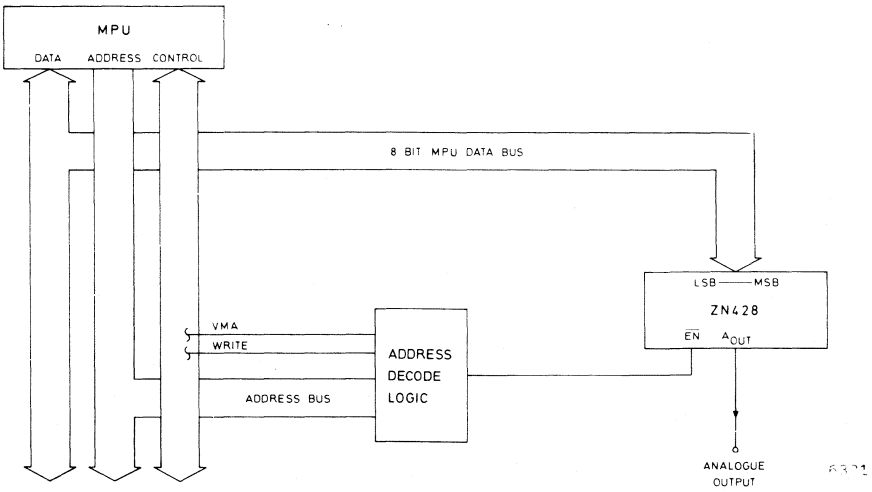


Fig. 5.

The ZN428 data inputs can be directly connected to an MPU data bus when used in the Memory Mapped configuration, this is illustrated in Fig. 5. For this application the address decode logic has only to generate the NOT ENABLE signal for the DAC. This is accomplished by gating the MPU

WRITE signal with the decoded address signal in order that when a memory write instruction to the DAC address location is executed, then a negative going pulse is applied to the $\overline{EN}$ input which will transfer the binary code from the data bus to the ZN428 input latches.

INTERFACING TO THE 6800 BUS

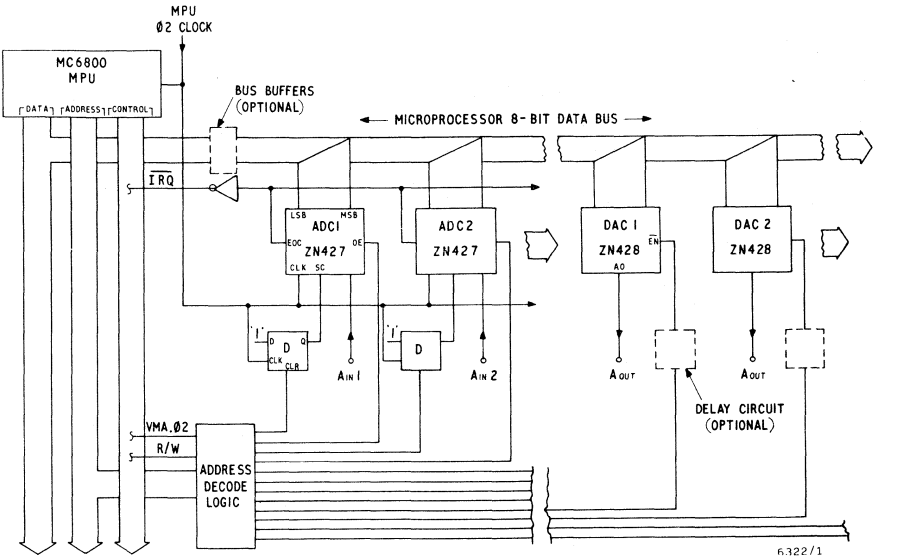


Fig. 6. ZN427/ZN428 TO 6800 BUS INTERFACE

With the ability of the ZN427 and ZN428 to be bus compatible it is possible to produce a complete Analogue I/O system, specifically configured to the designer's own requirements with the converters connected directly to the MPU data bus. Such a system is illustrated in figure 6 built around a 6800 MPU.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL logic the 6800 requires only a single +5 volt power supply, it features a set of 72 instructions with 7 addressing modes and full 65K byte memory addressing capability. The microprocessor communicates with its external memory and all I/O peripherals over an 8-bit bi-directional data bus and a 16-bit address bus. (Full data on the 6800 microprocessor is readily available from its manufacturers and their distributors).

The number of ZN427s and ZN428s which can be hung on the data bus is not limited, the only restrictions being the total load presented to the data bus and the number of decoded address lines available. The loading and drive characteristics of the converters are summarised in Table 1. Optional bi-directional bus buffers are shown in the diagram, these can be used to expand the system. Use of these will be dependent on the total number of converters used, other peripheral and memory devices on the data bus, and other loading factors such as the physical length of bus required.

ZN427		ZN428	
Parameter	Specification	Parameter	Specification
I_{IL}	–5 μA max.	I_{IL}	–5 μA max.
I_{IH}	15 μA max.	I_{IH}	20 μA max.
I_{IH} (Clock)	30 μA max.		
I_{OL}	1.6 mA min.		
I_{OH}	–100 μA min.		
I_{OHX} (Off state leakage)	2 μA max.		

(NOTE: Currents specified at 0.4V and 2.4V).

TABLE 1. LOADING CHARACTERISTICS OF THE ZN427 and ZN428

The level of address decoding will depend on the overall MPU system design. This can range from merely using the upper address lines directly with no hardware decoding to provide the control lines for the converters – which rapidly depletes the number of address locations available for memory, through to full address decoding where all 65K addresses can be utilised. The address decode hardware can usually be produced from a few TTL gates in association with an Address Decoder I/C such as the ZN74154. In order to avoid addressing problems it is necessary on the 6800 to qualify the decoded address with the Valid Memory Address (VMA) and ∅2 clock signals. The READ/WRITE control line can also be utilised to permit a single decoded address to control each ZN427, i.e. a WRITE instruction to the specific address would generate the SC signal and a READ instruction of the same address would enable the converter outputs and read the data. The function of the 'D' type flip flops shown in the diagram is to ensure that the timing criteria of the SC pulse are met. The requirements for this are that the SC pulse should start at least 1.5 μs before the first active (negative going) clock edge after the SC pulse, and that the trailing edge of the SC pulse must not occur within ±200 ns of a negative going clock edge, see figure 2. By careful design of the address decode logic when deriving the converter clock from the MPU it is possible to produce the correct timing for the SC pulse and to dispense with the 'D' type flip-flops.

The other advantage of using the MPU clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of MPU machine cycles. Again with reference to figure 2 it can be seen that the conversion cycle always takes less than 10 clock cycles after the end of the SC pulse. Hence instead of using the EOC output to drive the MPU $\overline{IRQ}$ input a simple programme delay loop can be substituted. Note that the EOC outputs of up to five ZN427s can be 'wire-anded' together to form a common interrupt line.

The clock frequency of the standard 6800 is 1 MHz which can be used directly to drive the ZN427s if a small loss of accuracy can be tolerated. The 6871B MPU clock generator is produced in a version with a 614.4 kHz clock signal. This is only marginally higher than the specified ZN427 clock rate of 600 kHz and the $\varnothing 2$ TTL output of this can be used directly for the converter clock if full accuracy is essential.

With the 6800 it may be necessary to delay the decoded address enable signal to the ZN428 converters if glitch free operation is desired. This is due to the fact that during a write operation on the 6800 the address and address qualifying control signals become valid before the data bus signals are valid, thereby enabling the DAC before the data is established on the data bus.

The Analogue output can be taken directly from the ZN428 output pin which provides a nominal output range from zero volts to $V_{REF\ IN}$ with a 4kΩ output resistance. For most applications higher output ranges or drive will be required. This can easily be accomplished on the ZN428 by the addition of an external buffer amplifier which can be chosen for the specific characteristics required. The ZN428 is provided with separate Analogue and Digital ground pins which should normally be connected together close to the I.C. For noisy systems or environments an improvement may be obtained, in some cases, by running the two ground pins to supply ground separately, taking the Analogue ground of each ZN428 to a single common earth point in the system away from the sources of high noise such as clock oscillators, digital buses, etc. Note that the maximum voltage between the Analogue and Digital ground pins should not be allowed to exceed 200 mV.

Both the ZN427 and ZN428 contain a nominal 2.5V internal band-gap voltage reference. Use of this on-chip reference is pin optional to retain flexibility and an external reference can be substituted which allows ratiometric operation over the range of typically 1.5 to 3V. The on-chip reference is capable of supplying the reference voltage for up to five ZN427s and ZN428s. This useful feature saves power, discrete components and gives excellent gain tracking between the converters in a system. The tail current for the comparator on the ZN427 is derived via an external resistor from a negative supply. By suitable choice of resistor any negative supply of between –3 and –30 volts may be used. Since the negative current is only of the order of 65microamps per converter then for applications where only a positive supply is available a simple diode pump circuit can be used.

With a memory mapped interface the full range of memory reference instructions are available to the programmer in order to control the converters, and programming becomes a relatively simple matter of reading and writing data to the addresses allocated to the converters. For example, for the ADCs a conversion cycle could be initiated by a store accumulator command (STA A) to address location ALOC 1, where ALOC 1 is the address of the ADC to be accessed. The contents of the MPU accumulator 'A' at this time are irrelevant since we only want to generate a memory write cycle to produce a pulse at the SC input. Now one can either enable the MPU interrupt and wait for the EOC output to generate an interrupt request signal if this is the method used or alternatively a simple programme delay loop can be entered to produce a delay of $\geqslant 9$ converter clock cycles (i.e. $\geqslant 15\ \mu s$ if a 600 kHz clock is used). Upon receipt of an interrupt or completion of the delay a load accumulator command (LDA A) can be performed on address ALOC 1. This will read the binary data from the converter into the MPU accumulator 'A'. It is even simpler to programme the DACs. All one needs to do is to load the value to be outputted to say accumulator 'A' in binary format. A store accumulator command (STA A) is then programmed to address location ALOC 2, where ALOC 2 is the address allocated to the DAC. Upon execution of this the data will be transferred from the accumulator via the data bus to the DAC input latches, and be present at the DAC output in analogue form within 1.25 microseconds of the enable pulse.

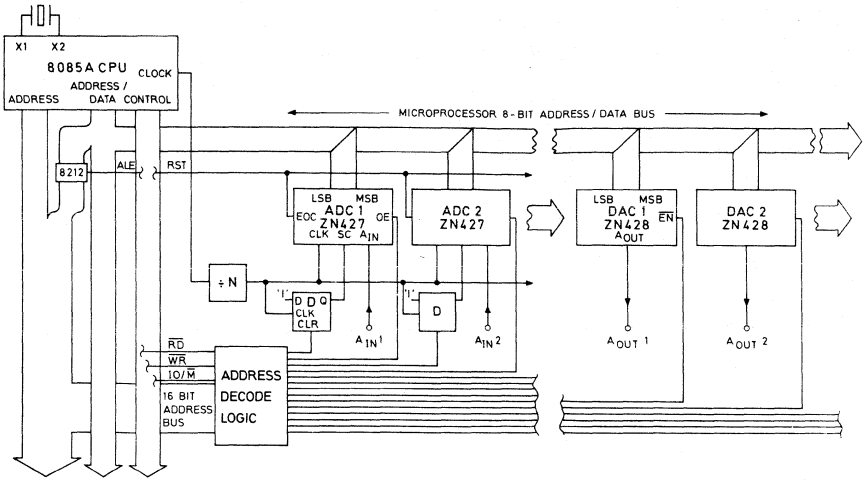


Fig. 7. ZN427/ZN428 TO 8085 BUS INTERFACE

An analogue I/O system for the 8085A microprocessor is shown in figure 7. This is similar to the 6800 system but the following exceptions should be noted.

The 8085A is another popular 8-bit microprocessor. However, unlike the 6800 this MPU uses a multiplexed data bus whereby the lower 8 address bits A0-A7 are time shared with the 8 data bits. The address bus contains the upper 8 bits A8-A15. If the lower 8 address bits are to be used for address decoding then it is preferable to de-multiplex the bus using an 8 bit latch, such as the 8212, strobed with the Address Latch Enable (ALE) signal from the MPU. The 8085A offers either Memory Mapped I/O or I/O Mapped I/O by means of a separate control line (IO/$\overline{M}$). This allows use of the 'IN' and 'OUT' instructions to control I/O data transfers and the retention of the full 65K memory locations. If using this method then it is unnecessary to de-multiplex the Address/Data Bus, since only the lower 256 addresses are used for I/O transfers, and the address in the lower 8 bits is mirrored into the upper 8 address bits during this operation.

The standard 8085A clock frequency is 3 MHz. Hence it is necessary to divide the output from the 8085A CLK output pin down by a factor of at least 4 to produce an acceptable ZN427 clock. Because of this it is more difficult to synchronise the decoded address signals with the ZN427 clock in order to meet the start pulse timing criteria, and one will usually have to incorporate the 'D' type flip-flops as indicated to generate the SC pulse.

Note that with the 8085A the common EOC line can be used directly to generate an interrupt via one of the 3 Restart Interrupt inputs. The decoded address input to the ZN428s $\overline{EN}$ input can also be used without any additional delay since, with this MPU the bus data is valid during the time that the WRITE signal is established.

Again programming is very straightforward. With a Memory Mapped I/O configuration the Data Transfer commands – Move (MOV), Load (LDA), and Store (STA) can be used to control data transfers between the converters and the MPU. If an I/O Mapped I/O configuration is adapted then the input (IN) and Output (OUT) commands are used to transfer data between the MPU accumulator and the converters.

SUMMARY

The Analogue I/O systems described in this report are intended only as a guide to illustrate to design engineers the ease and versatility with which these two converters can be used to produce analogue I/O channels for popular 8-bit microprocessors. As a result of the low cost, low external component count and flexibility of these converters, designs based on the 'one converter per channel concept' will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessary usage of traditional data acquisition methods involving a single high cost hybrid ADC utilising sample and hold and multichannel multiplexing techniques.

Microprocessor Interfacing Using The ZN432 10-Bit Data Converter

INTRODUCTION

The use of Microprocessors in the fields of Process Control, Automotive applications, Industrial Data Acquisition and Logging and Domestic Consumer Products is becoming increasingly widespread. Indeed the fall in the price of the microprocessor itself is creating new applications in fields previously uneconomical to develop, and whilst the price of the microprocessor has fallen dramatically over the past two or three years the fall in the price of compatible Data Conversion products has not been so sharp. This is partially due to the fact that most Data Conversion products cannot be produced by using a single semiconductor process (as can microprocessors), but have to be manufactured in hybrid form using different processes for the digital and linear elements plus thin film technology and laser trimming for the precision resistor networks. Currently one may purchase a Microprocessor Integrated Circuit for only a few pounds whilst a microprocessor compatible Data Acquisition module may well cost in the region of £200. This module will of course probably provide 16 channels at 12 bit accuracy, but not every user wants all these channels or accuracy and though lower cost Converter I.C's are available the system manufacturer may well be disinclined to spend the time and manpower in designing a converter interface for his microprocessor system due to the complexities with which he fears he may be faced.

This Application Note describes a monolithic 10 bit accurate Analogue to Digital (A/D) Converter integrated circuit and explains the different techniques of interfacing this to common 8-bit microprocessors using the minimum of external discrete components and standard TTL logic elements.

THE ZN432 A/D CONVERTER

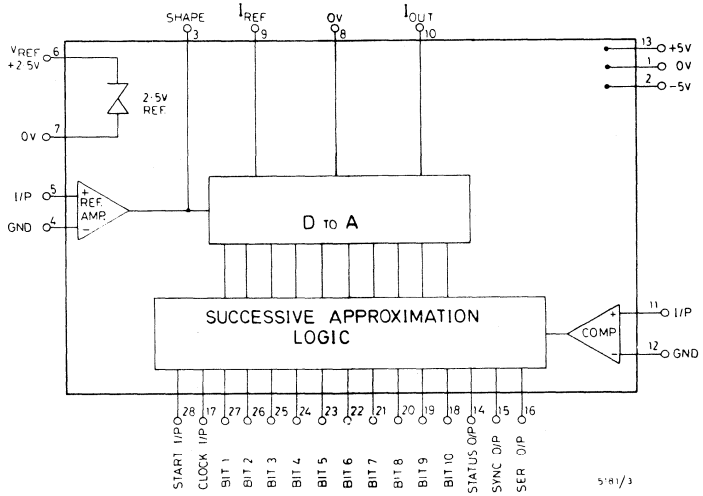


Fig. 1. ZN432 LOGIC DIAGRAM

The ZN432 is a 10-bit Analogue to Digital Converter produced in monolithic form by a silicon bipolar process. The converter is of the Successive Approximation type and includes an on-chip precision reference, reference amplifier, comparator, successive approximation logic and a D to A Converter. The D to A converter operates on the unit current source principle with a current switching

array using a matrix of diffused resistors. As a result of incorporating several design and layout innovations and the use of highly developed processing and photomask techniques, 10-bit accuracy is obtained without the need for post diffusion trimming operations. Only a few external components are required, including two capacitors, to shape the internal reference and reference amplifier outputs, and several resistors which define the input voltage range of the converter, which can be either unipolar or bipolar over whichever range is required by selecting suitable external resistors. The ZN432 is available in 3 temperature ranges, including full military temperature range, and in either 8 9 or full 10-bit accurate versions, packaged in a 28 lead hermetically sealed ceramic D.I.L. encapsulation.

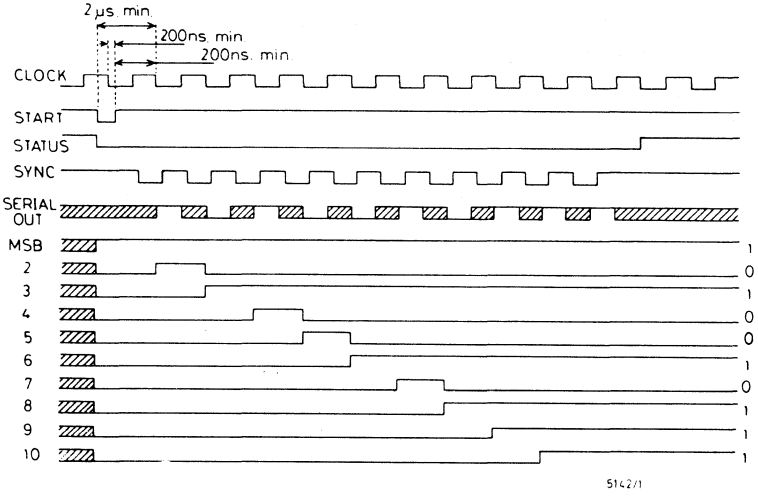


Fig. 2. TIMING DIAGRAM

The operation of the converter can best be described by reference to the timing diagram, Fig. 2. Conversion is initiated by a negative going START pulse which sets the MSB to a logic '1' and all other bits to a logic '0'. The STATUS output is also set to a logic '0' at this time indicating that the converter is busy. The leading edge of the START pulse should occur at least 2 μs before the 1st active negative going edge of the clock and the trailing edge of the START pulse must not occur within ±200 ns of a negative going clock edge. On the next negative going clock edge a decision is made on whether to set the MSB back to a logic '0' if the input current is less than the D to A output or, if not, it is left at a logic '1'. Bit 2 is switched to a logic '1' on the same clock edge and on the next negative edge a decision is made about Bit 2, again by comparing the input current with the internal D to A output. This process is repeated for all 10 bits so that when the STATUS output goes to a logic '1' on the 11th negative clock the digital output from the converter is a valid representation of V_{in}. A SERIAL DATA output is also provided on the ZN432, this data is outputted during the conversion cycle and is valid on the positive going edge of the pulses on the SYNCH output.

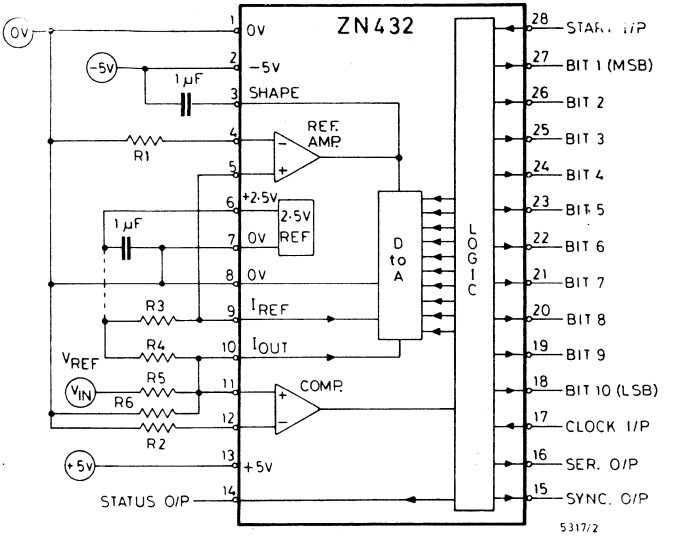


Fig. 3. TYPICAL EXTERNAL COMPONENTS

A diagram showing typical external components for the ZN432 is shown in Figure 3. The capacitor on pin 3 is used to stabilise the reference loop whilst that on pin 6 is for stabilisation and decoupling of the voltage reference output. Resistors R1 and R2 control the bias current of the reference amplifier and comparator, R3 defines the D to A reference current, R4 and R5 set the input voltage range and R6 is selected to obtain a suitable D to A time constant. For setting up, R3 will adjust the converter gain and R4 the offset. As an example, the resistor values for a ± 10 volt input range are:

R1 = 5 kΩ
R2 = 1.25 kΩ
R3 = 5 kΩ
R4 = 2.5 kΩ
R5 = 10 kΩ
R6 = 3.33 kΩ

Resistors R3, R4 and R5 affect gain and offset and hence high stability types should be used whereas the nearest preferred values may be chosen for R1, R2 and R6. Refer to the ZN432 Series Data Sheet for more information on the selection of external components.

INTERFACING DATA CONVERTERS TO MICROPROCESSORS

Peripheral devices can be interfaced to microprocessor systems by two basic methods. The first and simplest is to use a general purpose I/O device, (also known as Peripheral Interface Adapters, Versatile Interface Adaptors or Programmable Peripheral Interfaces, etc.). Most microprocessor systems on the market usually include one or more of these components in their Microprocessor Systems Family. They normally consist of one or more data ports, usually of 8 bits which can be programmed to function either as inputs or outputs. With some devices the complete port has to be programmed to function either as all Inputs or all Outputs, but the more useful I/O devices allow the individual pins of each data port to be programmed separately as Inputs or Outputs. In addition most devices also feature several control lines for the purposes of generating handshake signals with peripherals and generating microprocessor interrupts etc.

The second interface method is to connect the peripheral device directly to the microprocessor Data Bus. This method is termed Memory Mapped I/O which as its name implies, is to make each peripheral I/O function appear to the microprocessor as a normal memory location. This allows the full set of memory reference instructions to be used for I/O data transfer, but also implies that the peripheral device must be capable of responding at least as fast as memory, and hence it should be compatible with the MPU bus timing characteristics. With 10-bit converters a problem exists when using this method in that the 8-bit data bus is not wide enough to handle the converter data as a single word. It is therefore necessary to split the data into two words usually of 8 and 2 bits which are fed to the data bus in two separate bytes by means of appropriate gating on the converter outputs. Naturally when using a 16-bit microprocessor this problem does not arise, as converter data can then be read as a single word on the data bus. The disadvantages of Memory Mapped I/O are that it usually requires additional address decoding logic and also, since the I/O will be addressed as memory, there will consequently be fewer addresses available for actual memory. A variation of Memory Mapped I/O commonly referred to as I/O Mapped I/O or Isolated I/O is available on some microprocessors which overcomes this last disadvantage. This allows a defined range of memory addresses to be used also for I/O by means of separate Input and Output instructions. A special control output is used to tell the memory I/O devices whether the address of the current Read to Write cycle refers to memory or to I/O. This technique, does, however, restrict the freedom of the programmer to the use of these Input/Output instructions which usually operate only on data in the microprocessor accumulator.

So far we have dealt with interfacing to the ZN432 using the parallel binary outputs, alternatively the Serial Output can be used in applications which demand that the number of lines to the converter need to be kept to a minimum. Two schemes are briefly described here although other variations are possible. The first would be to connect the Serial Output to one I/O pin of an I/O device and to use the Status Output to generate microprocessor interrupts via one of the I/O device control inputs, thereby reading the serial data from the I/O device on the positive going edge of each pulse on the Status Output. The other method is to use a microprocessor with a direct Serial input part such as the 8085A. This would either involve synchronising the converter clock to a sub-multiple of the microprocessor clock and programming the microprocessor to read the data at the correct time, or by again using the Status Output to generate an interrupt. Unfortunately both these methods restrict the maximum converter clock period to a minimum of at least several instruction execution times i.e. the time needed to interrupt the microprocessor, read the data and store it in memory. Another option open to the designer would be to use a cascadeable shift register with 3-state outputs (i.e. a TTL 74LS395A) at the microprocessor and to convert from 10-bit serial to parallel data which would then be applied direct to the data bus in 2 words via the three-state outputs.

A ZN432 I/O INTERFACE

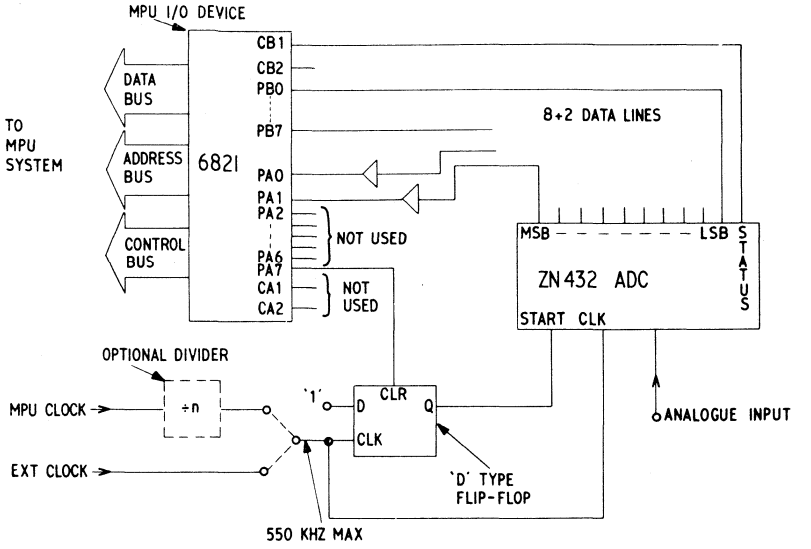


Fig. 4. ZN432 – 6800 I/O INTERFACE

Figure 4 illustrates one configuration of interfacing the ZN432 to an I/O device; in this case the 6821 Peripheral Interface Adaptor (PIA) device of the 6800 microprocessor family.

The PIA provides a flexible means of interfacing byte orientated peripherals to the microprocessor through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed individually to act either as an Input or an Output and each of the four control lines may be programmed for one of several control modes.

The diagram shows all 8 lines from Port B and 2 lines from Port A connected to the binary outputs of the ZN432. These lines are programmed as Inputs and allow the microprocessor to read the converted data by the execution of a microprocessor read peripheral data operation. Note the use of the two buffers on data lines PA1 snd PA2, these are necessary due to the higher input current of the Port A inputs.

The converter clock can be suppled either from the microprocessor clock or from an external source. Use of the microprocessor clock is preferrable since this allows a precise calculation to be made of the conversion time in terms of microprocessor machine cycles. If, however, the microprocessor clock is greater than the maximum converter clock rate of 550 kHz then it must be divided down to an acceptable level.

The 'D' type flip-flop is used to generate the Start pulse for the converter from the PA7 line, programmed as an output. The function of this flip-flop is to ensure that the Start pulse timing criteria with respect to the clock are met as explained earlier.

The STATUS output from the ZN432 is connected to CB1 control line. This can be programmed to set the interrupt flag bit-7 in Control Register B of the PIA, on occurrence of a positive transition of the CB1 input signal. The contents of this register can be read by the microprocessor and the state of this bit tested to determine the completion of the conversion cycle. Alternatively the PIA can be

programmed to generate a direct microprocessor interrupt from the Status signal on CB1. In this case, an interrupt routine in the program would be accessed on completion of a conversion and this would transfer the converter data via the PIA to defined storage locations in microprocessor registers or memory. This method is really only necessary if maximum utilisation of microprocessor time or converter data throughput is required. For situations where this is not critical the converter clock can be synchronised to the microprocessor clock as previously described, and a delay loop built into the program to allow for the conversion time. Since this is only 20 μs when running at the maximum clock rate a delay loop of only a few instructions will be sufficient to produce adequate delay.

A typical program to control the converter may be organised as follows:
Initially the PIA would be set-up with PB0 – PB7, PA0 and PA1 as Inputs, PA7 as an Output and Control Register B set to generate a microprocessor interrupt on a positive transition of the CB1 input. Note that the remaining lines PA2 – PA7, CA1, CA2 and CB2 are unused. A logic '0' followed by a logic '1' is then written to PA7; this clears the 'D' type and sets the START input, via the Q output, to a logic '0'. On the first positive going clock edge after PA7 returns to a logic '1' the Q output is clocked to a logic '1' allowing the ZN432 conversion cycle to proceed. (Note that it is not important if the START input is held low for several clock cycles, it will simply hold the converter with the MSB at a logic '1' and all other bits at a '0'). On the 11th negative clock edge after the Start pulse the STATUS output goes to a logic '1' indicating that the ZN432 has finished the conversion. This positive transition activates the $\overline{IRQ}$ line of the 6800, via the PIA, causing an interrupt. The 6800 stops execution of the current program sequence and begins an interrupt sequence. This involves saving the microprocessor register contents on the stack and setting the Interrupt Mask Bit so that no further interrupts will be serviced. The microprocessor is then directed to a vectoring address and branches to an interrupt routine in memory. This routine will read the converter data, via the PIA by addressing Ports A and B in turn and will then either store the data away in memory for future use, or will test the data and act accordingly on the results. Reading the data on Port B of PIA also has the effect of clearing the Interrupt Flag Bit. Resumption of the interrupted program sequence can now be made by execution of a Return from Interrupt (RTI) instruction.

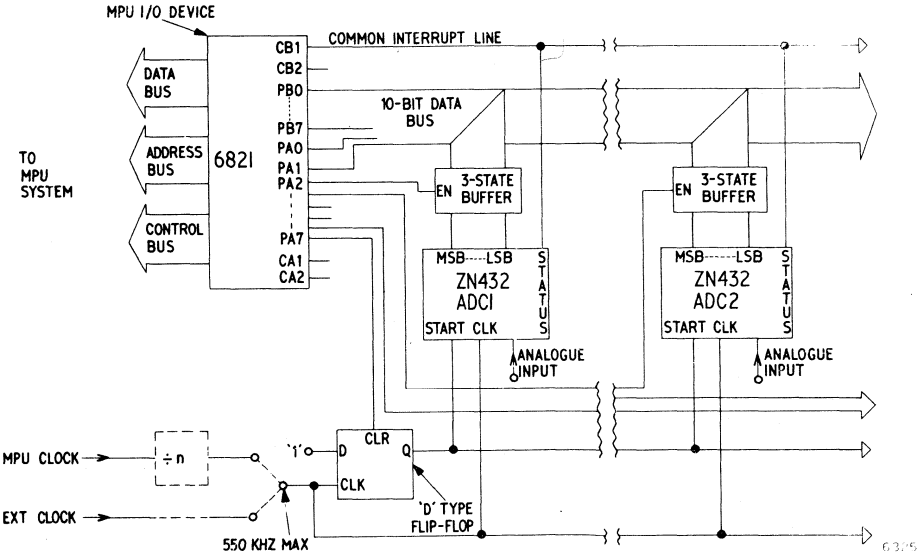


Fig. 5. MULTIPLE ZN432 – 6800 I/O INTERFACE

The configuration illustrated in figure 5 shows a suggested scheme for interfacing several ZN432's to an I/O device. This arrangement is similar to that previously described but in this circuit three-state buffers are used to interface each ZN432 to a common 10 bit bus from the PIA. The previously redundant lines PA2 – PA6 are now used to provide the enable signals for the three-state buffers. Note that the buffers of only one converter should be enabled at any one time otherwise false data will be read from the PIA.

The STATUS output of the ZN432 has a resistive pull-up load allowing typically up to 4 outputs to be 'wire-anded' together to form a common interrupt line. With the particular configuration shown a common Start signal for all the converters is produced, again from PA7 via the 'D' type flip-flop. Application of this signal would start all the converters simultaneously and a positive transition on the CB1 line would signify that all the converters had finished. Data from each converter would then be read by enabling the 3-state buffers via lines PA2 – PA6 in turn.

A ZN432 BUS INTERFACE

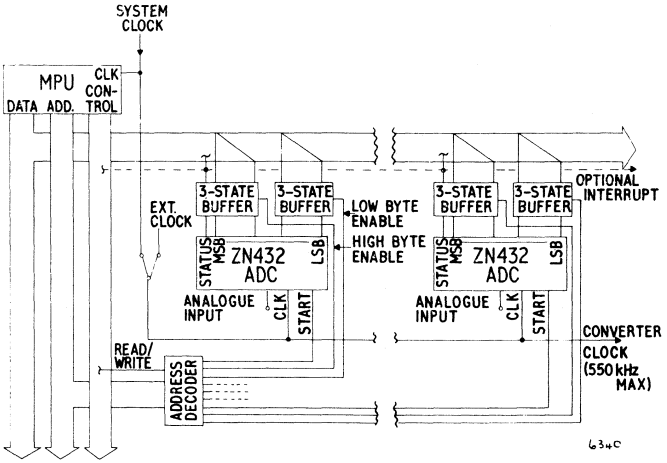


Fig. 6. MULTIPLE ZN432 MICROPROCESSOR BUS INTERFACE

The most versatile way of interfacing to a microprocessor is to go directly onto the Data Bus. Figure 6 illustrates this concept with the ZN432 where three-state buffers are again used but this time connected directly to the Data Bus of an 8-bit microprocessor such as the 6800. Since it is only an 8 bit bus the converter data has to be read in two words by enabling the buffers per converter in two groups as indicated by the High and Low Byte Enable lines per converter. One suggested scheme would be to transfer the output data as shown in Table 1. (Note that in converter terminology Bit 10 is the least significant bit (LSB).

TABLE 1

Data Bus Lines	Low Byte	High Byte
D7	Bit 3	—
D6	Bit 4	—
D5	Bit 5	—
D4	Bit 6	—
D3	Bit 7	—
D2	Bit 8	(Status)
D1	Bit 9	Bit 1 (MSB)
D0	Bit 10 (LSB)	Bit 2

The STATUS output can be read on the Data Bus with the High Data Byte or alternatively these outputs can be 'wire-anded' or gated together to produce a common interrupt signal.

The Start pulse and High and Low Byte Enable signals are generated from a logic block labled 'Address Decode Logic'. The function of this is to drive the appropriate input when the address, which has been allocated to that particular input, is present on the Address Bus and the Control Bus signals indicate a valid Memory Read or Write operation. Note that the level of address decoding used must ensure that the three-state buffers are disabled at all times except when the actual converter data should be on the bus, otherwise bus contention problems, with other devices using the bus may occur. A convenient means of address utilisation for the system in figure 6 is shown in Table 2, which allocates two consecutive addresses to each converter.

TABLE 2

ADDRESS	MPU READ	MPU WRITE
XXX 0	High Byte Enable ADC1	Start ADC1
XXX 2	Low Byte Enable ADC1	Start ADC1
XXX 2	High Byte Enable ADC2	Start ADC2
XXX 3	Low Byte Enable ADC2	Start ADC2
XXX 4	High Byte Enable ADC3	Start ADC3
etc.	etc.	etc.

(XXX = unique address for particular MPU system.)

A Write instruction to either address will then start that converter. On completion of the conversion, detected either by interrupt, testing of the Status Bit, or fixed program delay, the converter data can be read by a double byte load instruction which will load the data into two consecutive RAM memory locations or into a 16 bit microprocessor register, (i.e. Instruction LDX – Load Index Register of the 6800, loads the more significant byte of the index register from the byte of memory at the address specified by the program and loads the less significant byte of the index register from the next byte of memory at one plus the address specified by the program).

Note that the 'D' type flip-flop is not shown in figure 6. With a direct microprocessor clock it is possible to design the address decode logic so that the timing criteria of the Start pulse with respect to the clock input is complied with.

SUMMARY

Numerous different microprocessors are currently available and each microprocessor based control system will have its own individual data acquisition requirements. It is impossible in a paper of this type to cover all possible permutations of microprocessor/converter interfaces, but adoption of one of the two basic methods described here should be possible with most 8-bit microprocessors, allowing the design engineer to produce the most efficient data acquisition system to meet his design objectives. The ZN432's versatility and ease of use, coupled with its wide operating temperature range and TTL compatibility, will allow it to be used in a diverse range of applications where 10-bit accuracy is necessary.

Further information on the device characteristics and gain selection components, etc., is given in the ZN432 Series Data Sheet.

A Serial Interface For The ZN427 A/D Converter

A SERIAL INTERFACE FOR THE ZN427 A/D CONVERTER

In many data aquisition applications it is advantageous to situate the A/D converter close to the transducer and to transmit the digital data in serial form back to the data collection centre of the system. The serial data link uses less conductors and provides better noise immunity than a parallel data bus. This application note describes a RS-232C compatible serial data interface for the ZN427 8-bit A to D converter using an industry standard 6402 UART.

A simplified block diagram is shown in Fig. 1.

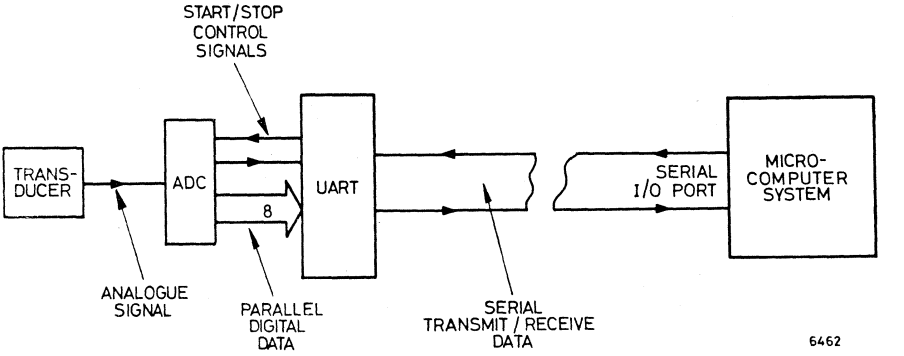


Fig. 1 Serial Data Interface

In order to initiate a conversion cycle a character is transmitted by the microcomputer. Upon receipt of this character by the UART its DR (Data Received) output goes to a high level which generates a start pulse for the A/D converter triggering a conversion cycle. At the end of the cycle the EOC (End of Convert) output is used to load the converted data into the UART which performs a parallel to serial conversion and transmits the data back to the microcomputer.

The ZN427 is an 8-bit successive approximation A to D converter. It features 3-state output buffers to permit bussing onto common data lines, fast 10 μs conversion time and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D to A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5V precision band-gap reference. A logic diagram of the converter is shown in Fig. 2. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a limiting resistor for the negative supply current. This will provide a nominal input voltage range of 0 to $V_{REF\ IN}$. Other input ranges both Unipolar and Bipolar can be obtained by connecting a simple resistor network to V_{IN} (Pin 6) as illustrated in Figs. 3(a) and (b). Further information on the ZN427 can be found in the Data Sheet.

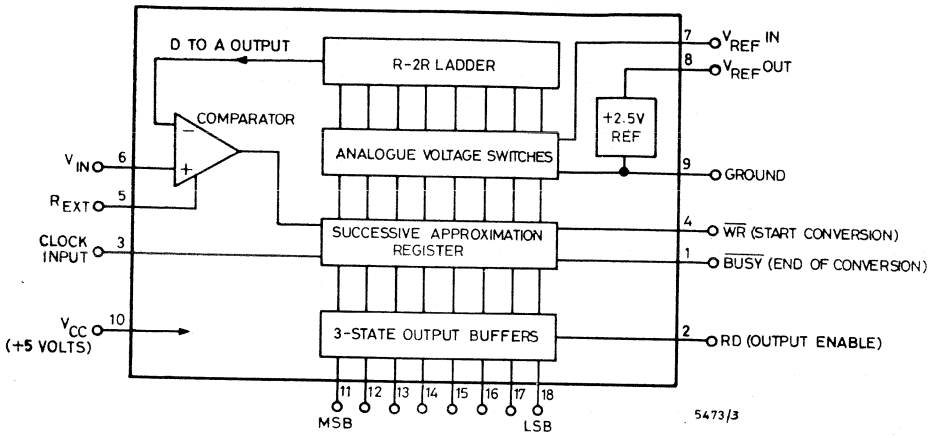


Fig. 2 System Diagram

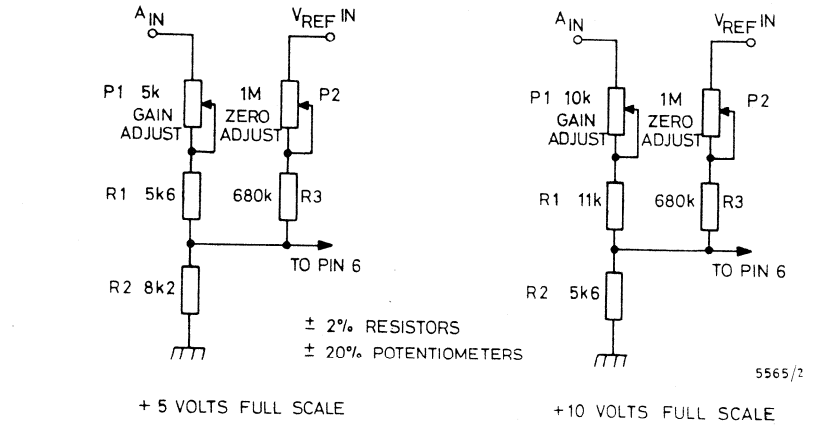


Fig. 3a Unipolar Operation - Component Values

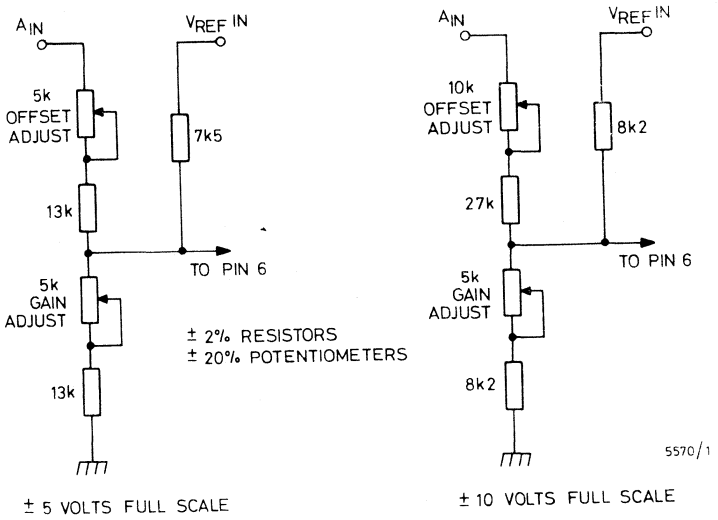


Fig. 3b Bipolar Operation – Component Values

A detailed circuit diagram of the converter interface is shown in Fig. 4.

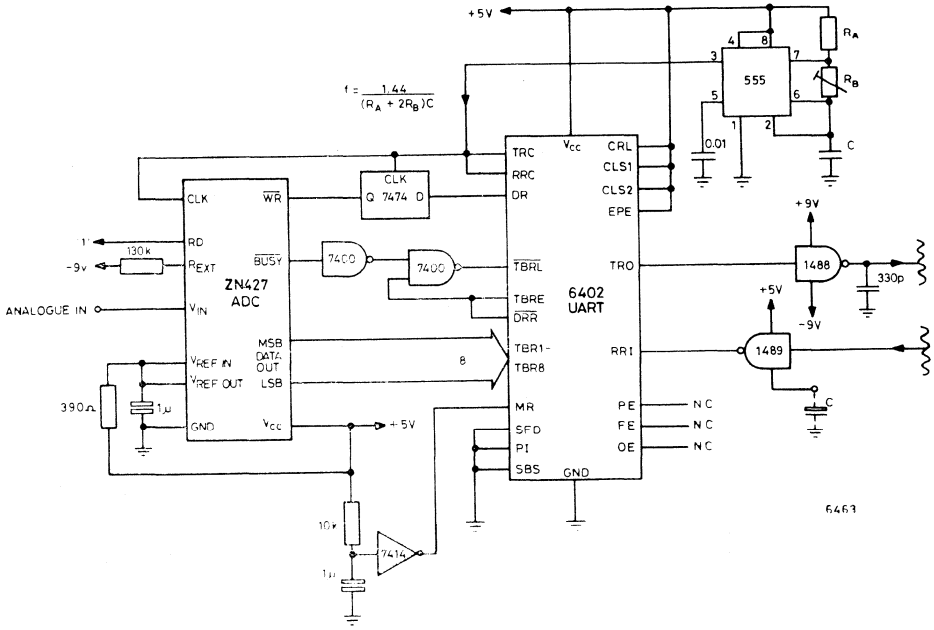


Fig 4. ZN427 UART Interface

The DR output of the UART is connected to the 'D' input of the 7474 latch, the 'Q' output of which drives the $\overline{WR}$ (Start Convert) input of the ADC. The use of this ensures that the timing of the $\overline{WR}$ pulse with respect to the converter clock input is correct. On the ninth negative clock edge after the $\overline{WR}$ pulse the $\overline{BUSY}$ output goes to a high level signalling that the conversion cycle is complete. This low to high transition is used to load the data into the UART via the TBRL (Transmitter Buffer Register Load Input). The signal is gated with the TBRE (Transmitter Buffer Register Empty) signal which holds the TBRL input high until the UART transfers the data to its transmitter register. If TBRL were allowed to return low before TBRE went high the converter data would be overwritten since the TBR (Transmitter Buffer Register) is a transparent latch. The TBRE signal is also used to drive the DRR (Data Received Reset) input which clears the DR output to a low level allowing another character to be received.

The waveforms associated with this operation are shown in Fig. 5. A simple oscillator using a 555 I.C. is shown which generates both the ADC clock and the Transmit/Receive clocks for the UART. The external clock is 16 times the data rate, the signal being divided internally by the UART. If a more stable data rate is an important factor then the 6403 UART, which is functionally similar but which uses a crystal oscillator as the timing source, may be substituted. In this case the ADC clock would still be generated by the 555 since it is not necessary for the converter and UART clocks to be synchronous. The UART control inputs CLS1, CLS2 (Character Length Select) ; PI (Parity Inhibit) ; EPE (Even Parity Enable) ; SBS (Stop Bit Select) are hard wired for whatever data format is wanted.

The MR (Master Reset) input is driven via a 7414 Schmitt trigger I.C. from a R-C delay circuit to generate the recommended reset pulse after power-up.

The 1488 and 1489 I.C.'s shown buffering the UART TRO (Transmitter Register Output) and RRI (Receive Register Input) pins are RS-232C compatible line drivers and receivers.

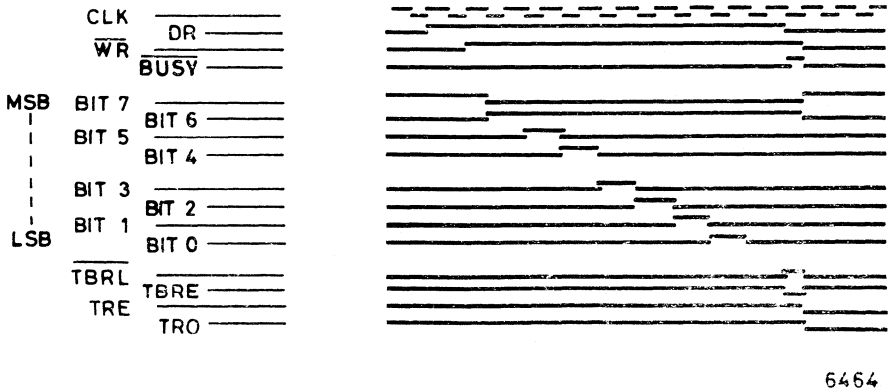


Fig. 5 ZN427 UART Interface Waveforms

In some applications incorporating microcomputers with RS-232C serial I/O ports no additional interfacing at the data collection centre end will be necessary. However if only a parallel I/O port is provided then another UART to convert the serial data back to parallel will be needed. An interface for the PET microcomputer which connects to the Parallel User Port on connector J2 is shown in Fig. 6. This uses the eight I/O data lines. PA0-PA7 and two control lines CA1 and CB2 which originate from a 6522 Versatile Interface Adaptor I.C. The data lines PA0-PA7 are connected to the RBR (Receive Buffer Register) outputs of the UART. The CA1 input is driven by the UART DR output and is operated in the latched mode which stores the received data within the VIA on a positive transistion of this pin. In order to initiate a new reading from the ADC the remaining control pin CB2 is used. This is connected to the UART inputs DRR and TBRL. When programmed to produce a negative going pulse the DR output is reset and a character is transmitted to the converter UART to start a new conversion cycle.

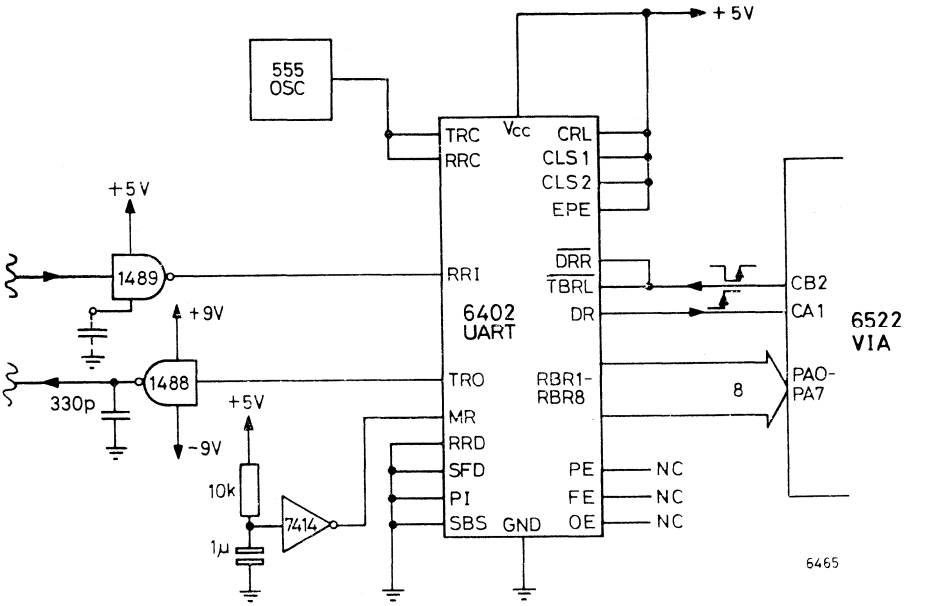


Fig. 6 6522 VIA UART Interface

A simple program example written in PET Basic is shown below.

PROGRAM EXAMPLE

```
10  REM UART INTERFACE REV. 3
20  REM SET PORT A TO INPUTS
30  POKE 59459, 0
40  REM DISABLE CA1 INTERRUPT
50  POKE 59470, 2
60  REM SET PCR TO 111XXXX1
70  POKE 59468, PEEK (59468) OR 225
80  REM SET ACR TO XXX000X1
90  POKE 59467, PEEK (59467) AND 227 OR 1
100 REM CLEAR CA1 FLAG IN IFR
110 A = PEEK (59457)
120 REM PULSE CB2 LOW-HIGH
130 POKE 59468, PEEK (59468) AND 31 OR 192
140 POKE 59468, PEEK (59468) OR 225
150 REM WAIT FOR +TRAN ON CA1
160 REM TEST CA1 FLAG IN IFR
170 IF (PEEK (59469) AND 2) THEN 190
180 GOTO 170
190 REM READ IRA AND CLEAR CA1 FLAG
200 A = PEEK (59457)
210 PRINT A
220 GOTO 120
```

Initially the appropriate VIA internal registers are set up and then a negative going pulse is produced on the CB2 pin. This starts a conversion sequence and when the new data is received the CA1 input goes high, latching the data in the VIA, and setting the CA1 Flag bit in the Interrupt Flag Register. This flag is tested by the program and when set the data is read and printed out. CB2 is again pulsed low and the sequence repeated.

For 6502 based microcomputer systems where all I/O lines of a 6522 VIA are available the CA2 pin can be used in the Read Handshake Mode in place of the CB2 pin, simplifying the program. Also the Status Flag of the UART can be monitored by the other I/O port lines for error checking purposes.

A Single Channel Codec

Acknowledgement: Ferranti wish to thank Mr. J. Everard and his colleagues of the British Post Office whose work this report is based upon and the Institute of Electrical and Electronic Engineers Inc. for permission to use extracts from a paper titled 'A Single Channel Codec' written by J. Everard and presented at ISSCC 78–Toronto.

INTRODUCTION

Conventional techniques for pulse code modulation (pcm) conversion for use in completely digital switching systems employ ladder networks requiring many high precision components to define the quantiser characteristic to sufficient accuracy. Alternative techniques employ linear ramps requiring either excessively high clock speeds or a number of ramps of precisely relative slopes.

In order to meet the signal-to-noise and gain-linearity constraints usually imposed on such systems, particularly for the telecommunications market, the use of expensive analogue to digital and digital to analogue hybrid circuitry is necessary. Due to the very high cost of the A/D and D/A component, multi-channel multiplexing techniques are usually employed.

The system described herein uses an advanced approach to a pcm codec (coder/decoder) designed at the British Post Office Research Centre at Martlesham Heath. The original aim was to produce an inexpensive codec capable of fully meeting the relevant C.C.I.T.T. recommendations. The B.P.O. realised that the way to achieve this was to make optimum use of state-of-the-art semiconductor L.S.I. technology. One such technology chosen was the Ferranti L.S.I. bipolar process. The result is a single channel codec of the type outlined in figure 1. The L.S.I. codec chip is the Ferranti ZNPCM1, the performance of which completely meets the performance specification defined by the British Post Office. The operation and realisation of the single channel codec is described in the following pages.

SYSTEM CONSIDERATIONS

The B.P.O. adopted an approach based on the principle of conversion to and from pcm via an intermediate digital code format, i.e. the encoder may consist of a waveform tracking encoder to provide highly oversampled A/D conversion followed by digital processing logic to convert the intermediate code to pcm. The decoder may consist of digital processing logic to convert pcm to some intermediate code format and a simple D/A to convert from the intermediate code to analogue. B.P.O. studies revealed that a trade-off was necessary between analogue A/D and D/A simplicity and conversion logic speed and complexity.

The trade-off was taken to its limit resulting in the simplest form of A/D and D/A converters possible providing that circuitry was realisable with state-of-the-art L.S.I. technology. Fig. 1 shows a block schematic of the basic codec.

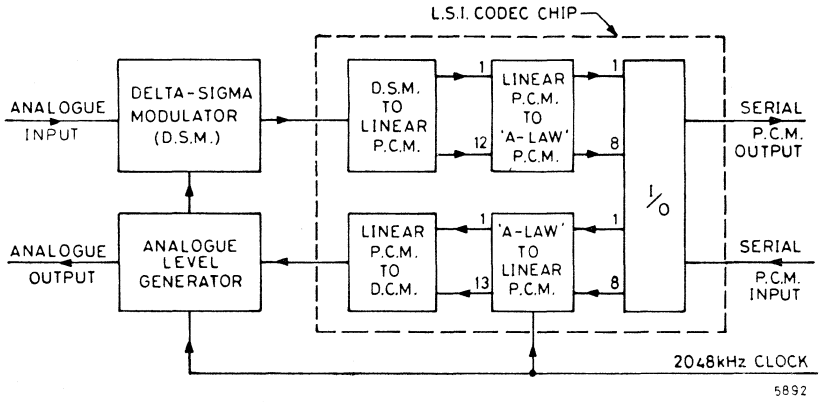


Fig. 1. Codec Schematic

The intermediate code format chosen for both encoder and decoder is that produced by a delta sigma modulator (dsm). It is especially simple to convert from this format back to analogue as one only has to pass the digital stream through a low pass filter cutting off just above the highest signal frequency to be recovered (3.4 kHz).

The area enclosed by the dotted line indicates the functions integrated into the L.S.I. codec chip ZNPCM1. The dsm circuitry is presently realised using discrete TTL logic, a differential amplifier, resistors and capacitors. However under development at present at Ferranti is an I.C. dsm solution which will be available by mid-1979.

THE DELTA SIGMA MODULATOR (DSM)

A modified form of delta sigma modulator/demodulator is used, resulting in an adequate performance using a clock rate as low as 2.048 kHz. Fig. 2 shows the functional circuit of the dsm, incorporating an operational amplifier integrator, and a D-type bistable for the threshold detector and approximation level generator. The modulator accepts a band-limited analogue input signal (300-3400 Hz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The demodulator produces one of two precisely defined analogue levels in response to the single bit/sample delta sigma bit stream.

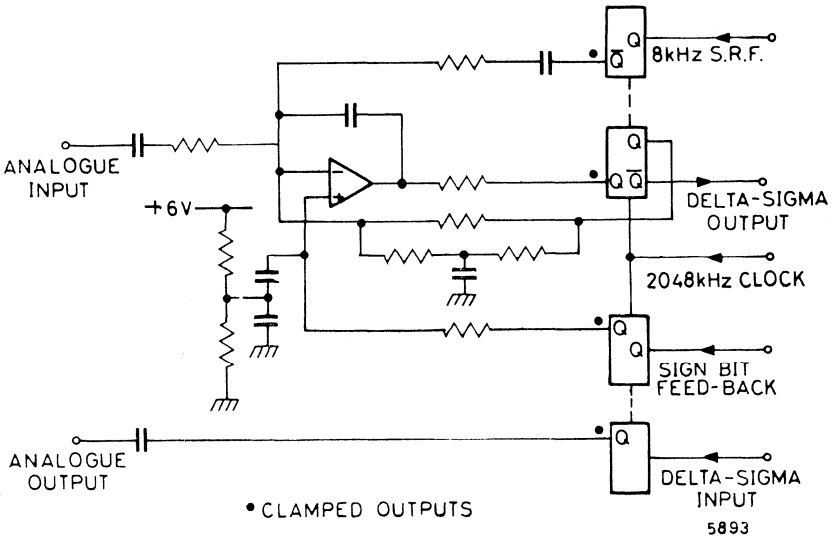


Fig. 2. Modulator/Demodulator Circuit

The modulator circuit relies on the use of two logic signals being fed back from the code converter; the sign bit of the generated pcm codewords, used to control the d.c. alignment conditions, and an 8 kHz square wave (Spectral Redistribution Function) which is added to the input signal to improve performance. A complex feedback network is also used to feed back a higher level of quantisation noise below approximately 16 kHz to shift quantisation noise to higher frequencies where the code converter provides greater suppression. In the reverse direction the decoder delta sigma stream coming from the code converter is passed through a D-type bistable for edge re-timing and level definition before the required analogue signal is recovered by low-pass filtering.

Encoder and decoder gain errors due to initial component variations from their nominal values are corrected at a gain adjustment point in the system. The main requirement is on gain stability, rather than absolute gain. The gain is a factor of both resistor ratios and the D-type output voltages. The output voltages are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the codec, and clamping the high state output voltages to a 2.45V reference by the use of schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, together with a small modulator/demodulator physical size, by implementing the resistors and small capacitors as an in-line passive hybrid.

The modulator also includes a 'fast start' circuit to ensure rapid stabilisation of the d.c. conditions when the codec is powered-up. This is important when the codec is used in switching applications where considerable power savings arise if the codec is only powered-up when required.

The detail circuit of the dsm is shown in Fig. 3. In addition to the basic modulator and demodulator circuit the decoded output is shown being fed into a simple second order Sallen and Key filter. This is shown as a technique for demonstrating the equalisation of sin.x/x distortion resulting from the sample and hold process of the decode function. The compensation would normally be provided as an integral part of the decoder band limiting filter.

Ferranti have under development an integrated circuit version of the dsm and samples will be available by mid-1979. The I.C. version will be much less dependent on external component tolerances than the discrete version. Only 7 or 8 external R and Cs will be required. The I.C. will be available in an 18 pin plastic or ceramic package and should also allow improved speed performance compared to the discrete solution. Fig. 4 shows an advance drawing of what the two I.C. single channel codec is expected to be, however this may be subject to change depending upon the final evaluation of the dsm integrated circuit.

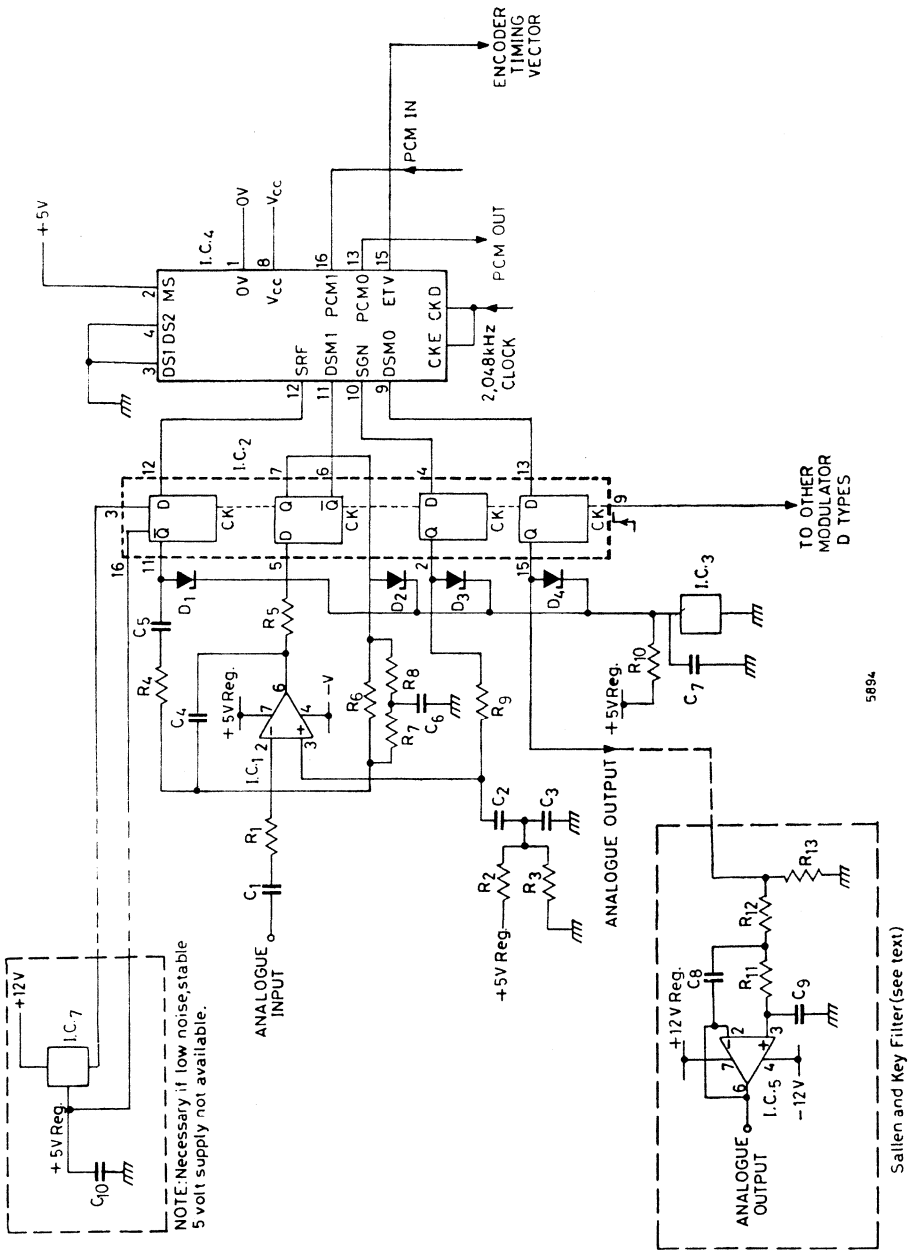


Fig. 3. Discrete Delta Sigma Modulation Circuit

COMPONENTS LISTING FOR COMPLETE CODEC CIRCUIT

1. MAIN CIRCUIT

Integrated Circuits

I.C.1	—	CA3140S/T
I.C.2	—	SN74175N J or ZN74175 E/J
I.C.3	—	ZN458
I.C.4	—	ZNPCM1E or J

Diodes

D1, D2, D3 and D4	—	ZC2800 or 1N6263

Capacitors

C1	—	3.3 μF ±20%
C2 & C3	—	6.8 μF ±20% (6.3V)
C4	—	68 pF ±20% } +15%, –18% (See Note 1)
C5	—	15 nF ±10% } +15%, –18% (See Note 1)
C6	—	10 nF ±2% } +15%, –18% (See Note 1)
C7	—	6.8 μF ±20% (6.3V)

Resistors

R1	—	2.7kΩ ±2% (High Stability Resistor)
R2	—	10kΩ ±2%
R3	—	4.7kΩ ±2%
R4	—	47kΩ ±2%
R5	—	620Ω ±5%
R6	—	10kΩ ±2% (High Stability Resistor)
R7 and R8	—	2kΩ ±2% (High Stability Resistor)
R9	—	2.7kΩ ±10%
R10	—	260Ω ±10%

NOTE 1. Limits apply over temperature range and equipment working life.

NOTE 2. High stability resistors should track each other to ±1% to meet British Post Office Specification Requirements.

2. SUBSIDIARY CIRCUITS

Integrated Circuits

I.C.5	—	ZLD741C
I.C.7	—	LM78LO5ACH

Capacitors

C8	—	1 nF ±2%
C9	—	10 nF ±2%
C10	—	2.2 μF ±20%

Resistors

R11 & R12	—	91.8kΩ ±1%
R13	—	100kΩ ±5%

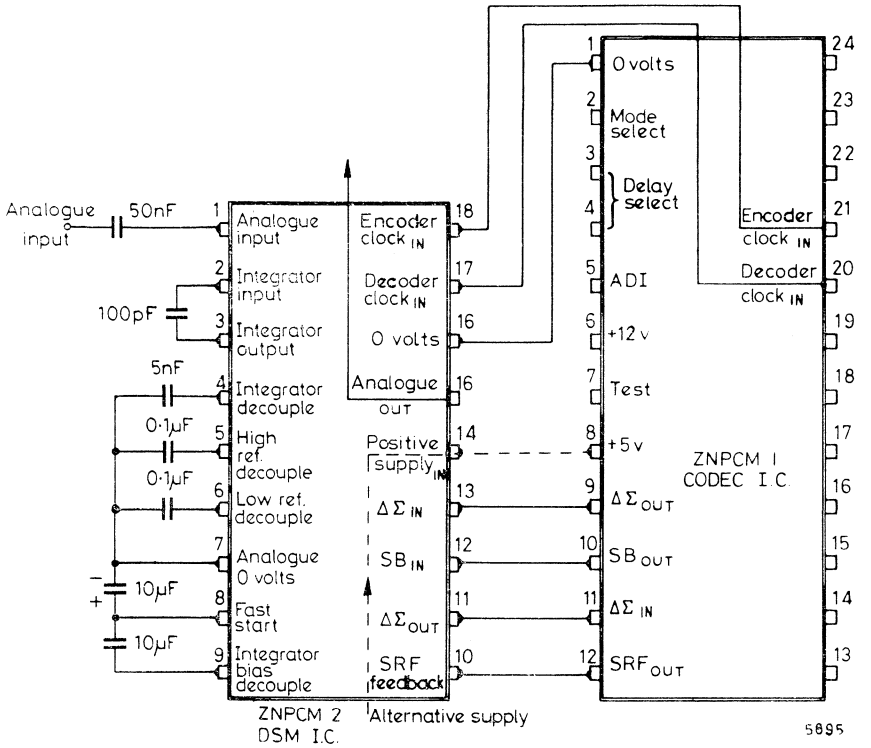


Fig. 4. DSM-Codec Interface

THE CODE CONVERSION

The dsm signal is fed into the integrated circuit at 2,048 kbits/second and converted to compressed pcm at a bit rate of 64 kbits/s or, by the application of external timing signals a maximum of 2,048 kbits/s for multiplexing in a burst format. Conversely the I.C. will accept at the pcm interface either a 64 kbit/s stream or, by the application of external timing signals, a bit rate of up to 2,048 kbit/s in a burst format. This is then converted to a delta sigma pulse stream of 2,048 kbit/s. The actual code conversion can be broken down into two stages; (i) Delta Sigma to linear pcm and vice-versa; (ii) Linear pcm to compressed pcm and vice-versa.

(i) *Delta sigma to Linear pcm*

The converter operates by multiplying the 256 delta sigma input samples occurring in each 125 microsecond pcm sample period by coefficients according to a triangular profile and accumulating the products to form the required linear pcm codeword at the end of the interval. Fig. 5 shows the converter logic structure.

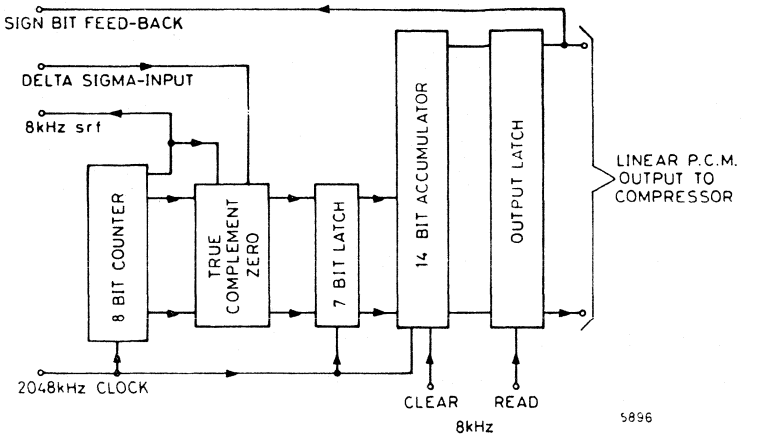


Fig. 5. Delta sigma to Linear pcm Converter

It consists of an eight bit counter, logic for operating on the seven least significant bits of the counter, a re-timing buffer, a 14 bit accumulator and an output latch. The first seven bits of the counter generate numbers zero to 127 as shown in Fig. 6(a). The eighth bit divides the generated number sawtooth into odd and even phases as shown in Fig. 6(b). Bit eight is also used in conjunction with the delta sigma ($\Delta\Sigma_i$) output to operate on the seven bit count sequence to produce the correct value of $\Delta\Sigma_i W_i$ to be added into the accumulator, where W_i is the required weight from the triangular profile during the ith clock period.

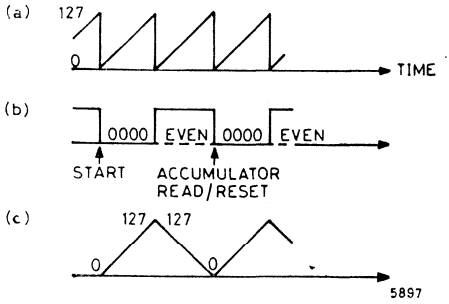


Fig. 6. a) 7 Bit Counter Number Sawtooth
b) Counter Most Significant Bit
c) Effective Available Weight Sequence

The technique of generating a triangular co-efficient profile allows a continuous up-counter to be used, which in turn allows the easy generation of the required timing waveforms to drive different parts of the codec. The 8 kHz square wave used within the modulator is taken from the most significant bit of the counter and the sign bit feedback to the modulator is derived from the output latch.

The converter produces 14 bit linear pcm codewords at 8k samples/s with an effective accuracy such that the signal to noise ratio obtained, after converting the 'A' law pcm, complies with C.C.I.T.T. recommendations.

In the decode direction the principle of conversion is the implementation of the delta sigma algorithm (see appendix 1) in all digital logic. The linear pcm input appears as a sample and held signal, the digital dsm performing a continuous conversion to the delta sigma format. The realisation of the circuitry is shown in Fig. 11.

(ii) *Linear PCM to Compressed PCM*

A useful relationship exists between linear pcm codewords and their 'A law' compressed equivalents allowing conversion between the two formats to be readily accomplished using data selection techniques. Fig. 7 shows a linear pcm to 'A law' pcm converter where the segment code is derived directly from the linear codeword using combinational logic. The segment code is then used to control a data selection matrix to extract the required interval code.

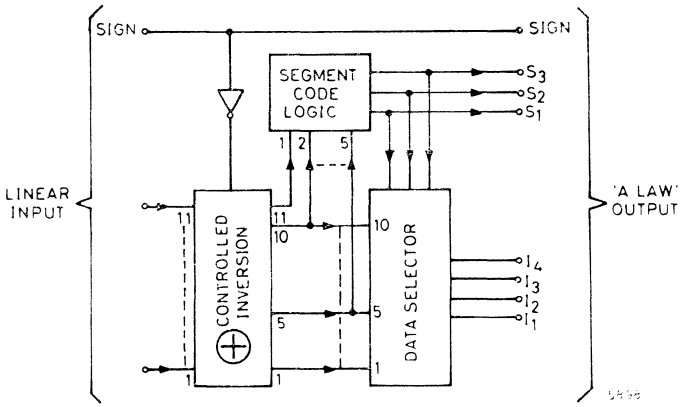


Fig. 7. Linear to 'A Law' Converter

Facilities are provided for controlled alternate digit inversion of the 'A law' codewords prior to parallel to serial conversion for serial output. In most applications ADI must be provided but for testing purposes it is useful if it can be removed.

Similar techniques are used in the decode direction to convert the compressed pcm into linear pcm.

INPUT-OUTPUT INTERFACE

One of the most important features of a pcm codec is the structure of its input-output interface as this directly influences the ease with which the codec can be used in a given application. A very flexible I/O interface has been included which can operate in either of two modes by means of pin selection.

In the first mode the pcm codewords are clocked in and out automatically at 64 kbits using clocks internally derived from the applied 2,048 kHz clock. The only timing waveform required is a timing vector to indicate when the first bit (the sign bit) of each codeword is required (which automatically defines the positions of the other bits at this rate). To take account of many applications where the received pcm codewords are not in the frame alignment with the transmitted codewords, two pins are provided for the user to strap appropriately to indicate the actual displacement. The four possibilities allow for zero to three digits delay of the received with respect to the transmitted codewords.

In the second mode, a much wider range of operation is possible. The pcm codewords may be clocked in and out at any rate in the range 64 to 2,048 kbits. Access is provided to the output and input shift registers to allow the multiplexing and demultiplexing of signalling bits if required. Also separate encoder and decoder 2,048 kHz clock inputs are provided to allow asynchronous working between the two directions of transmission, which is typical of pcm multiplex applications.

ZNPCM1 – THE L.S.I. CODEC

From its initial conception the codec has been designed with a view to producing the circuit in an L.S.I. semiconductor technology. Using advanced circuit design, photographic mask making and processing techniques developed originally for the F100L 16 bit bipolar microprocessor[2] Ferranti have produced a single chip codec incorporating all the circuit functions shown in the dotted rectangle in Fig. 1. The device operates from a single 5V supply with a maximum operating frequency of 6 MHz and all inputs and outputs are TTL compatible. For reduced power requirements the device will operate down to 3.5V maintaining TTL compatibility and as low as 3V with some degradation of input/output voltage levels.

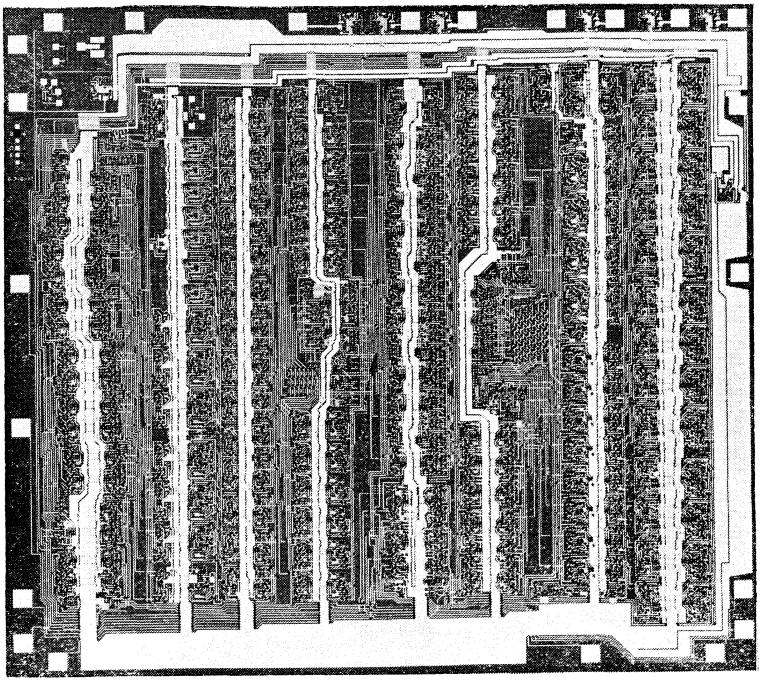


Fig. 8. Codec Chip Photograph

The chip size is 178 thou. by 163 thou. (see Fig. 8) and is available in a 24 lead D.I.L. ceramic (ZNPCM1J) or moulded package (ZNPCM1E).

Performance

The codec described meets all the performance requirements of the C.C.I.T.T. Recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

1. Idle channel noise: –69 dBmOp

   (C.C.I.T.T. recommendation = –65 dBmOp)

2. Signal-to-noise ratio and Gain-level linearity: Figs. 9(a) and 9(b) show the results using a 450-550 kHz pseudo-random noise test.

3. Intermodulation distortion:

   Measured products are at least 10 dB and on average 18 dB better than the C.C.I.T.T. recommendations.

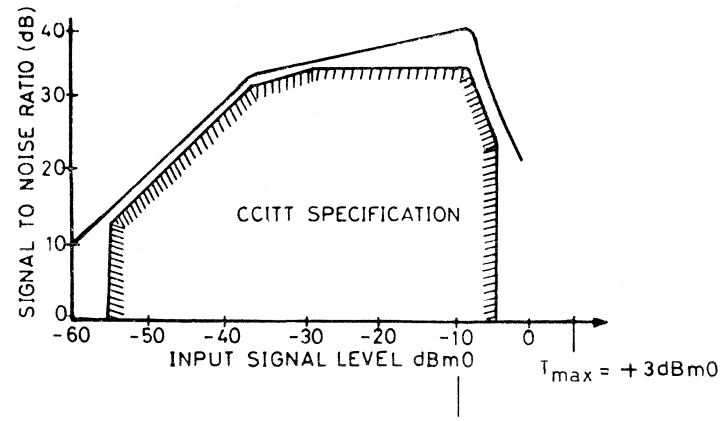


Fig. 9(a). Signal to Noise Ratio, 'A law'

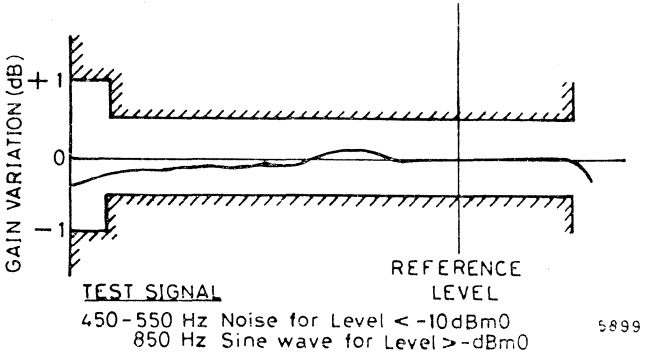


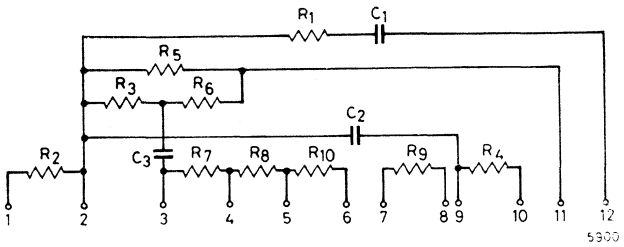
Fig. 9(b). Gain to Signal Level, 'A law'

Another aspect of the codec performance is the Sinc (π ft) decoder frequency characteristic, having infinite attenuation at 8 kHz and multiples thereof, introduced by the digital full-width sample and hold process occurring within the code converter. Although this requires equalisation in-band with an appropriate analogue post filter design, the characteristic ensures complete suppression of the sampling frequency components and harmonics, independent of any d.c. offset in the received codewords.

The sinc (π ft) characteristic is also useful when considering the design of less complex analogue filters to be used with the codec in digital switching applications, where codecs may be provided on a per customers line basis. A less complex filter may be allowable since, in the local telephone networks, there is not the problem of interworking with frequency division multiphase systems.

APPENDIX 1

DSM Hybrid



Component Values

R1	47kΩ		R4	620Ω	
R2	2.7kΩ		R9	2.7MΩ	±20%
R3	2kΩ		R10	260Ω	
R5	10kΩ	±5%			
R6	2kΩ				
R7	4.3kΩ				
R8	10kΩ				
C1	15 nF				
C2	68 pF	+15%, –18%			
C3	10 nF				

Resistor Ratio Tolerances

If, $R_p = \dfrac{(R_3 + R_6)\,R_5}{(R_3 + R_6 + R_5)}$

then R_p/R_2 shall commence with ±5% of the nominal ratio and then remain with ±1% of the starting ratio over operating temperature range and equipment life.

The ratios R_p/R_1 and $R_7/R_7 + R_8$ will remain within ±5% of nominal ratios.

The tolerances quoted are those required over the temperature range and working life to obtain a performance compatible with that required by the British Post Office and may be relaxed for less stringent requirements.

The hybrid is packaged in a single in-line package with 0,24 mm lead pitch and a maximum length of 33 mm, width of 6,35 mm and height of 17,8 mm. For further details contact:–

Type: CN466A

Allen Bradley Electronics Ltd.,
Bede Trading Estate,
Jarrow,
Tyne and Wear, NE32 3HG
Telephone: 0632 (Jarrow) 897771.

Type: TIM529

Tectronic (Electronics Ltd.),
Cirtec Works,
Wokingham,
Berkshire, RCH 2YD
Telephone: 0346 (Crowthorne) 5115.

APPENDIX 2

Fig. 10 shows the algebraic notation used for the numbers existing within the modulator during the nth clock cycle.

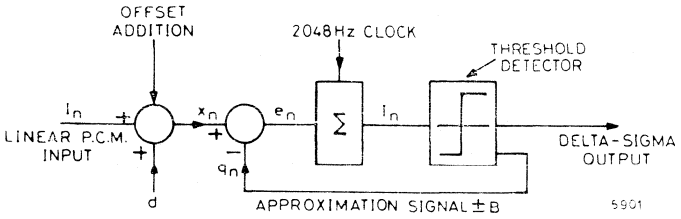


Fig. 10. The Digital DSM

The 13 bit linear pcm input I_n has a constant offset d added to it, resulting in a number $x_n = I_n + d$ being presented to the digital dsm. The offset d, equal to 1/16th of the peak pcm codeword magnitude, acts as a spectral redistribution function[3] which improves the performances considerably. The approximation signal q used in the feedback loop can take one of two binary numbers +B or −B. The difference $e_n = x_n - q_n$ is presented to a digital integrator. At the end of clock period 'n', e_n is added to I_n, the integral or sum of all previous differences to form $I_n + 1$.

$$\text{i.e., } I_n + 1 = I_n + e_n = \sum_{o}^{n} (x_i - q_i)$$

The threshold detector outputs the sign of $I_n + 1$ which is used to control the sign of the approximation signal during the $(n + 1)$th period the sign being chosen so as to minimise the integral,

i.e., $q_n + 1$ B sgn $(I_n + 1)$

over a period of m dsm cycles

$$I_n = I_n - m + \sum_{n-m}^{m-1} (x_i - q_i)$$

Rearranging and dividing by m:

$$\frac{1}{m}\sum_{n-m}^{n-1} q_i = \frac{1}{m}\sum_{n-m}^{n-1} x_i - \frac{1}{m}(I_n - I_{(n\ m)})$$

i.e., the mean value of q over m cycles is equal to the mean value of the input x plus some error term. The larger the value of m the smaller the error term becomes. Viewed in the frequency domain the feedback loop causes the low frequency components of q to track the baseband frequency components of the input x, any difference being the inband quantisation noise due to the transformation or coding process.

Fig. 11 shows the circuit realisation of the digital dsm. The simplicity of the configuration arises from choosing the magnitude of the approximation levels $\pm B$, such that the difference between x_n and q_n can be formed by combinational logic techniques on the most significant bits of x_n and q_n without performing a full subtraction operation. Generalising, if x is represented by a two's complement number k bits in length, then,

$$-2^{k-1} \leqslant x \leqslant 2^{k-1} - 1$$

The two possible values of q are made

$$+ B = 2^{k-1} \text{ and } - B = -2^{k-1}$$

As a consequence the k + 1 bit value of e can be formed by using the k – 1 least significant bits of x (unchanged) combined with two bits in the most significant positions which are inverses of the sign bits of x and q, hence the logic structure shown in Fig. 11. The digital dsm cycle rate is governed by the rate at which the accumulator latch is clocked, the delta sigma output being taken from the sign bit of the accumulator.

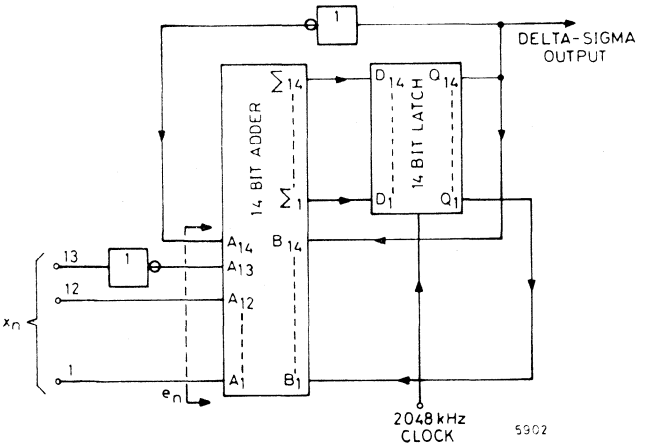


Fig. 11. Digital DSM Circuit Realisation

References

1. C.C.I.T.T. Orange Book Vol. III – 2 Rec. G711, 712.
2. F100L circuit, Design and Manufacture by Mr. D. Grundy – Electronic Equipment News, May 1978.
3. Everard, J.D. 'Single Channel PCM Codec' IEE Journal –Solid State CCTS Vol. COM 27 No. 2. Feb. 1979 par. 1 pp 25-38.

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