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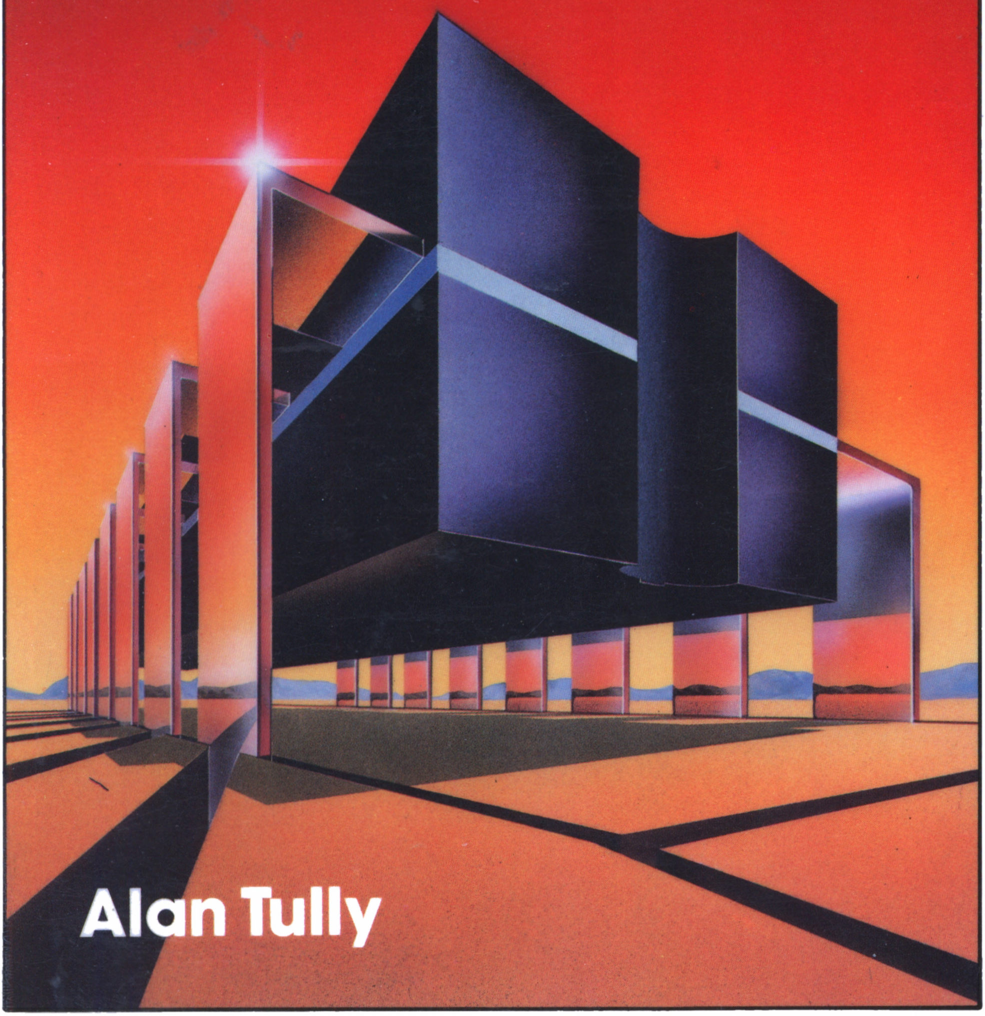
Z-80 REFERENCE GUIDE



Alan Tully

Z80 Reference Guide

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CHAPTER 1

Introduction

This book is intended for users and prospective users of Z8Ø based micro-computers who already have some machine code programming experience and wish to extend their ability to write and modify programs. It is designed to be a convenient reference manual when specifying and coding new programs or debugging and modifying existing systems and programs.

The Zilog Z8Ø micro-processor was designed to be compatible with the Intel 8Ø8Ø range of micro-processors. That is programs which run on Intel 8ØØ8 or 8Ø8Ø processors will also run ont he Z8Ø, although, as the Z8Ø provides additional facilities (instructions, registers, block input/output, etc.) it is extremely unlikely that a program written for the Z8Ø would run successfully on either the 8ØØ8 or 8Ø8Ø.

Chapter 2 describes the various registers provided in the Z8Ø and contains tables showing the effect various groups of transactions have on the Flag Register.

Chapter 3 gives brief details of the timing principles used in the Z8Ø.

Chapter 4 contains a summary of the instructions, identified within a number of groups, each of which is related to specific functions or activities. This chapter is intended for the programmer who knows what is required of the program and needs to select the most appropriate instruction(s).

Chapter 5 gives full details of each individual instruction, together with its effect on the Flag Register, Timing and an example of all except the most simple instructions.

Chapter 6 contains various practical hints and tips based on the experience of a number of individual programmers.

The following tables are provided as appendices for easy reference:
Appendix A — ASCII Codes.
Appendix B — ASCII Hexadecimal/Decimal Conversion.
Appendix C — Glossary of Terms and Abbreviations used in this book.
Appendix D — Table of Instructions by Operator Code, indexed.
Appendix E — Table of Instructions by mnemonics, indexed.

CHAPTER 2
Registers and Flags

Z8Ø Registers can be considered under three different groups:

Type of Register	**No.**
General Purpose Registers	14
Flag Register	1
Special Purpose Registers	6

General Purpose Registers

Fourteen 8-Bit General Purpose Registers are provided, in two sets, identified as A, B, C, D, E, H and L plus A′, B′, C′, D′, E′, H′ and L′. Only one set, together with the equivalent Flag Register (F or F′) can be in use at any one time. A "set" of registers may consist of either A and F or A′ and F′ plus either B, C, D, E, H and L or A′, B′, C′, D′, E′, H′ and L′, i.e.:

Set		Set		Set		Set
A		A		A′		A′
B		B′		B		B′
C		C′		C		C′
D	or	D′	or	D	or	D′
E		E′		E		E′
H		H′		H		H′
L		L′		L		L′

Special Register Selection instructions provide the facility to switch between the two sets of registers, allowing extra storage in registers, which is much faster than using external memory, particularly if interrupts are likely to occur.

The A Register is the Accumulator and is the most frequently used of all the registers. The result of an Arithmetic or Logical operation, such as ADD, SBC, XOR, etc., is always stored in the Accumulator (Register A).

The remaining six General Purpose Registers in a set can be used to store either data or memory addresses and are frequently referred to as Register Pairs — BC, DE, HL. This enables a Register Pair to be used to store a complete memory address (up to 64K) or to provide double precision arithmetic facilities.

NOTE: The H and L registers were originally designated as such because one held the High (H) byte of a memory address and the other the Low (L) byte of the same memory address.

Register Pairs

B	C	← BC		B'C'→	B'	C'
D	E	← DE		D'E'→	D'	E'
H	L	← HL		H'L'→	H'	L'
High Order Byte	Low Order Byte				High Order Byte	Low Order Byte

Flag Register

Two Flag Registers are provided, one identified as the F Register, which is always associated with Register A, and the other identified as F', which is always associated with Register A'. The Flag (F) Register contains 8 Bits, as do the General Purpose Registers, but each individual Bit is used to identify conditions within the C.P.U. (Central Processing Unit) which exist after an instruction has been obeyed. The purpose of each Bit within the Flag Register is given on the next page.

Bit Positions

7	6	5	4	3	2	1	Ø

Bit	**Flag**	**Details**
7	Sign	SET = 1 if the result of certain operations are negative, RESET = Ø if the result is not negative. (See Table 2.1)
6	Zero	SET = 1 if the result of certain operations are zero, RESET = Ø if the result is not zero. (See Table 2.1)
5	—	Not used.
4	Half Carry	Indicates whether there has been a carry from Bit 3 (Add operations), borrow from Bit 4 (Subtract operations) or if the Low Order half byte of the result of an operation has a value greater than 1ØØ1, i.e. is invalid for Binary Coded Decimal purposes. (See Table 2.3)
3	—	Not used.
2	Parity/Overflow	A dual-purpose flag. When used to indicate Parity, it is SET = 1, for Even Parity and RESET = Ø for Odd Parity. When used to indicate Overflow it is SET = 1 if the result of an arithmetic operation is too large to be contained in 8 Bits (or 16 Bits for Two Byte operations). (See Table 2.4)
1	Subtract	SET = 1 if the instruction was a Subtract operation, RESET = Ø if the instruction was an Add Operation.
Ø	Carry	Indicates whether there has been a Carry or Borrow during Arithmetic operations and can be SET or RESET by certain Shift and Rotate operations. (See Table 2.5)

Table 2.1 — Sign Flag

Instruction Group (See Ch.4)	Instructions	Effect
Single Byte Load Group	LD A,I	SET = 1 if the I Register is negative, otherwise RESET = Ø.
Exchange, Block Transfer and Search Group.	CPI CPIR CPD CPDR	SET = 1 if the result is negative, otherwise RESET = Ø.
Single Byte Arithmetic Group	ADC A,s ADD A,s AND s CP s DEC s INC s OR s SBC A,s SUB s XOR s	SET = 1 if the result is negative, otherwise RESET = Ø.
Two Byte Arithmetic Group.	ADC HL,rr SBC HL,rr	SET = 1 if the result is negative, otherwise RESET = Ø.
General Purpose Arithmetic and C.P.U. Control Group	DAA	SET = 1 if the most significant bit of the Accumulator = 1, otherwise RESET = Ø.
	NEG	SET = 1 if the result is negative, otherwise RESET = Ø.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

Rotate and Shift Group	RL s RR s RLC s RRC s SLA s SRA s SRL s	SET = 1 if the result is negative, otherwise RESET = Ø.
	RLD RRD	SET = 1 if the Accumulator is negative after the shift, otherwise RESET = Ø.
Bit Set, Reset and Test (Flag) Group.	BIT b,r	Unknown
Input and Output Group	IN R,(C)	SET = 1 if the input data is negative, otherwise RESET = Ø.
	IND INDR INI INIR OTDR OTIR OUTD OUTI	Unknown

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

Table 2.2 — Zero Flag

Instruction Group (See Ch. 4)	Instructions	Effect
Single Byte Load Group	LD A,I	SET = 1 if I Register = Ø, otherwise RESET = Ø.
	LD A,R	SET = 1 if the R Register = Ø, otherwise RESET = Ø.
Exchange, Block Transfer and Search Group	CPD CPI CPDR CPIR	SET = 1 if the contents of the Accumulator = the contents of the memory location whose address is held in Register Pair HL.
Single Byte Arithmetic Group	ADC A,s ADD A,s CP s DEC s INC s OR s SBC A,s SUB s XOR s	SET = 1 if the result = Ø, otherwise RESET = Ø.
Two Byte Arithmetic Group	ADC HL,rr SBC HL,rr	SET = 1 if the result = Ø, otherwise RESET = Ø.
General Purpose Arithmetic and C.P.U. Control Group	DAA NEG	SET = 1 if the result = Ø, otherwise RESET = Ø.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

Rotate and Shift Group	RL s RR s RLD RRD RLC s RRC s SLA s SRA s SRL s	SET = 1 if the result = Ø, otherwise RESET = Ø.
Bit Set, Reset and Test (Flag) Group	BIT b,r	SET = 1 if the nominated Bit in the specified Register = Ø, otherwise RESET = Ø.
Input and Output Group	IN r,(C)	SET = 1 if the Input Data = Ø, otherwise RESET = Ø.
	IND INI	SET = 1 if the contents of Register B − 1 = Ø, otherwise RESET = Ø.
	INDR INIR	SET = 1.
	OTDR OTIR	SET = 1.
	OUTD OUTI	SET = 1 if the contents of Register B − 1 = Ø, otherwise RESET = Ø.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

Table 2.3 — Half Carry Flag

Instruction Group (See Ch. 4)	Instructions	Effect
Single Byte Load Group	LD A,I LD A,R	RESET = Ø.
Exchange, Block Transfer and Search Group	CPD CPI CPDR CPIR	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
	LDD LDI LDDR LDIR	RESET = Ø.
Single Byte Arithmetic Group	ADC A,s ADD A,s INC s	SET = 1 if Carry from Bit 3, otherwise RESET = Ø.
	CP s DEC s SBC A,s SUB s	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
	AND s OR s XOR s	SET = 1.
Two Byte Arithmetic Group	ADC HL,rr ADD HL,rr ADD IX,rr ADD IY,rr	SET = 1 if Carry from Bit 11, otherwise RESET = Ø.
	SBC HL,rr	SET = 1 if no Borrow from Bit 12, otherwise RESET = Ø.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

General Purpose Arithmetic and C.P.U. Control Group	CCF	Not affected.
	CPL	SET = 1.
	DAA	Not known.
	NEG	SET = 1 if no borrow from Bit 4, otherwise RESET = Ø.
	SCF	RESET = Ø.
Rotate and Shift Group	RL s RR s RLA RLD RRA RRD RLC s RRC s RLCA RRCA SLA s SRA s SRL s	RESET = Ø.
Bit Set, Reset and Test Group	BIT r,s	SET = 1.
Input and Output Group	IN r,(C)	RESET = Ø.
	IND INI INDR INIR OTDR OTIR OUTD OUTI	Not known.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

Table 2.4 — Parity/Overflow Flag

Instruction Group (See Ch. 4)	Instructions	Effect
Single Byte Load Group	LD A,I LD A,R	Set equal to the contents of IFF2.
Exchange, Block Transfer and Search Group	CPD CPI CPDR CPIR LDD LDI	SET = 1 if the new contents of Register Pair BC = Ø, otherwise RESET = Ø.
	LDDR LDIR	RESET = Ø.
Single Byte Arithmetic Group	ADC A,s ADD A,s CP s SBC A,s SUB s	SET = 1 if Overflow, otherwise RESET = Ø.
	AND s OR s XOR s	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
	DEC s	SET = 1 if operand was 8Ø(Hex.) before decrement, otherwise RESET = Ø.
	INC s	SET = 1 if Operand was 7F(Hex.) before increment, otherwise RESET = Ø.
Two Byte Arithmetic Group	ADC HL,rr SBC HL,rr	SET = 1 if Overflow, otherwise RESET = Ø.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

General Purpose Arithmetic and C.P.U. Control Group	DAA	SET = 1 if the Accumulator is Parity Even, otherwise RESET = Ø.
	NEG	SET = 1 if the Accumulator contents = 8Ø(Hex.) before negate, otherwise RESET = Ø.
Rotate and Shift Group	RL s RR s RLD RRD RLC s RRC s SLA s SRA s SRL s	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Bit Set, Reset and Test Group	BIT b,r	Not known.
Input and Output Group	IN r,(C)	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
	IND INI INDR INIR OTDR OTIR OUTD OUTI	Not known

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

Table 2.5 — Carry Flag

Instruction Group (See Ch. 4)	Instructions	Effect
Single Byte Arithmetic Group	ADC A s ADD A,s	SET = 1 if Carry from Bit 7, otherwise RESET = Ø.
	CP s SBC s SUB s	SET = 1 if no Borrow, otherwise RESET = Ø.
	AND s OR s XOR s	RESET = Ø.
Two Byte Arithmetic Group	ADC HL,rr ADD HL,rr ADD IX,rr ADD IY,rr	SET = 1 if Carry from Bit 15, otherwise RESET = Ø.
	SBC HL,rr	SET = 1 if no Borrow, otherwise RESET = Ø.
General Purpose Arithmetic and C.P.U. Control Group	CCF	SET = 1 if the C (Carry) Flag = Ø before the instruction, otherwise RESET = Ø.
	DAA	SET = 1 if Binary Coded Decimal (BCD) carry, otherwise RESET = Ø.
	NEG	SET = 1 if the contents of the Accumulator = ØØ(Hex.) before the instruction, otherwise RESET = Ø.
	SCF	SET = 1.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

Rotate and Shift Group	RL s RLC s SLA s	Set from Bit 7 of the Operand.
	RR s RRC s SRA s SRL s	Set from Bit Ø of the Operand.
	RLA RLCA	Set from Bit 7 of the Accumulator.
	RRA RRCA	Set from Bit Ø of the Accumulator.

NOTES:
b represents a specified Bit.
r represents a specified Register.
s represents a specified Operand.
rr represents a specified Register Pair.

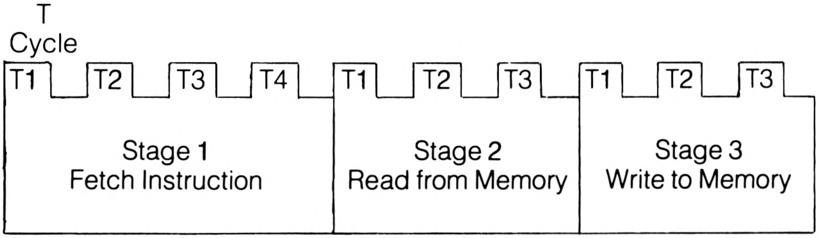
CHAPTER 3
Timing

The execution of instructions within the Z8Ø requires time which is measured in cycles. There are two types of cycle — the clock or time cycles, known as T Cycles, and a longer machine cycle, referred to as the M Cycle. T Cycles are always of the same length, and indicate the time taken for the 'clock' which is used to co-ordinate the actions of the Z8Ø to 'tick' once. They are the fundamental unit of time for the processor. Machine cycles are more abstract, each one representing the time taken for the Z8Ø to perform one particular action, such as fetching a program instruction, or writing a byte to memory. Because they can represent different actions, M Cycles can take varying amounts of time, from 3 to 6 T states (Note: this is simply another term for a T cycle). To find the actual time taken by an instruction, divide the number of T states taken by the clock rate being used. Thus, if an instruction taken 11 T states, and the Z8Ø is being run at 2 megahertz, the instruction will take 5.5 microseconds to execute. If a 2 MHz. clock is used to control the Z8Ø (as is assumed throughout this book), each T cycle will take Ø.5 microseconds to complete.

NOTE: A 4 MHz. clock will reduce the completion time of one T cycle to Ø.25 microseconds but will not necessarily halve the time required to execute any given instruction, as it may not be possible to fetch instructions and data from the memory twice as fast as they were previously being fetched.

Since the time required to execute a given instruction, or follow a loop or subroutine, can be crucial to the design and efficient running of a program, full details of the number of M and T cycles, and the processing time in microseconds (assuming a 2 MHz. clock) are given for each individual instruction code in chapter 5. Note that some conditional instructions will not always take the same amount of time to execute. Where two execution times are shown, one is for the case in which the condition is met, and the other is for the case in which the condition is not met. For instance, the instruction JR Z,1ØØØ will take 12 T states if the zero flag is set, and the jump is performed, whereas it will take 7 T states if the zero flag is not set, and the jump is not performed.

Each instruction can be considered as executing in three stages;
— fetch the instruction
— where appropriate, read from the memory
— where appropriate, write to the memory, e.g.



During stage 1 the instruction will be fetched and decoded, then any necessary processing carried out within the C.P.U. If the instruction requires a memory read, this will take place during stage 2 and, similarly, any memory write activity takes place during stage 3.

CHAPTER 4

Instruction Groups

Full details of each instruction are given in Chapter 5. However, for convenience of programming, these can be considered under a number of separate groups, each related to a specific function or activity. These Groups are:

1. Single Byte (8 Bit) Load Group.
2. Two Byte (16 Bit) Load Group.
3. Exchange, Block Transfer and Search Group.
4. Single Byte (8 Bit) Arithmetic Group.
5. Two Byte (16 Bit) Arithmetic Group.
6. Logical Group.
7. General Purpose Arithmetic and C.P.U. Control Group.
8. Rotate and Shift Group.
9. Bit Set, Reset and Test (Flag) Group.
10. Jump, Call (Subroutine) and Return Group.
11. Input and Output Group.

The following pages give a brief description of each transaction within each of these groups, each transaction being cross-referenced to full details in Chapter 5.

1. Single Byte (8 Bit) Load Group

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
LD r,r'	Dependent on value of r(Bits 5 4 3) and r'(Bits 2 1 0) 01 ← r →← r' → (Binary)		N	N	N	N	N	N	1	1	4	2	r and r' represent Registers A,B, C,D,E,H or L.	
													r and r' Bit Pattern is	
													A = 111	189
													B = 000	189
													C = 001	189
													D = 010	189
													E = 011	189
													H = 100	189
													L = 101	189
LD r, n			N	N	N	N	N	N	2	2	7	3.5		
r = A	3E n	062 n												188
r = B	06 n	006 n												188
r = C	0E n	014 n												188
r = D	16 n	022 n												188
r = E	1E n	030 n												188
r = H	26 n	038 n												188
r = L	2E n	046 n												188
LD r, (HL)			N	N	N	N	N	N	1	2	7	3.5		
r = A	7E	126												191
r = B	46	070												191
r = C	4E	078												191
r = D	56	086												191
r = E	5E	094												191
r = H	66	102												191
r = L	6E	110												191
LD r, (IX + d)			N	N	N	N	N	N	3	5	19	9.5		
r = A	DD 7E d	221 126 d												193
r = B	DD 46 d	221 070 d												193
r = C	DD 4E d	221 078 d												193
r = D	DD 56 d	221 086 d												193
r = E	DD 5E d	221 094 d												193
r = H	DD 66 d	221 102 d												193
r = L	DD 6E d	221 110 d												193
LD r, (IY + d)			N	N	N	N	N	N	3	5	19	9.5		
r = A	FD 7E d	253 126 d												193
r = B	FD 46 d	253 070 d												193
r = C	FD 4E d	253 078 d												193
r = D	FD 56 d	253 086 d												193
r = E	FD 5E d	253 094 d												193
r = H	FD 66 d	253 102 d												193
r = L	FD 6E d	253 110 d												193
LD (HL), r			N	N	N	N	N	N	1	2	7	3.5		
r = A	77	119												212
r = B	70	112												212
r = C	71	113												212
r = D	72	114												212
r = E	73	115												212
r = H	74	116												212
r = L	75	117												212
LD (IX + d), r			N	N	N	N	N	N	3	5	19	9.5		
r = A	DD 77 d	221 119 d												215
r = B	DD 70 d	221 112 d												215
r = C	DD 71 d	221 113 d												215
r = D	DD 72 d	221 114 d												215
r = E	DD 73 d	221 115 d												215
r = H	DD 74 d	221 116 d												215
r = L	DD 75 d	221 117 d												215
LD (IY + d), r			N	N	N	N	N	N	3	5	19	9.5		
r = A	FD 77 d	253 119 d												215
r = B	FD 70 d	253 112 d												215
r = C	FD 71 d	253 113 d												215
r = D	FD 72 d	253 114 d												215
r = E	FD 73 d	253 115 d												215
r = H	FD 74 d	253 116 d												215
r = L	FD 75 d	253 117 d												
LD (HL), n	36 n	054 n	N	N	N	N	N	N	2	3	10	5		211
LD (IX + d), n	DD 36 d n	221 054 d n	N	N	N	N	N	N	4	5	19	9.5		214
LD (IY + d), n	FD 36 d n	253 054 d n	N	N	N	N	N	N	4	5	19	9.5		214
LD A, (BC)	0A	010	N	N	N	N	N	N	1	2	7	3.5		186
LD A, (DE)	1A	026	N	N	N	N	N	N	1	2	7	3.5		187

SINGLE BYTE (8 BIT) LOAD GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
LD A,(nn)	3A n n	050 n n	N	N	N	N	N	N	3	4	13	6.5		185
LD (BC),A	02	002	N	N	N	N	N	N	1	2	7	3.5		210
LD (DE),A	12	018	N	N	N	N	N	N	1	2	7	3.5		210
LD (nn),A	32 n n	050 n n	N	N	N	N	N	N	3	4	13	6.5		205
LD A,I	ED 57	237 087	*	*	Ø	IFF	Ø	N	2	2	9	4.5		183
LD A,R	ED 5F	237 095	*	*	Ø	IFF	Ø	N	2	2	9	4.5		184
LD I,A	ED 47	237 071	N	N	N	N	N	N	2	2	9	4.5		195
LD R,A	ED 4F	237 079	N	N	N	N	N	N	2	2	9	4.5		196

FLAG KEY: N – Not affected.
Ø – RESET = Ø.
1 – SET = 1.
? – Unknown.
* – Affected according to the result.
IFF – Content of Interrupt Flip Flop 2 copied into flag.

LD r,r' Chapter 5, Page 189

Where:

r and r' represent any of the C.P.U. registers A, B, C, D, E, H or L.

This instruction simply loads the contents of the r' register into the r register, leaving the contents of the r' register untouched.

LD r,n Chapter 5, Page 188

Where:

r represents any of the C.P.U. registers A, B, C, D, E, H or L.
n is an 8-bit value, specified in the instruction.

This instruction loads the 8-bit value n into the register r.

LD r,(HL) Chapter 5, Page 191

Where:

r represents any of the C.P.U. registers A, B, C, D, E, H or L.

This loads the contents of a memory location, identified by the contents of register pair HL, into the register r, leaving the contents of both the memory location and register pair HL untouched.

LD r,(IX + d) Chapter 5, Page 193

Where:

r represents any of the C.P.U. registers A, B, C, D, E, H or L.
d is the displacement, in Bytes, from the location identified by the contents of Index Register IX.

This loads the contents of a memory location, identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction), into the register r, leaving the contents of both the memory location and Index Register IX untouched.

LD r,(IY + d) Chapter 5, Page 193

Where:

r represents any of the C.P.U. registers, A, B, C, D, E, H or L.

d is the displacement, in Bytes, from the location indentified by the contents of the Index Register IY.

This loads the contents of a memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction), into the register r, leaving the contents of both the memory location and Index Register IY untouched.

LD (HL), r Chapter 5, Page 212

Where:

r represents any of the C.P.U. registers, A, B, C, D, E, H or L.

This loads the contents of register r into a memory location which is identified by the contents of Register Pair HL. The contents of Register Pair HL remain untouched.

LD (IX + d),r Chapter 5, Page 215

Where:

r represents any of the C.P.U. registers A, B, C, D, E, H or L.

d is the displacement, in Bytes, from the location identified by the contents of Index Register IX.

This loads the contents of register r into a memory location, which is identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction). The contents of Index Register IX remain unaltered.

LD (IY + d),r Chapter 5, Page 215

Where:

r represents any of the C.P.U. registers A, B, C, D, E, H or L.

d is the displacement, in Bytes, from the location identified by the contents of Index Register IY.

This loads the contents of register r into a memory location, which is identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction). The contents of Index Register IY remain unaltered.

LD (HL),n Chapter 5, Page 211

Where:

n is an 8-bit value, specified in the instruction.

Loads the value n into a memory location identified by the contents of Register Pair HL.

LD (IX + d),n Chapter 5, Page 214

Where:

n is an 8-bit value, specified in the instruction.
d is the displacement, in Bytes, from the location identified by the contents of Index Register IX.

Loads the value n into a memory location, identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction).

LD (IY + d),n Chapter 5, Page 214

Where:

n is an 8-bit value, specified in the instruction.
d is the displacement, in Bytes, from the location identified by the contents of Index Register IY.

Loads the value n into a memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction).

LD A, (BC) Chapter 5, Page 186

Loads the contents of a memory location, specified by the contents of Register Pair BC, into the Accumulator, leaving the contents of the memory location untouched.

LD A, (DE) Chapter 5, Page 187

Loads the contents of a memory location, identified by the contents of Register Pair DE, into the Accumulator, leaving the contents of the memory location unaltered.

LD A, (nn) Chapter 5, Page 185

Where:

nn is a spcific memory location, identified in two bytes of the instruction.

Loads the contents of the specified memory location, nn, into the Accumulator, leaving the contents of location nn unaltered.

LD (BC),A Chapter 5, Page 210

Loads the contents of the Accumulator into a memory location identified by the contents of Register Pair BC. The contents of the Accumulator remain unchanged.

LD (DE),A Chapter 5, Page 210

Loads the contents of the Accumulator into a memory location identified by the contents of Register Pair DE, leaving the contents of the Accumulator unchanged.

LD (nn),A Chapter 5, Page 205

Where:

nn is a specific memory location, identified by two bytes of the instruction.

Loads the contents of the Accumulator into the memory location specified in the instruction, leaving the contents of the Accumulator unaltered.

LD A,I Chapter 5, Page 183

Loads the contents of the Interrupt Register I into the Accumulator, leaving the contents of Interrupt Register I untouched.

LD A,R Chapter 5, Page 184

Loads the contents of the Refresh Register 'R' into the Accumulator, leaving the contents of Refresh Register R unchanged.

LD I,A Chapter 5, Page 195

Loads the contents of the Accumulator into the Interrupt Register I, leaving the contents of the Accumulator unchanged.

LD R,A Chapter 5, Page 196

Loads the contents of the Accumulator into the Refresher Register R, leaving the contents of the Accumulator unaltered.

2. Two Byte (16 Bit) Load Group

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
LD, dd, nn			N	N	N	N	N	N	3	3	10	5		
dd = BC	01 nn	001												197
dd = DE	11 nn	017												197
dd = HL	21 nn	033												197
dd = SP	31	049												197
LD IX, nn	DD 21 nn	221 033 nn	N	N	N	N	N	N	4	4	14	7		198
LD IY, nn	FD 21 nn	253 033 nn	N	N	N	N	N	N	4	4	14	7		198
LD dd, (nn)			N	N	N	N	N	N	4	6	20	10		
dd = BC	ED 4B nn	237 075												199
dd = DE	ED 5B nn	237 091												199
dd = HL	ED 6B nn	237 107												199
dd = SP	ED 7B nn	237 123												199
LD IX (nn)	DD 2A nn	221 042 nn	N	N	N	N	N	N	4	6	20	10		201
LD IY, (nn)	FD 2A nn	253 042 nn	N	N	N	N	N	N	4	6	20	10		201
LD (nn), dd			N	N	N	N	N	N	4	6	20	10		
dd = BC	ED 43 nn	237 067 nn												206
dd = DE	ED 53 nn	237 083 nn												206
dd = HL	ED 63 nn	237 099 nn												206
dd = SP	ED 73 nn	237 115 nn												206
LD (nn), IX	DD 22 nn	221 034 nn	N	N	N	N	N	N	4	6	20	10		208
LD (nn), IY	FD 22 nn	253 034 nn	N	N	N	N	N	N	4	6	20	10		208
LD SP, HL	F9	249	N	N	N	N	N	N	1	1	6	3		203
LD, SP, IX	DD F9	221 249	N	N	N	N	N	N	2	2	10	5		204
LD SP, IY	FD F9	253 249	N	N	N	N	N	N	2	2	10	5		204
PUSH rr			N	N	N	N	N	N	1	3	11	5.5		
rr = AF	F5	245												246
rr = BC	C5	197												246
rr = DE	D5	213												246
rr = HL	E5	229												246
PUSH IX	DD E5	221 229	N	N	N	N	N	N	2	4	15	7.5		248
PUSH IY	FD E5	253 229	N	N	N	N	N	N	2	.4	15	7.5		248
POP rr			N	N	N	N	N	N	1	3	10	5		
rr = AF	F1	241												242
rr = BC	C1	193												242
rr = DE	D1	209												242
rr = HL	E1	225												242
POP IX	DD E1	221 225	N	N	N	N	N	N	2	4	14	7		244
POP IY	FD E1	253 225	N	N	N	N	N	N	2	4	14	7		244

FLAG KEY N - Not affected.
Ø - Reset = Ø.
1 - Set = 1.
? - Unknown.
• - Affected according to the result.
IFF - Content of Interrupt Flip Flop copied into flag.

LD dd,nn Chapter 5, Page 197

Where:

dd is any of the register pairs BC, DE, HL or SP.
nn is a specific memory location.

Loads the memory location nn into the Register Pair dd.

LD IX,nn Chapter 5, Page 198

Where:

nn is a specific memory location.

Loads the contents of memory location nn, specified in the instruction, into the Low Order byte of Index Register IX and the contents of memory location nn+1 into the High Order byte of Index Register IX.

LD IY,nn Chapter 5, Page 198

Where:

nn is a specific memory location.

Loads the contents of the memory location nn, specified in the instruction, into the Low Order byte of Index Register IY and the contents of memory location nn+1 into the High Order byte of Index Register IY.

LD dd,(nn) Chapter 5, Page 199

Where:

dd is any of the register pairs BC, DE, HL or SP.
nn is a specific memory location.

Loads the contents of memory location nn (specified in the instruction) into the Low Order byte of the specified Register Pair and the contents of memory location nn+1 into the High Order byte of the same Register Pair. The contents of both memory locations remain unchanged.

LD IX,(nn) Chapter 5, Page 201

Where:

nn is a specific memory location.

Loads the contents of memory location nn, which is specified in the instruction, into the Low Order byte of Index Register IX and the contents of memory location nn+1 into the High Order byte of the same register. The contents of both memory locations remain unchanged.

LD IY,(nn) Chapter 5, Page 201

Where:

nn is a specific memory location.

Loads the contents of memory location nn, specified in the instruction, into the Low Order byte of Index Register IY and the contents of memory location nn+1 into the High Order byte of that register, leaving the contents of both memory locations unaltered.

LD (nn),dd Chapter 5, Page 206

Where:

nn is a specific memory location.
dd is any one of the Register Pairs BC, DE, HL or SP.

Loads the contents of the Low Order byte of the nominated Register Pair into memory location nn, and the contents of the High Order byte of the same Register Pair into memory location nn+1. The contents of the Register Pair are not affected.

LD (nn),IX Chapter 5, Page 208

Where:

nn is a specified memory location.

Loads the contents of the Low Order byte of Index Register IX into memory location nn and the contents of the High Order byte of the same register into memory location nn+1. The contents of Index Register IX remain unchanged.

LD (nn),IY Chapter 5, Page 208

Where:

nn is a specified memory location.

Loads the contents of the Low Order byte of Index Register IY into memory location nn and the contents of the High Order byte of the same register into memory location nn+1. The Index Register contents are not changed.

LD SP,HL Chapter 5, Page 203

Loads the Stack Pointer with the contents of Register Pair HL, but does not change the contents of Register Pair HL.

LD SP,IX Chapter 5, Page 204

Loads the Stack Pointer with the contents of Index Register IX, leaving the contents of that register unchanged.

LD SP,IY Chapter 5, Page 204

Loads the Stack Pointer with the contents of Index register IY, leaving the contents of that register unaltered.

PUSH rr Chapter 5, Page 246

Where:

rr is any of the Register Pairs AF, BC, DE or HL.

Pushes the contents of the nominated Register Pair on to the memory stack. The Stack Pointer (SP), which contains the address of the top of the memory stack, is decremented and the High Order byte of the Register Pair is pushed out to that location. The Stack Pointer is again decremented and the Low Order byte of the Register Pair is pushed out to this new location. The contents of the Register Pair are not changed.

PUSH IX Chapter 5, Page 248

Pushes the contents of the Index Register IX on to the memory stack. The Stack Pointer (SP), which contains the address of the top of the memory stack, is decremented and the High Order byte of register

IX is pushed out to that location. The Stack Pointer is again decremented and the Low Order byte of Index Register IX is pushed out to the new location. The contents of Index Register IX are not affected.

PUSH IY Chapter 5, Page 248

Pushes the contents of the Index Register IY on to the memory stack. The Stack Pointer (SP), which contains the address of the top of the memory stack, is decremented and the High Order byte of Index Register IY is pushed out to that location. The Stack Pointer is again decremented and the Low Order byte of Index Register IY pushed out to that new location. The contents of Index Register IY remain unaltered

POP rr Chapter 5, Page 242

Where:

rr is any of the register pairs AF, BC, DE or HL.

Loads the contents of the memory location identified by the Stack Pointer into the Low Order byte of the nominated Register Pair. The Stack Pointer is then incremented and the contents of the location now identified by the Stack Pointer is loaded into the High Order byte of the same Register Pair. Finally, the Stack Pointer is again incremented.

POP IX Chapter 5, Page 244

Loads the contents of the memory location identified by the Stack Pointer into the Low Order byte of Index Register IX. The Stack Pointer is then incremented and the contents of this new location loaded into the High Order byte of the IX Index Register. The Stack Pointer is once again incremented.

POP IY Chapter 5, Page 244

Loads the contents of the memory location identified by the Stack Pointer into the Low Order byte of Index Register IY. The Stack Pointer is then incremented and the contents of that location loaded into the High Order byte of Index Register IY. The Stack Pointer is then incremented once more.

3. Exchange, Block Transfer and Search Group

This group of instructions allows the exchange of 16 bit data blocks between register pairs in the same set of registers AND between the two sets of registers. It also includes instructions which transfer data from one block of memory to another and those which search a specified block of memory.

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
EX DE, HL	EB	235	N	N	N	N	N	N	1	1	4	2		149
EX AF, AF'	08	008	N	N	N	N	N	N	1	1	4	2		148
EXX	D9	217	N	N	N	N	N	N	1	1	4	2		154
EX (SP), HL	E3	227	N	N	N	N	N	N	1	5	19	9.5		150
EX (SP), IX	DD E3	221 227	N	N	N	N	N	N	2	6	23	11.5		152
EX (SP), IY	FD E3	253 227	N	N	N	N	N	N	2	6	23	11.5		152
LDD	ED A8	237 168	N	N	Ø	•	Ø	N	2	4	16	8		217
LDDR	ED B8	237 184	N	N	Ø	Ø	Ø	N	2	5	21	11.5	If BC ≠ Ø	219
										4	16	8	If BC = Ø	
LDI	ED A0	237 160	N	N	Ø	•	Ø	N	2	4	16	8		221
LDIR	ED B0	237 176	N	N	Ø	Ø	Ø	N	2	5	21	11.5	If BC ≠ Ø	223
										4	16	8	If BC = Ø	
CPD	ED A9	237 169	•	•	•	•	1	N	2	4	16	8		129
CPDR	ED B9	237 185	•	•	•	•	1	N	2	5	21	10.5	If BC ≠ Ø and A ≠ (HL)	130
										4	16	8	If BC = Ø or A = (HL)	
CPI	ED A1	237 161	•	•	•	•	1	N	2	4	16	8		132
CPIR	ED B1	237 177	•	•	•	•	1	N	2	5	21	10.5	If BC ≠ Ø and A ≠ (HL)	133
										4	16	8	If BC = Ø or A = (HL)	

FLAG KEY:		
	N	- Not affected.
	Ø	- RESET = Ø.
	1	- SET = 1.
	?	- Unknown.
	•	- Affected according to the result.
	IFF	- Content of Interrupt Flip Flop copied into flag.

A. Exchange Instructions

EX DE,HL Chapter 5, Page 149

Exchanges the contents of the DE and HL Register Pairs.

EX AF,AF' Chapter 5, Page 148

Exchanges the contents of Register Pair AF with Register Pair AF'.

EXX Chapter 5, Page 154

The contents of Register Pairs BC, DE and HL are exchanged with the contents of Register Pairs BC', DE', and HL' respectively.

EX (SP),HL Chapter 5, Page 150

The Low Order byte of Register Pair HL (i.e. the contents of Register L) is exchanged with the contents of the memory location whose address is contained in the Stack Pointer (SP). The High Order byte of Register Pair HL is exchanged with the contents of the next sequential memory location. The contents of the Stack Pointer are not changed.

EX (SP),IX Chapter 5, Page 152

Exchanges the Low Order byte of Index Register IX with the memory location whose address is contained in the Stack Pointer (SP) and the High Order byte of that register is exchanged with the next memory location. The contents of the Stack Pointer are not altered.

EX (SP),IY Chapter 5, Page 152

The contents of the Low Order byte of Index Register IY are exchanged with the memory location whose address is contained in the Stack Pointer (SP) and the High order byte of the register is exchanged with the next sequential memory location. The contents of the Stack Pointer are not changed.

B. Transfer Instructions

LDD Chapter 5, Page 217

Transfers one byte of date from the memory location whose address is held in register Pair HL to the memory location whose address is held in Register Pair DE. Register Pair BC is used as a byte counter. All three register pairs (BC, DE and HL) are then decremented.

LDDR Chapter 5, Page 219

Transfers one byte of data from the memory location whose address is held in Register Pair HL to the memory location whose address is held in Register Pair DE. Register Pair BC is used as a byte counter. The three Register Pairs are then decremented. If Register Pair BC becomes zero, then the instruction is terminated, otherwise the Program Counter is decremented by 2 and the instruction is repeated.

WARNING: If Register Pair BC is initially set to zero, the instruction will loop through all 64K of memory.

LDI Chapter 5, Page 221

Transfers one byte of data from the memory location whose address is held in Register Pair HL to the memory location whose address is held in Register Pair DE. Register Pair BC is used as a byte counter. Register Pairs DE and HL are then incremented while Register Pair BC is decremented.

LDIR Chapter 5, Page 223

Transfers one byte of data from the memory location whose address is held in Register Pair HL to the memory location whose address is held in Register Pair DE. Register Pair BC is used as a byte counter. Register Pairs DE and HL are then incremented while Register Pair BC is decremented. If Register Pair BC becomes zero then the instruction is terminated, otherwise the Program Counter (PC) is decremented by 2 and the instruction is repeated.

WARNING: If Register Pair BC is initially set to zero, the instruction will loop through 64K of memory.

6. Search Instructions

CPD Chapter 5, Page 129

Compares the contents of the Accumulator with the contents of the memory location whose address is contained in Register Pair HL. If the contents match Condition Flag Z is set, otherwise it is reset. The contents of Register Pair HL are decremented as are the contents of Register Pair BC (used as a byte counter).

CPDR Chapter 5, Page 130

Compares the contents of the Accumulator with the contents of the memory location whose address is contained in Register Pair HL. If the contents match Condition Flag Z is set, otherwise it is reset. The contents of both Register Pair HL and Register Pair BC (used as a byte counter) are decremented. If either a match has been achieved, or the new value of Register Pair BC is zero, the instruction is terminated. If neither of these conditions are met the Program Counter (PC) is decremented by 2 and the instruction is repeated.

NOTE: Execution of this instruction increments the Program Counter (PC) by 2, therefore failure of the tests returns the Program Counter to the start of the CPDR instruction.

WARNING: If Register Pair BC is initialised to zero, this instruction will loop until either a match is found or it has cycled through all 64K of memory. It can therefore be used to test all 64K of memory.

CPI Chapter 5, Page 132

Compares the contents of the Accumulator with the contents of the memory location whose address is contained in Register Pair HL. If the conditons match Condition Flag Z is set, otherwise it is reset. The contents of Register Pair HL are incremented while the contents of Register Pair BC (used as a byte counter) are decremented.

CPIR Chapter 5, Page 133

Compares the contents of the Accumulator with the contents of the memory location whose address is contained in Register Pair HL. If the contents match, then Condition Flag Z is set, otherwise it is reset. The contents of Register Pair HL are incremented while the contents of Register Pair BC (used as a byte counter) are decremented. If either a match has been achieved, or the new value of Register Pair BC is zero, the instruction is terminated. If neither of these conditions are met the Program Counter (PC) is decremented by 2 and the instruction is repeated.

NOTE: Execution of this instruction increments the Program Counter (PC) by 2, therefore failure of both tests returns the Program Counter to the start of the CPIR instruction.

WARNING: If Register Pair BC is initialised to zero, this instruction will loop through until either a match is found or it has cycled through all 64K of memory. It can be used to test the entire memory.

4. Single Byte (8 Bit) Arithmetic Group

SINGLE BYTE (8 BIT) ARITHMETIC GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
ADC A, n	CE n	206	•	•	•	V	Ø	•	2	2	7	3.5	Adds with Carry	71
ADC A, r			•	•	•	V	Ø	•	1	1	4	2	Adds with Carry	
r = A	8F	143												73
r = B	88	136												74
r = C	89	137												74
r = D	8A	138												74
r = E	8B	139												74
r = H	8C	140												74
r = L	8D	141												74
ADC A, (HL)	8E	142	•	•	•	V	Ø	•	1	2	7	3.5		76
ADC A, (IX + d)	DD 8E d	221 142 d	•	•	•	V	Ø	•	3	5	19	9.5		78
ADC A, (IY + d)	FD 8E d	253 142 d	•	•	•	V	Ø	•	3	5	19	9.5		78
ADD A, n	C6 n	198 n	•	•	•	V	Ø	•	2	2	7	3.5		82
ADD A, r			•	•	•	V	Ø	•	1	1	4	2		
r = A	87	135												83
r = B	80	128												83
r = C	81	129												83
r = D	82	130												83
r = E	83	131												83
r = H	84	132												83
r = L	85	133												83
ADD A, (HL)	86	134	•	•	•	V	Ø	•	1	2	7	3.5		85
ADD A, (IX + d)	DD 86 d	221 134 d	•	•	•	V	Ø	•	3	5	19	9.5		86
ADD A, (IY + D)	FD 86 D	253 134 D	•	•	•	V	Ø	•	3	5	19	9.5		86
DEC d														
d = A	3D	061							1	1	4	2		138
d = B	05	005							1	1	4	2		138
d = C	OD	013							1	1	4	2		138
d = D	15	021							1	1	4	2		138
d = E	1D	029							1	1	4	2		138
d = H	25	037							1	1	4	2		138
d = L	2D	045							1	1	4	2		138
DEC (HL)	35	053	•	•	•	V	I	N	1	3	11	5.5		140
DEC (IX + d)	DD 35 d	221 053 d	•	•	•	V	I	N	3	6	23	11.5		141
DEC (IY + d)	FD 35 d	253 053 d	•	•	•	V	I	N	3	6	23	11.5		141
INC r			•	•	•	V	Ø	N	1	1	4	2		
r = A	3C	060												162
r = B	04	004												162
r = C	OC	012												162
r = D	14	020												162
r = E	1C	028												162
r = H	24	036												162
r = L	2C	044												162
INC (HL)	34	052	•	•	•	V	Ø	N	1	3	11	5.5		165
INC (IX + d)	DD 34 d	221 052 d	•	•	•	V	Ø	N	3	6	23	11.5		166
INC (IY + d)	FD 34 d	253 052 d	•	•	•	V	Ø	N	3	6	23	11.5		166
SBC A, n	DE n	222 n	•	•	•	V	1	•	2	2	7	3.5	Subtract with Carry	301
SBC A, r			•	•	•	V	1	•	1	1	4	2	Subtract with Carry	
r = A	9F	159												302
r = B	98	152												303
r = C	99	153												303
r = D	9A	154												303
r = E	9B	155												303
r = H	9C	156												303
r = L	9D	157												303
SBC A, (HL)	9E	158	•	•	•	V	1	•	1	2	7	3.5		305
SBC A, (IX + d)	DD 9E d	221 158 d	•	•	•	V	1	•	3	5	19	9.5		307
SBC A, (IY + d)	FD 9E d	253 158 d	•	•	•	V	1	•	3	5	19	9.5		307
SUB n	D6 n	214 n	•	•	•	V	1	•	2	2	7	3.5		334
SUB r			•	•	•	V	1	•	1	1	4	2		
r = A	97	151												336
r = B	90	144												337
r = C	91	145												337
r = D	92	146												337

SINGLE BYTE (8 BIT) ARITHMETIC GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
r = E	93	147												337
r = H	94	148												337
r = L	95	149												337
SUB (HL)	96	150	•	•	•	V	1	•	1	2	7	3.5		339
SUB (IX + d)	DD 96 d	221 150 d	•	•	•	V	1	•	3	5	19	9.5		341
SUB (IY + d)	FD 96 d	253 150 d	•	•	•	V	1	•	3	5	19	9.5		341

FLAG KEY:		
	N	- Not affected
	P	- Contains the Parity of the result (1 = Parity Even)
	V	- Contains the Overflow of the result (1 = Overflow)
	Ø	- RESET = Ø
	1	- SET = 1
	?	- Unknown
	•	- Affected according to the result
	IFF	- Content of Interrupt Flip Flop copied into flag.

ADC A,n Chapter 5, Page 71

Where:

n is an 8-bit value, specified in the instruction.
Adds the value n to the Accumulator, with Carry.

ADC A,r Chapter 5, Page 73

Where:

r represents any one of the single byte registers A, B, C, D, E, H or L.

Adds the contents of the specified register to the Accumulator, with Carry.

ADC A,(HL) Chapter 5, Page 76

Adds the contents of the memory location whose address is contained in Register Pair HL, to the Accumulator, with Carry.

ADC A,(IX + d) Chapter 5, Page 78

Where:

d is the displacement, in bytes, from the location identified by the contents of Index Register IX.

Adds, with Carry, the contents of a memory location, identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction) into the Accumulator. The contents of the memory location remain unaltered.

ADC A,(IY + d) Chapter 5, Pages 00

Where:

d is the displacement, in bytes, from the location identified by the contents of Index Register IY.

Adds, with Carry, the contents of a memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) into the Accumulator. The contents of the memory location remain unchanged.

ADD A,n Chapter 5, Page 82

Where:

n is an 8-bit value, specified in the instruction.

Adds n to the Accumulator.

ADD A,r Chapter 5, Page 83

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Adds the contents of the register specified in the instruction to the Accumulator. The register remains unchanged.

ADD A,(HL) Chapter 5, Page 85

Adds the contents of the memory location whose address is contained in Register Pair HL to the Accumulator. The contents of the location remain unaltered.

ADD A,(IX + d) Chapter 5, Page 86

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IX.

Adds the contents of a memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) to the Accumulator. The contents of the memory location remain unchanged.

ADD A,(IY + d) Chapter 5, Page 86

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IY.

Adds the contents of a memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) to the Accumulator. The contents of the memory location remain unaltered.

DEC r Chapter 5, Page 138

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Decrements the contents of the specified register by 1.

DEC (HL) Chapter 5, Page 140

Where:

Decrements by **1** the contents of the memory location whose address is held in Register Pair HL.

DEC (IX + d) Chapter 5, Page 141

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IX.

Decrements by **1** the contents of a memory location, identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction).

DEC (IY + d) Chapter 5, Page 141

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IY.

Decrements, by **1**, the contents of a memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction).

INC r Chapter 5, Page 162

Where:

r represents any one of the Registers A, B, C, D, E, H or L..

Increments the contents of the specified register by **1**.

INC (HL) Chapter 5, Page 165

Increments by **1** the contents of a memory location whose address is held in Register Pair HL.

INC (IX + d) Chapter 5, Page 166

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IX.

Increments by **1** the contents of a memory location, identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction).

INC (IY + d) Chapter 5, Page 166

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IY.

Increments, by 1, the contents of a memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction).

SBC A,n Chapter 5, Page 301

Where:

n is a single byte integer, specified in the instruction.

Subtracts n, and the Carry Flag, from the Accumulator.

SBC A,r Chapter 5, Page 302

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Subtracts the contents of the register specified in the instruction, and the Carry Flag, from the Accumulator. The contents of the register are not changed.

SBC A,(HL) Chapter 5, Page 305

Subtracts the contents of the memory location whose address is contained in Register Pair HL, and the Carry Flag, from the Accumulator. The contents of Register Pair HL are unchanged.

SBC A,(IX + d) Chapter 5, Page 307

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IX.

Subtracts the contents of the memory location, identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction), and the Carry Flag, from the Accumulator. The contents of the memory location and Index Register IX remain unchanged.

SBC A,(IY + d) Chapter 5, Page 307

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IY.

Subtracts the contents of the memory location, identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction), and the Carry Flag, from the Accumulator. The contents of the memory location and Index Register IY are not altered.

SUB n Chapter 5, Page 334

Where:

n is a single byte integer, specified in the instruction.

Subtracts the integer n from the Accumulator.

SUB r Chapter 5, Page 336

Where:

r represents any one of the registers A, B, C, D, E, H or L

Subtracts the contents of the register specified in the instruction from the Accumulator. The contents of the register remain unchanged.

SUB (HL) Chapter 5, Page 339

Subtracts the contents of the memory location whose address is contained in Register Pair HL from the Accumulator. The contents of the memory location are not changed.

SUB (IX + d) Chapter 5, Page 341

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IX.

Subtracts the contents of the memory location identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction) from the Accumulator. The contents of the memory location are unchanged.

SUB (IY + d) Chapter 5, Page 341

Where:

d is the displacement, in bytes, from the memory location identified by the contents of Index Register IY.

Subtracts the contents of the memory location identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) from the Accumulator. The contents of the memory location remain unaltered.

5. Two Byte (16 Bit) Arithmetic Group

TWO BYTE (16 BIT) ARITHMETIC GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
ADC HL, ss			•	•	•	•	0	•	2	4	15	7.5		
ss = BC	ED 4A	237 74												80
ss = DE	ED 5A	237 90												80
ss = HL	ED 6A	237 106												80
ss = SP	ED 7A	237 122												80
SBC HL, ss			•	•	•	•	1	•	2	4	15	7.5		
ss = BC	ED 42	237 66												309
ss = DE	ED 52	237 82												309
ss = HL	ED 62	237 98												309
ss = SP	ED 72	237 114												309
ADD HL, ss			N	N	•	N	Ø	•	1	3	11	5.5		
ss = BC	09	009												88
ss = DE	19	025												88
ss = HL	29	041												88
ss = SP	39	057												88
ADD IX,pp			N	N	•	N	Ø	•	2	4	15	7.5		
pp = BC	DD 09	221 009												89
pp = DE	DD 19	221 025												90
pp = IX	DD 29	221 041												91
pp = SP	DD 39	221 057												93
ADD IY, rr			N	N	•	N	Ø	•	2	4	15	7.5		
rr = BC	FD 09	253 009												89
rr = DE	FD 19	253 025												90
rr = IY	FD 29	253 041												92
rr = SP	FD 39	253 057												93
DEC ss			N	N	N	N	N	N	1	1	6	3		
ss = BC	OB	011												143
ss = DE	IB	027												143
ss = HL	2B	043												143
ss = SP	3B	059												143
DEC IX	DD 2B	221 043	N	N	N	N	N	N	2	2	10	5		144
DEC IY	FD 2B	253 043	N	N	N	N	N	N	2	2	10	5		144
INC ss			N	N	N	N	N	N	1	1	6	3		
ss = BC	03	003												164
ss = DE	13	019												164
ss = HL	23	035												164
ss = SP	33	051												164
INC IX	DD 23	221 035	N	N	N	N	N	N	2	2	10	5		168
INC IY	FD 23	253 035	N	N	N	N	N	N	2	2	10	5		168

FLAG KEY: N - Not affected.
Ø - Reset = Ø.
1 - Set = 1.
? - Unknown.
• - Affected according to the result.

ADC HL,ss Chapter 5, Page 80

Where:

ss represents any one of the Register Pairs BC, DE, HL or SP.

Adds the contents of the nominated Register Pair to the HL Register Pair with carry. If the nominated Register Pair is BC, DE or SP its contents remain unaltered.

ADD HL, ss Chapter 5, Page 88

Where:

ss represents any one of the Register Pairs BC, DE, HL or SP.

Adds the contents of the nominated Register Pair to the HL register pair. If the nominated Register Pair is BC, DE or SP its contents are unaltered.

ADD IX, rr Chapter 5, Page 89

Where:

pp represents any one of the Register Pairs BC, DE, SP, or Index Register IX.

Adds the contents of the nominated Register Pair to Index Register IX. If the Register pair BC, DE or SP is nominated, the contents of that Register Pair are unchanged.

ADD IY,rr Chapter 5, Page 89

Where:

rr represents any one of the Register Pairs BC, DE or SP, or Index Register IY.

Adds the contents of the nominated Register Pair to Index Register IY. If Register Pair BC, DE or SP is nominated, the contents of that Register Pair are not changed.

SBC HL,ss Chapter 5, Page 309

Where:

ss represents any one of the Register Pairs BC, DE, HL, or SP.

Subtracts the contents of the nominated Register Pair plus the carry, from the HL Register Pair. If the nominated Register Pair is BC, DE, or SP, its contents remain unaltered.

DEC ss Chapter 5, Page 143

Where:

ss represents any one of the Register Pairs BC, DE, HL or SP.

Decrements the contents of the nominated Register Pair.

DEC IX Chapter 5, Page 144

Decrements Index Register IX.

DEC IY Chapter 5, Page 144

Decrements Index Register IY.

INC ss Chapter 5, Page 164

Where:

ss represents any one of the Register Pairs BC, DE, HL or SP.

Increments the contents of the nominated Register Pair.

INC IX Chapter 5, Page 168

Increments the contents of Index Register IX.

INC IY Chapter 5, Page 168

Increments the contents of Index Register IY.

6. Logical Group

LOGICAL GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
AND n	E6 n	230 n	•	•	1	P	Ø	Ø	2	2	7	3.5		94
AND r			•	•	1	P	Ø	Ø	1	1	4	2		
r = A	A7	167												95
r = B	AO	160												95
r = C	A1	161												95
r = D	A2	162												95
r = E	A3	163												95
r = H	A4	164												95
r = L	A5	165												95
AND (HL)	A6	166	•	•	1	P	Ø	Ø	1	2	7	3.5		98
AND (IX + d)	DD A6 d	221 166 d	•	•	1	P	Ø	Ø	3	5	19	9.5		99
AND (IY + d)	FD A6 d	253 166 d	•	•	1	P	Ø	Ø	3	5	19	9.5		99
CP n	FE n	n	•	•	•	V	1	•	2	2	7	3.5		122
CP r			•	•	•	V	1	•	1	1	4	2		
r = A	BF	181												123
r = B	B8	184												124
r = C	B9	185												124
r = D	BA	186												124
r = E	BB	187												124
r = H	BC	188												124
r = L	BD	189												124
CP (HL)	BE	190	•	•	•	V	1	•	1	2	7	3.5		126
CP (IX + d)	DD BE d	221 190 d	•	•	•	V	1	•	3	5	19	9.5		127
CP (IY + d)	FD BE d	253 190 d	•	•	•	V	1	•	3	5	19	9.5		127
OR n	F6 n	246 n	•	•	1	P	Ø	Ø	2	2	7	3.5		227
OR r			•	•	1	P	Ø	Ø	1	1	4	2		
r = A	B7	183												229
r = B	BO	176												229
r = C	B1	177												229
r = D	B2	178												229
r = E	B3	179												229
r = H	B4	180												229
r = L	B5	181												229
OR (HL)	B6	182	•	•	1	P	Ø	Ø	1	2	7	3.5		231
OR (IX + d)	DD B6 d	221 182 d	•	•	1	P	Ø	Ø	3	5	19	9.5		233
OR (IY + d)	FD B6 d	253 182 d	•	•	1	P	Ø	Ø	3	5	19	9.5		233
XOR n	EE n	238 n	•	•	1	P	Ø	Ø	2	2	7	3.5		343
XOR r			•	•	1	P	Ø	Ø	1	1	4	2		
r = A	AF	175												345
r = B	A8	168												347
r = C	A9	169												347
r = D	AA	170												347
r = E	AB	171												347
r = H	AC	172												347
r = L	AD	173												347
XOR (HL)	AE	174	•	•	1	P	Ø	Ø	1	2	7	3.5		349
XOR (IX + d)	DD AE d	221 174 d	•	•	1	P	Ø	Ø	3	5	19	9.5		351
XOR (IY + d)	FD AE d	253 174 d	•	•	1	P	Ø	Ø	3	5	19	9.5		351

FLAG KEY:		
	N	- Not affected.
	P	- Contains the Parity of the result (1 = Parity Even).
	V	- Contains the Overflow of the result (1 = Overflow).
	Ø	- RESET = Ø.
	1	- SET = 1.
	?	- Unknown.
	•	- Affected according to the result.

The AND instruction compares a specified operand, bit by bit, with the Accumulator. For each bit position, if either operand or Accumulator is Ø, then Ø is placed in that bit position in the Accumulator. If a bit position in both the operand and the Accumulator contain a **1**, then a **1** is placed in that bit position in the Accumulator. The prime use of the AND instruction is to mask out unwanted bits in a field.

AND n Chapter 5, Page 94

Where:

n represents a single byte, specified in the instruction.

Performs a Logical AND on the contents of the Accumulator with n and stores the result in the Accumulator.

AND r Chapter 5, Page 95

Where:

r represents any one of the registers A, B, C, D, E, H or L

Performs a Logical AND on the contents of the Accumulator, with the contents of the nominated register, and stores the result in the Accumulator. The contents of that register are not changed.

AND (HL) Chapter 5, Page 98

Performs a Logical AND on the contents of the Accumulator, with the contents of the memory location whose address is contained in Register Pair HL and stores the result in the Accumulator. The contents of the memory location are not changed.

AND (IX + d) Chapter 5, Page 99

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Performs a Logical AND on the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction) and stores the result in the Accumulator. The contents of the memory location remain unaltered.

AND (IY + d) Chapter 5, Page 99

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Performs a Logical AND on the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) and stores the result in the Accumulator. The contents of the memory location are not changed.

The COMPARE (CP) instructions compare a specified operand with the contents of the Accumulator and, if the two bytes are equal (i.e. a TRUE condition exists) then a Flag is set.

CP n Chapter 5, Page 122

Where:

n is a single byte, specified in the instruction.

Compares the contents of the Accumulator with n. If a TRUE condition exists a Flag is set. The contents of the Accumulator are not altered.

CP A Chapter 5, Page 123

Compares the contents of the Accumulator with itself. Since a TRUE condition must always exist this is a convenient method of setting a particular Flag. The contents of the Accumulator are not changed.

CP r Chapter 5, Page 124

Where:

r represents any one of the registers B, C, D, E, H or L.

Compares the contents of the Accumulator with the contents of the register nominated in the instruction. If a TRUE condition exists a Flag is set. The contents of the nominated register and the Accumulator remain unchanged.

CP (HL) Chapter 5, Page 126

Compares the contents of the Accumulator with the contents of a memory location whose address is held in Register Pair HL. If a TRUE condition exists, a Flag is set.

CP (IX + d) Chapter 5, Page 127

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Compares the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction). If a TRUE condition exists, a Flag is set.

CP (IY + d) Chapter 5, Page 127

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Compares the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction). If a TRUE condition exists, a Flag is set.

The OR instruction compares a specified operand, bit by bit, with the Accumulator. For each bit position, if either the operand or the Accumulator is 1, then the result is always 1. This instruction can be used to set any number of bits to 1.

OR n Chapter 5, Page 227

Where:

n is a single byte, specified in the instruction.

Performs a Logical OR on the contents of the Accumulator with n and stores the result in the Accumulator.

OR r Chapter 5, Page 229

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Performs a Logical OR on the contents of the Accumulator with the contents of the nominated register and stores the result in the Accumulator. The contents of the register are not altered.

OR (HL) Chapter 5, Page 231

Performs a Logical OR on the contents of the Accumulator with the contents of the memory location whose address is contained in Register Pair HL and stores the result in the Accumulator. The contents of the memory location remain unchanged.

OR (IX + d) Chapter 5, Page 233

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Performs a Logical OR on the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction) and stores the result inthe Accumulator. The contents of the memory location are not changed.

OR (IY + d) Chapter 5, Page 233

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Performs a Logical OR on the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) and stores the result in the Accumulator. The contents of the memory location remain unchanged.

The Exclusive OR (XOR) instruction differs from the OR instruction in only one respect. It compares a specified operand, bit by bit, with the Accumulator and, as for the OR instruction, if either the operand or Accumulator value for a bit position is 1, then the result is 1. However, unlike the OR instruction, if BOTH operand and Accumulator have a value of 1 in the same bit position, then the result is Ø.

XOR n Chapter 5, Page 343

Where:

n is a single byte, specified in the instruction.

Performs a Logical XOR on the contents of the Accumulator with n and stores the result in the Accumulator.

XOR r Chapter 5, Page 345

Where:

r represents any one of the registers A, B, C, D, E, H or L

Performs a Logical XOR on the contents of the Accumulator with the contents of the nominated register and stores the result in the Accumulator. If the nominated register is B, C, D, E, H or L the contents of that register are not changed.

XOR (HL) Chapter 5, Page 349

Performs a Logical XOR on the contents of the Accumulator with the contents of the memory location whose address is contained in Register Pair HL and stores the result in the Accumulator. The contents of the memory location are not changed.

XOR (IX + d) Chapter 5, Page 351

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Performs a Logical XOR on the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction) and stores the result in the Accumulator. The contents of the memory location remain unaltered.

XOR (IY + d) Chapter 5, Page 351

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Performs a Logical XOR on the contents of the Accumulator with the contents of the memory location identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) and stores the result in the Accumulator. The contents of the memory location are not changed.

7. General Purpose Arithmetic and C.P.U. Control Group

All instructions in this Group are implied addressing instructions.

GENERAL PURPOSE ARITHMETIC AND C.P.U. CONTROL GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
CCF	3F	063	N	N	?	N	Ø	•	1	1	4	2		121
CPL	2F	047	N	N	1	N	1	N	1	1	4	2		135
DAA	27	039	•	•	•	P	N	•	1	1	4	2		136
DI	F3	243	N	N	N	N	N	N	1	1	4	2		145
EI	FB	251	N	N	N	N	N	N	1	1	4	2		147
HALT	76	118	N	N	N	N	N	N	1	1	4	2		155
IM Ø	ED 46	237 070	N	N	N	N	N	N	2	2	8	4		156
IM 1	ED 56	237 086	N	N	N	N	N	N	2	2	8	4		157
IM 2	ED 5E	237 094	N	N	N	N	N	N	2	2	8	4		158
NEG	ED 44	237 068	•	•	•	V	1	•	2	2	8	4		225
NOP	00	000	N	N	N	N	N	N	1	1	4	2		226
SCF	37	055	•	•	Ø	•	Ø	1	1	1	4	2		311

FLAG KEY		
	N	- Not affected.
	P	- Contains the Parity of the result (1 = Parity Even).
	V	- Contains the Overflow of the result (1 = Overflow).
	Ø	- RESET = Ø.
	1	- SET = 1.
	?	- Unknown.
	•	- Affected according to the result.

CCF Chapter 5, Page 121

Complements (i.e. reverses) the Carry bit C in the Flag Register.

CPL Chapter 5, Page 135

Complements the entire contents of the Accumulator.

DAA Chapter 5, Page 136

The Accumulator is decimal adjusted to obtain the correct representation for Binary Coded Decimal (BCD).

DI Chapter 5, Page 145

Resets the Interruptable Flip-Flops, disabling all maskable interrupts.

EI Chapter 5, Page 147

Sets the Interruptable Flip-Flops, enabling the maskable interrupt function. The maskable interrupt function is not enabled until this instruction is completed.

HALT Chapter 5, Page 155

Suspends operation of the CPU, until interrupt or reset is received.

NOTE: The CPU NOP's so that memory refresh continues until interrupt or reset is received.

IM Ø Chapter 5, Page 156

Sets the Interrupt Mode Ø allowing an interrupting device to insert an instruction code on the data bus for immediate execution.

IM 1 Chapter 5, Page 157

Sets Interrupt Mode 1, allowing the CPU to execute a restart to Location ØØ38H (Hexadecimal) when an interrupt takes place.

IM 2 Chapter 5, Page 158

Sets Interrupt Mode 2. A memory address is placed on to the address bus, the lower order byte being supplied by the interrupting device and the higher order byte being the contents of the Interrupt Vector Register I. A CALL to this address is then executed by the CPU.

NEG Chapter 5, Page 225

Negates the contents of the Accumulator, equivalent to subtracting those contents from zero.

NOP Chapter 5, Page 226

No Operation. Nothing is done for one machine cycle.

SCF Chapter 5, Page 311

Sets the Carry Flag C in the Flag Register F.

8. Rotate and Shift Group

ROTATE AND SHIFT GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO.	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ		
RL r			•	•	Ø	P	Ø	•	2	2	8	4		
r = A	CB 17	203 023												263
r = B	CB 10	203 016												263
r = C	CB 11	203 017												263
r = D	CB 12	203 018												263
r = E	CB 13	203 019												263
r = H	CB 14	203 020												263
r = L	CB 15	203 021												263
RLA	17	023	N	N	Ø	N	Ø	•	1	1	4	2		269
RL (HL)	CB 16	203 022	•	•	Ø	P	Ø	•	2	4	15	7.5		265
RL (IX + d)	DD CB d 16	221 203 d 022	•	•	Ø	P	Ø	•	4	6	23	11.5		267
RL (IY + d)	FD CB d 16	253 203 d 022	•	•	Ø	P	Ø	•	4	6	23	11.5		267
RLC r			•	•	Ø	P	Ø	•	2	2	8	4		
r = A	CB 07	203 007												271
r = B	CB 00	203 000												271
r = C	CB 01	203 001												271
r = D	CB 02	203 002												271
r = E	CB 03	203 003												271
r = H	CB 04	203 004												271
r = L	CB 05	203 005												271
RLCA	07	07	N	N	0	N	0	•	1	1	4	2		277
RLC (HL)	CB 06	203 006	•	•	Ø	P	Ø	•	2	4	15	7.5		273
RLC (IX + d)	DD CB d 06	221 203 d 006	•	•	Ø	P	Ø	•	4	6	23	11.5		275
RLC (IY + d)	FD CB d 06	253 203 d 006	•	•	Ø	P	Ø	•	4	6	23	11.5		275
RLD	ED 6F	237 111	•	•	Ø	P	Ø	N	2	5	18	9		279
RR r			•	•	Ø	P	Ø	•	2	2	8	4		
r = A	CB 1F	203 031												281
r = B	CB 18	203 024												281
r = C	CB 19	203 025												281
r = D	CB 1A	203 026												281
r = E	CB 1B	203 027												281
r = H	CB 1C	203 028												281
r = L	CB 1D	203 029												281
RRA	1F	31	N	N	0	N	0	•	1	1	4	2		287
RR (HL)	CB 1E	203 030	•	•	Ø	P	Ø	•	2	4	15	7.5		283
RR (IX + d)	DD CB d IE	221 203 d 030	•	•	Ø	P	Ø	•	4	6	23	11.5		285
RR (IY + d)	FD CB d IE	253 203 d 030	•	•	Ø	P	Ø	•	4	6	23	11.5		285
RRC r			•	•	Ø	P	Ø	•	2	2	8	4		
r = A	CB 0F	203 015												289
r = B	CB 08	203 008												289
r = C	CB 09	203 009												289
r = D	CB 0A	203 010												289
r = E	CB 0B	203 011												289
r = H	CB 0C	203 012												289
r = L	CB 0D	203 013												289
RRCA	0F	15	N	N	0	N	0	•	1	1	4	2		295
RRC (HL)	CB 0E	203 014	•	•	Ø	P	Ø	•	2	4	15	7.5		291
RRC (IX + d)	DD CB d 0E	221 203 d 014	•	•	Ø	P	Ø	•	4	6	23	11.5		293
RRC (IY + d)	FD CB d 0E	253 203 d 014	•	•	Ø	P	Ø	•	4	6	23	11.5		293
RRD	ED 67	237 103	•	•	Ø	P	Ø	N	2	5	18	9		297
SLA r			•	•	Ø	P	Ø	•	2	2	8	4		
r = A	CB 27	203 039												316
r = B	CB 20	203 032												316
r = C	CB 21	203 033												316
r = D	CB 22	203 034												316
r = E	CB 23	203 035												316
r = H	CB 24	203 036												316
r = L	CB 25	203 037												316
SLA (HL)	CB 26	203 038	•	•	Ø	P	Ø	•	2	4	15	7.5		318
SLA (IY + d)	FD CB d 26	253 203 d 038	•	•	Ø	P	Ø	•	4	6	23	11.5		
SRA r			•	•	Ø	P	Ø	•	2	2	8	4		
r = A	CB 2F	203 047												322
r = B	CB 28	203 040												322
r = C	CB 29	203 041												322
r = D	CB 2A	203 042												322
r = E	CB 2B	203 043												322
r = H	CB 2C	203 044												322
r = L	CB 2D	203 045												322

ROTATE AND SHIFT GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
SRA (HL)	CB 2E	203 046	•	•	Ø	P	Ø	•	2	4	15	7.5		324
SRA (IX + d)	DD CB d 2E	221 203 d 046	•	•	Ø	P	Ø	•	4	6	23	11.5		326
SRA (IY + d)	FD CB d 2E	253 203 d 046	•	•	Ø	P	Ø	•	4	6	23	11.5		326
SRL r			•	•	Ø	P	Ø	•	2	2	8	4		
r = A	CB 3F	203 063												328
r = B	CB 38	203 056												328
r = C	CB 39	203 057												328
r = D	CB 3A	203 058												328
r = E	CB 3B	203 059												328
r = H	CB 3C	203 060												328
r = L	CB 3D	203 061												328
SRL (HL)	CB 3E	203 062	•	•	Ø	P	Ø	•	2	4	15	7.5		330
SRL (IX + d)	DD CB d 3E	221 203 d 062	•	•	Ø	P	Ø	•	4	6	23	11.5		332
SRL (IY + d)	FD CBd 3E	253 203 d 062	•	•	Ø	P	Ø	•	4	6	23	11.5		332

FLAG KEY: N - Not affected.
P - Contains the Parity of the result (1 = Parity Even).
V - Contains the Overflow of the result (1 = Overflow).
Ø - RESET = Ø.
1 - SET = 1.
? - Unknown.
• - Affected according to the result.

RLA Chapter 5, Page 269

Where:

This has the same effect as RL A, although it is slightly faster. This instruction is included to retain compatibility with the Intel 8Ø8Ø processor.

RL r Chapter 5, Page 263

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Rotates the contents of the nominated register Left. The content of Bit 7 is placed in the Carry Flag (C in the Flag Register) and the previous content of C is placed in Bit Ø of the nominated register.

RL (HL) Chapter 5, Page 265

Rotates Left the contents of the memory location, whose address is contained in Register Pair HL. The content of Bit 7 is placed in the Carry Flag (C in the Flag Register) and the previous content of C is placed in Bit Ø of the memory location.

RL (IX + d) Chapter 5, Page 267

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Rotates Left the contents of the memory location identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction). The content of Bit 7 is placed in the Carry Flag (C in the Flag Register) and the previous content of C is placed in Bit Ø of the memory location.

RL (IY + d) Chapter 5, Page 267

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Rotates Left the contents of the memory location identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction). The content of Bit 7 is placed in the Carry Flag (C in the Flag Register) and the previous content of C is placed in Bit Ø of the memory location.

RLCA Chapter 5, Page 277

Where:

This has the same effect as RLC A, although it is slightly faster. This instruction is included to retain compatibility with the Intel 8Ø8Ø processor.

RLC r Chapter 5, Page 271

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Rotates Left the contents of the nominated register. Bit 7 is placed in both the Carry Flag (C in the Flag Register) and the Bit Ø position.

RLC (HL) Chapter 5, Page 273

Rotates Left the contents of the memory location whose address is contained in Register Pair HL. The content of Bit 7 is placed in both the Carry Flag (C in the Flag Register) and the Bit Ø position.

RLC (IX + d) Chapter 5, Page 275

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Rotates Left the contents of the memory location whose address is identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction). The content of Bit 7 is placed in both the Carry Flag (C in the Flag Register) and the Bit Ø position.

RLC (IY + d) Chapter 5, Page 275

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Rotates Left the contents of the memory location whose address is identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction). The content of Bit 7 is placed in both the Carry Flag (C in the Flag Register) and the Bit Ø position.

RLD Chapter 5, Page 279

Rotates the contents of a memory location, whose address is held in Register Pair HL, with the Accumulator as follows:

1. The Lower Order four bits (Ø to 3) of the memory location are placed in the Higher Order four bit positions (4 to 7) of the same location.
2. The Higher Order four bits (4 to 7) of the memory location are placed in the Lower Order four bits (Ø to 3) of the Accumulator.
3. The Lower Order four bits (Ø to 3) of the Accumulator are placed in the Lower Order four bits of the memory location.

NOTE: This instruction has no affect on the Higher Order four bits (4 to 7) of the Accumulator.

RR r Chapter 5, Page 281

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Rotates Right the contents of the register nominated in the instruction. The content of Bit Ø is placed in the Carry Flag (C in the Flag Register) while the previous content of C is placed in Bit 7 of the nominated register.

RRA Chapter 5, Page 287

Where:

This has the same effect as RR A, although it is slightly faster. This instruction is included to retain compatibility with the Intel 8Ø8Ø processor.

RR (HL) Chapter 5, Page 283

Rotates Right the contents of the memory location whose address is contained in Register Pair HL. The content of Bit Ø is placed in the Carry Flag (C in the Flag Register) while the previous content of C is placed in Bit 7 of the memory location.

RR (IX + d) Chapter 5, Page 285

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Rotates Right the contents of the memory location identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction). The content of Bit Ø is placed in the Carry Flag (C in the Flag Register) while the previous content of C is placed in Bit 7 of the memory location.

RR (IY + d) Chapter 5, Page 285

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Rotates Right the contents of the memory location identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction). The content of Bit Ø is placed in the Carry Flag (C in the Flag Register) while the previous content of C is placed in Bit 7 of the memory location.

RRCA Chapter 5, Page 295

Where:

This has the same effect as RRC A, although it is slightly faster. This instruction is included to retain compatibility with the Intel 8Ø8Ø processor.

RRC r Chapter 5, Page 289

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Rotates Right the contents of the register nominated in the instruction. The content of Bit Ø is placed in both the Carry Flag (C in the Flag Register) and Bit 7 of the nominated register.

RRC (HL) Chapter 5, Page 291

Rotates Right the contents of the memory location whose address is contained in Register Pair HL. The content of Bit Ø is placed in both the Carry Flag (C in the Flag Register) and Bit 7 of the memory location.

RRC (IX + d) Chapter 5, Page 293

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Rotates Right the contents of the memory location whose address is identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction). The content of Bit Ø is placed in both the Carry Flag (C in the Flag Register) and Bit 7 of the memory location.

RRC (IY + d) Chapter 5, Page 293

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Rotates Right the contents of the memory location whose address is identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction). The content of Bit Ø is placed in both the Carry Flag (C in the Flag Register) and Bit 7 of the memory location.

RRD Chapter 5, Page 297

Rotates the contents of a memory location, whose address is held in Register Pair HL, as follows:

1. Places the Lower Order four bits (Ø to 3) of the memory location into the Lower Order four bit positions of the Accumulator.

2. Places the previous contents of the Lower Order four bits (Ø to 3) of the Accumulator into the Higher Order four bits (4 to 7) of the memory location.

3. Places the original contents of the Higher Order four bits (4 to 7) of the memory location into the Lower Order four bits (Ø to 3) of the same location.

NOTE: This instruction has no effect on the Higher Order four bits (4 to 7) of the Accumulator.

SLA r Chapter 5, Page 316

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Shifts Left the contents of the register nominated in the instruction as follows:

1. Bit Ø is Reset to Ø.

2. Bits 1 to 6 are Shifted Left one position.

3. The previous content of Bit 7 is placed in the Carry Flag (C in the Flag Register).

SLA (HL) Chapter 5, Page 318

Shifts Left the contents of the memory location whose address is held in Register Pair HL as follows:

1. Bit Ø is Reset to Ø.
2. Bits 1 to 6 are Shifted Left one position.
3. The previous content of Bit 7 is placed in the Carry Flag (C in the Flag Register).

SLA (IX + d) Chapter 5, Page 320

Where:

d is the displacement, in bytes from the memory location whose address is identified by the contents of Index Register IX.

Shifts Left the contents of the memory location whose address is identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction), as follows:

1. Bit Ø is Reset to Ø.
2. Bits 1 to 6 are Shifted Left one position.
3. The previous content of Bit 7 is placed in the Carry Flag (C in the Flag Register).

SLA (IY + d) Chapter 5, Page 320

Where:

d is the displacement, in bytes from the memory location whose address is identified by the contents of Index Register IY.

Shifts Left the contents of the memory location whose address is identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction), as follows:

1. Bit Ø is Reset to Ø.
2. Bits 1 to 6 are Shifted Left one position.
3. The previous content of Bit 7 is placed in the Carry Flag (C in the Flag Register).

SRA r Chapter 5, Page 322

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Shifts Right the contents of the register nominated in the instruction as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. The original content of Bit position 7 remains unaltered.
3. The original content of Bit position Ø is placed in the Carry flag (C in the Flag Register).

SRA (HL) Chapter 5, Page 324

Shifts Right the contents of the memory location whose address is held in Register Pair HL as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. The original content of Bit position 7 remains unchanged.
3. The original content of Bit position Ø is placed in the Carry Flag (C in the Flag Register).

SRA (IX + d) Chapter 5, Page 326

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Shifts Right the contents of the memory location whose address is identified by the contents of Register IX (modified by displacement d, which is specified in the instruction) as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. The original content of Bit position 7 remains unaltered.
3. The original content of Bit position Ø is placed in the Carry Flag (C in the Flag Register).

SRA (IY + d) Chapter 5, Page 326

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Shifts Right the contents of the memory location whose address is identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. The original content of Bit position 7 remains unchanged.
3. The original content of Bit position Ø is placed in the Carry Flag (C in the Flag Register).

SRL r Chapter 5, Page 328

Where:

r represents any one of the registers A, B, C, D, E, H or L.

Shifts Right the contents of the register nominated in the instruction as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. Bit position 7 is Reset to Ø.
3. The original content of Bit position Ø is placed in the Carry Flag (C in the Flag Register).

SRL (HL) Chapter 5, Page 330

Shifts Right the contents of the memory location whose address is held in Register Pair HL as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. Bit position 7 is Reset to Ø.
3. The original content of Bit position Ø is placed in the Carry Flag (C in the Flag Register).

SRL (IX + d) Chapter 5, Page 332

Where:

d is the displacement, in bytes, fromthe memory location whose address is identified by the contents of Index Register IX.

Shifts Right the contents of the memory location whose address is identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction) as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. Bit position 7 is Reset to Ø.
3. The original content of Bit position Ø is placed in the Carry Flag (C in the Flag Register).

SRL (IY + d) Chapter 5, Page 332

Where:

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Shifts Right the contents of the memory location whose address is identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction) as follows:

1. The contents of Bit positions 1 to 7 are Shifted Right one position.
2. Bit position 7 is Reset to Ø.
3. The original content of Bit position Ø is placed in the Carry Flag (C in the Flag Register).

9. Bit Set, Reset and Test (Flag) Group.

These instructions either Set, Reset or Test one of the Bits in a specified CPU register or, alternatively, a particular memory location.

BIT SET, RESET AND TEST (FLAG) GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH 5 REF
BIT b, r			?	•	1	?	Ø	N	2	2	8	4		
r = A, b = Ø	CB 47	203 071												101
b = 1	CB 4F	203 079												101
b = 2	CB 57	203 087												101
b = 3	CB 5F	203 095												101
b = 4	CB 67	203 103												101
b = 5	CB 6F	203 111												101
b = 6	CB 77	203 119												101
b = 7	CB 7F	203 127												101
r = B, b = Ø	CB 40	203 064												101
b = 1	CB 48	203 072												101
b = 2	CB 50	203 080												101
b = 3	CB 58	203 088												101
b = 4	CB 60	203 096												101
b = 5	CB 68	203 104												101
b = 6	CB 70	203 112												101
b = 7	CB 78	203 120												101
r = C, b = Ø	CB 41	203 065												101
b = 1	CB 49	203 073												101
b = 2	CB 51	203 081												101
b = 3	CB 59	203 089												101
b = 4	CB 61	203 097												101
b = 5	CB 69	203 105												101
b = 6	CB 71	203 113												101
b = 7	CB 79	203 121												101
r = D, b = Ø	CB 42	203 066												101
b = 1	CB 4A	203 074												101
b = 2	CB 52	203 082												101
b = 3	CB 5A	203 090												101
b = 4	CB 62	203 098												101
b = 5	CB 6A	203 106												101
b = 6	CB 72	203 114												101
b = 7	CB 7A	203 112												101
r = E, b = Ø	CB 43	203 067												101
b = 1	CB 4B	203 075												101
b = 2	CB 53	203 083												101
b = 3	CB 5B	203 091												101
b = 4	CB 63	203 099												101
b = 5	CB 6B	203 107												101
b = 6	CB 73	203 115												101
b = 7	CB 7B	203 123												101
r = H, b = Ø	CB 44	203 068												101
b = 1	CB 4C	203 076												101
b = 2	CB 54	203 084												101
b = 3	CB 5C	203 092												101
b = 4	CB 64	203 100												101
b = 5	CB 6C	203 108												101
b = 6	CB 74	203 116												101
b = 7	CB 7C	203 124												101
r = L, b = Ø	CB 45	203 069												101
b = 1	CB 4D	203 077												101
b = 2	CB 55	203 085												101
b = 3	CB 5D	203 093												101
b = 4	CB 65	203 101												101
b = 5	CB 6D	203 109												101
b = 6	CB 75	203 117												101
b = 7	CB 7D	203 125												101
BIT b, (HL)			?	•	1	?	Ø	N	2	3	12	6		
b = Ø	CB 46	203 070												103
b = 1	CB 4E	203 078												103
b = 2	CB 56	203 086												103
b = 3	CB 5E	203 094												103
b = 4	CB 66	203 102												103
b = 5	CB 6E	203 110												103
b = 6	CB 76	203 118												103
b = 7	CB 7E	203 126												103
BIT b, (IX + D)			?	•	1	?	Ø	N	4	5	20	10		
b = Ø	DD CB d 46	221 203 d 070												105
b = 1	DD CB d 4E	221 203 d 078												105
b = 2	DD CB d 56	221 203 d 086												105
b = 3	DD CA d 5E	221 203 d 094												105

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
b = 4	DD CB d 66	221 203 d 102												105
b = 5	DD CB d 6E	221 203 d 110												105
b = 6	DD CB d 76	221 203 d 118												105
b = 7	DD CB d 7E	221 203 d 126												105
BIT b, (IY + D)			?	*	1	?	Ø	N	4	5	20	10		
b = Ø	FD CB d 46	253 203 d 070												105
b = 1	FD CB d 4E	253 203 d 078												105
b = 2	FD CB d 56	253 203 d 086												105
b = 3	FD CB d 5E	253 203 d 094												105
b = 4	FD CB d 66	253 203 d 102												105
b = 5	FD CB d 6E	253 203 d 110												105
b = 6	FD CB d 76	253 203 d 118												105
b = 7	FD CB d 7E	253 203 d 126												105
RES b, r			N	N	N	N	N	N	2	2	8	4		
r = A, b = Ø	CB 87	203 135												250
b = 1	CB 8F	203 143												250
b = 2	CB 97	203 151												250
b = 3	CB 9F	203 159												250
b = 4	CB A7	203 167												250
b = 5	CB AF	203 175												250
b = 6	CB B	203 183												250
b = 7	CB BF	203 191												250
r = B, b = Ø	CB 80	203 128												250
b = 1	CB 88	203 136												250
b = 2	CB 90	203 144												250
b = 3	CB 98	203 152												250
b = 4	CB AO	203 160												250
b = 5	CB A8	203 168												250
b = 6	CB BO	203 176												250
b = 7	CB B8	203 184												250
r = C, b = Ø	CB 81	203 129												250
b = 1	CB 89	203 137												250
b = 2	CB 91	203 145												250
b = 3	CB 99	203 153												250
b = 4	CB A1	203 161												250
b = 5	CB A9	203 169												250
b = 6	CB B1	203 177												250
b = 7	CB B9	203 185												250
r = D, b = Ø	CB 82	203 130												250
b = 1	CB 8A	203 138												250
b = 2	CB 92	203 146												250
b = 3	CB 9A	203 154												250
b = 4	CB A2	203 162												250
b = 5	CB AA	203 170												250
b = 6	CB B2	203 178												250
b = 7	CB BA	203 186												250
r = E, b = Ø	CB 83	203 131												250
b = 1	CB 8B	203 139												250
b = 2	CB 93	203 147												250
b = 3	CB 9B	203 155												250
b = 4	CB A3	203 163												250
b = 5	CB AB	203 171												250
b = 6	CB B3	203 179												250
b = 7	CB BB	203 187												250
r = H, b = Ø	CB 84	203 132												250
b = 1	CB 8C	203 140												250
b = 2	CB 94	203 148												250
b = 3	CB 9C	203 156												250
b = 4	CB A4	203 164												250
b = 5	CB AC	203 172												250
b = 6	CB B4	203 180												250
b = 7	CB BC	203 188												250
r = L, b = Ø	CB 85	203 133												250
b = 1	CB 8D	203 141												250
b = 2	CB 95	203 149												250
b = 3	CB 9D	203 157												250
b = 4	CB A5	203 165												250
b = 5	CB AD	203 173												250
b = 6	CB B5	203 181												250
b = 7	CB BD	203 189												250
RES b, (HL)			N	N	N	N	N	N	2	4	15	7.5		
b = Ø	CB 86	203 134												251
b = 1	CB 8E	203 142												251
b = 2	CB 96	203 150												251
b = 3	CB 9E	203 158												251
b = 4	CB A6	203 166												251
b = 5	CB AE	203 174												251

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
b = 6	CB B6	203 182												251
b = 7	CB BE	203 190												251
RES b,(IX + d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	DD CB d 86	221 203 d 134												253
b = 1	DD CB d 8E	221 203 d 142												253
b = 2	DD CB d 96	221 203 d 150												253
b = 3	DD CB d 9E	221 203 d 158												253
b = 4	DD CB d A6	221 203 d 166												253
b = 5	DD CB d AE	221 203 d 174												253
b = 6	DD CB d B6	221 203 d 182												253
b = 7	DD CB d BE	221 203 d 190												253
RES b,(IY + d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	FD CB d 86	253 203 d 134												253
b = 1	FD CB d 8E	253 203 d 142												253
b = 2	FD CB d 96	253 203 d 150												253
b = 3	FD CB d 9E	253 203 d 158												253
b = 4	FD CB d A6	253 203 d 166												253
b = 5	FD CB d AE	253 203 d 174												253
b = 6	FD CB d B6	253 203 d 182												253
b = 7	FD CB d BE	253 203 d 190												253
SET b, r			N	N	N	N	N	N	2	2	8	4		
r = A, b = Ø	CB C7	203 199												312
b = 1	CB CF	203 207												312
b = 2	CB D7	203 215												312
b = 3	CB DF	203 223												312
b = 4	CB E7	203 231												312
b = 5	CB EF	203 239												312
b = 6	CB F7	203 247												312
b = 7	CB FF	203 255												312
r = B, b = Ø	CB CO	203 192												312
b = 1	CB C8	203 200												312
b = 2	CB DO	203 208												312
b = 3	CB D8	203 216												312
b = 4	CB EO	203 224												312
b = 5	CB E8	203 232												312
b = 6	CB FO	203 240												312
b = 7	CB F8	203 248												312
r = C, b = Ø	CB C1	203 193												312
b = 1	CB C9	203 201												312
b = 2	CB D1	203 209												312
b = 3	CB D9	203 217												312
b = 4	CB E1	203 225												312
b = 5	CB E9	203 233												312
b = 6	CB F1	203 241												312
b = 7	CB F9	203 249												312
r = D, b = Ø	CB C2	203 194												312
b = 1	CB CA	203 202												312
b = 2	CB D2	203210												312
b = 3	CB DA	203 218												312
b = 4	CB E2	203 226												312
b = 5	CB EA	203 234												312
b = 6	CB F2	203 242												312
b = 7	CB FA	203 250												312
r = E, b = Ø	CB C3	203 195												312
b = 1	CB CB	203 203												312
b = 2	CB D3	203 211												312
b = 3	CB DB	203 219												312
b = 4	CB E3	203 227												312
b = 5	CB EB	203 235												312
b = 6	CB F3	203 243												312
b = 7	CB FB	203 251												312
r = H, b = Ø	CB C4	203 196												312
b = 1	CB CC	203 204												312
b = 2	CB D4	203 212												312
b = 3	CB DC	203 220												312
b = 4	CB E4	203 228												312
b = 5	CB EC	203 236												312
b = 6	CB F4	203 244												312
b = 7	CB FC	203 252												312
r = L, b = Ø	CB C5	203 197												312
b = 1	CB CD	203 205												312
b = 2	CB D5	203 213												312
b = 3	CB DD	203 221												312
b = 4	CB E5	203 229												312
b = 5	CB ED	203 237												312
b = 6	CB F5	203 245												312
b = 7	CB FD	203 253												312

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
SET b, (HL)			N	N	N	N	N	N	2	4	15	7.5		
b = Ø	CB C6	203 198												313
b = 1	CB CE	203 206												313
b = 2	CB D6	203 214												313
b = 3	CB DE	203 222												313
b = 4	CB E6	203 230												313
b = 5	CB EE	203 238												313
b = 6	CB F6	203 246												313
b = 7	CB FE	203 254												313
SET b,(IX + d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	DD CB d C6	221 203 d 198												314
b = 1	DD CB d CE	221 203 d 206												314
b = 2	DD CB d D6	221 203 d 214												314
b = 3	DD CB d DE	221 203 d 222												314
b = 4	DD CB d E6	221 203 d 230												314
b = 5	DD CB d EE	221 203 d 238												314
b = 6	DD CB d F6	221 203 d 246												314
b = 7	DD CB d FE	221 203 d 254												314
SET b,(IY + d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	FD CB d C6	253 203 d 198												314
b = 1	FD CB d CE	253 203 d 206												314
b = 2	FD CB d D6	253 203 d 214												314
b = 3	FD CB d DE	253 203 d 222												314
b = 4	FD CB d E6	253 203 d 230												314
b = 5	FD CB d EE	253 203 d 238												314
b = 6	FD CB d F6	253 203 d 246												314
b = 7	FD CB d FE	253 203 d 254												314

FLAG KEY:		
	N	- Not affected.
	P	- Contains the Parity of the result (1 = Parity Even).
	V	- Contains the Overflow of the result (1 = Overflow).
	Ø	- RESET = Ø.
	1	- SET = 1.
	?	- Unknown.
	•	- Affected according to the result.

BIT b,r Chapter 5, Page 101

Where:

b specifies the bit position concerned.

r identifies one of the registers A, B, C, D, E, H or L.

This instruction tests the specified bit in the nominated register and Sets/Resets the Z Flag in the Flag Register to the COMPLEMENT of that bit.

BIT b, (HL) Chapter 5, Page 103

Where:

b specifies the bit position to be tested.

Tests the specified bit in a memory location whose address is held in the Register Pair HL then Sets/Resets the Z Flag in the Flag Register to the COMPLEMENT of that bit.

BIT b, (IX + d) Chapter 5, Page 105

Where:

b specifies the bit position concerned.

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Tests the specified bit in a memory location whose address is identified by he contents of Index Register IX (modified by displacement d, which is specified in the instruction) then Sets/Resets the Z Flag in the Flag Register to the COMPLEMENT of that bit.

BIT b,(IY + d) Chapter 5, Page 107

Where:

b specifies the bit position concerned.

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Tests the specified bit in a memory location whose address is identified by contents of Index Register IY (modified by displacement d, which is specified in the instruction) then Sets/Resets the Z Flag in the Flag Register to the COMPLEMENT of that bit.

RES b,r Chapter 5, Page 250

Where:

b specifies the bit position required.

r represents one of the registers A, B, C, D, E, H or L.

Resets to Ø the specified Bit in the register nominated in the instruction.

RES b,(HL) Chapter 5, Page 251

Where:

b specifies the bit position required.

Resets to Ø the specified bit in the memory location whose address is held in the Register Pair HL.

RES b,(IX + d) Chapter 5, Page 253

Where:

b specifies the bit position required.

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Resets to Ø the specified bit in the memory location whose address is identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction).

RES b,(IY + d) Chapter 5, Page 253

Where:

b specifies the bit position required.

d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Resets to Ø the specified bit in the memory location whose address is indentified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction).

SET b,r Chapter 5, Page 312

Where:

b specifies the bit position required.
r represents one of the registers A, B, C, D, E, H or L.

Sets to 1 the specified bit in the Register nominated in the instruction.

SET b,(HL) Chapter 5, Page 313

Where:

b specifies the bit position required.

Sets to 1 the specified bit in the memory location whose address is held in Register Pair HL.

SET b,(IX + d) Chapter 5, Page 314

Where:

b specifies the bit position required.
d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Sets to 1 the specified bit in the memory location whose address is identified by the contents of Index Register IX (modified by displacement d, which is specified in the instruction).

SET b,(IY + d) Chapter 5, Page 314

Where:

b specifies the bit position required.
d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IY.

Sets to 1 the specified bit in the memory location whose address is identified by the contents of Index Register IY (modified by displacement d, which is specified in the instruction).

10. Jump, Sub-Routine Call and Return Group

JUMP instructions transfer control to another location in memory but do not save the contents of the Program Counter (PC) to identify where the jump occurred.

CALL instructions also transfer control to another memory location but save the original contents of the Program Counter in the Memory Stack.

RETURN instructions transfer the contents of the top of the Memory Stack to the Program Counter, thus returning control to the location where the CALL instruction occurred.

JUMP, (SUB-ROUTINE) CALL AND RETURN GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
CALL pq	CD pq	205 pq	N	N	N	N	N	N	3	5	17	8.5		109
CALL cc, pq			N	N	N	N	N	N	3	5	17	8.5	If cc is true	
										3	10	5	If cc is false	
cc = NZ	C4 pq	196 pq												117
cc = Z	CC pq	204 pq												116
cc = NC	D4 pq	212 pq												112
cc = C	DC pq	220 pq												111
cc = PO	E4 pq	228 pq												120
cc = PE	EC pq	236 pq												119
cc = P	F4 pq	244 pq												113
cc = M	FC pq	252 pq												115
DJNZ e	10 e-2	16 e-2	N	N	N	N	N	N	2	2	8	4	If Register B = Ø	146
										3	13	6.5	If Register B ≠ Ø	
JP nn	C3 nn	195 nn	N	N	N	N	N	N	3	3	10	5		175
JP cc, pq			N	N	N	N	N	N	3	3	10	5		
cc = NZ	C2 qp	194 qp												178
cc = Z	CA qp	202 qp												178
cc = NC	D2 qp	210 qp												178
cc = C	DA qp	218 qp												178
cc = PO	E2 qp	226 qp												178
cc = PE	EA qp	234 qp												178
cc = P	F2 qp	242 qp												178
cc = M	FA qp	250 qp												178
JP (HL)	E9	233	N	N	N	N	N	N	1	1	4	2		176
JP (IX)	DD E9	221 233	N	N	N	N	N	N	2	2	8	4		177
JP (IY)	FD E9	253 233	N	N	N	N	N	N	2	2	8	4		177
JR e	18 e-2	024 e-2	N	N	N	N	N	N	2	3	12	6		
JR C, e	38 e-2	056 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	180
										2	7	3.5	If condition not met	181
JR NC, e	30 e-2	048 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	
										2	7	3.5	If condition not met	181
JR NZ, e	20 e-2	032 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	
										2	7	3.5	If condition not met	181
JR Z, e	28 e-2	040 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	
										2	7	3.5	If condition not met	181
RET	C9	201	N	N	N	N	N	N	1	3	10	5		225
RET cc			N	N	N	N	N	N	1	3	11	5.5	If cc is true	
										1	5	2.5	If cc is false	
cc = NZ	C0	192												257
cc = Z	C8	200												257
cc = NC	D0	208												257
cc = C	D8	216												257
cc = PO	E0	224												257
cc = PE	E8	232												257
cc = P	F0	240												257
cc = M	F8	248												257
RET I	ED 4D	237 077	N	N	N	N	N	N	2	4	14	7		259
RET N	ED 45	237 069	N	N	N	N	N	N	2	4	14	7		261
RST P			N	N	N	N	N	N	1	3	11	5.5		
p = 00														
(Hex.)	C7	199												299
p = 08														
(Hex.)	CF	207												299
p = 10														
(Hex.)	D7	215												299
p = 18														
(Hex.)	DF	223												299
p = 20														
(Hex.)	E7	231												299
p = 28														
(Hex.)	EF	239												299
p = 30														
(Hex.)	F7	247												299
p = 38														
(Hex.)	FF	255												299

FLAG KEY: N – Not affected.

CALL pq Chapter 5, Page 109

Where:

p is the Lower Order byte of the address to which control is to be transferred.

q is the Higher Order byte of the address to which control is to be transferred.

Pushes the contents of the Program Counter (PC) on to the top of the Memory Stack then loads address pq into the Program Counter. This calls the subroutine which starts at memory address pq.

NOTE: To return from the subroutine, a RET instruction must be included in the subroutine code.

CALL cc,pq Chapter 5, Page 111-120

Where:

cc specifies the condition which must be met for the Call to become effective, based on the following table:

Condition		**cc (Bin.)**	**Flag**
Non-zero	NZ	ØØØ	Z
Zero	Z	ØØ1	Z
Non-Carry	NC	Ø1Ø	C
Carry	C	Ø11	C
Parity Odd	PO	1ØØ	P/V
Parity Even	PE	1Ø1	P/V
Sign Positive	P	11Ø	S
Sign Negative	M	111	S

p is the Lower Order byte of the address to which control is to be transferred.

q is the Higher Order byte of the address to which control is to be transferred.

Provided condition cc is TRUE, Pushes the contents of the Program Counter (PC) to the top of the Memory Stack then loads pq into the Program Counter. If Condition cc is NOT TRUE, the Program Counter is incremented and the program continues.

NOTE: A RET instruction must be included in the subroutine code to return control to the main program.

DJNZ e Chapter 5, Page 146

Where:

e is the displacement required if the Jump instruction is to be followed.

NOTE: The initial value of the second byte of this instruction must be e-2.

Decrements register B and Jumps if the result is Non-Zero, when e is added to the Program Counter (PC) giving the address to which control is to be transferred. If the contents of register B are Zero, the Jump does not take place and the program continues with the next instruction.

JP nn Chapter 5, Page 175

Where:

nn is a memory location specified in the instruction.

Jumps unconditionally to memory location nn, where the next instruction is held.

JP cc,pq Chapter 5, Page 178

Where:

cc specifies the condition which must be met for the Jump to become effective, based on the following table:

Condition		**cc (Bin.)**	**Flag**
Non-Zero	NZ	ØØØ	Z
Zero	Z	ØØ1	Z
Non-Carry	NC	Ø1Ø	C
Carry	C	Ø11	C
Parity Odd	PO	1ØØ	P/V
Parity Even	PE	1Ø1	P/V
Sign Positive	P	11Ø	S
Sign Negative	M	111	S

p is the Lower Order byte of the address to which control is to be transferred.

q is the Higher Order byte of the address to which control is to be transferred.

Provided Condition cc is TRUE, loads pq into the Program Counter (PC). If condition cc is False the Program Counter is incremented to the next sequential instruction.

JP (HL) Chapter 5, Page 176

Jumps unconditionally to the memory location whose address is held in Register Pair HL, i.e. the contents of HL are loaded into the Program Counter (PC).

JP (IX) Chapter 5, Page 177

Jumps unconditionally to the memory location whose address is held in Index Register IX, i.e. the contents of IX are loaded into the Program Counter (PC).

JP (IY) Chapter 5, Page 177

Jumps unconditionally to the memory location whose address is held in Index Register IY, i.e. the contents of IY are loaded into the Program Counter (PC).

JR e Chapter 5, Page 180

Where:

e is the displacement required from the current contents of the Program Counter (PC).

Adds e to the Program Counter (PC), the next instruction being fetched from the location identified by the new contents of the Program Counter.

JR C,e Chapter 5, Page 181

Where:

e is the displacement from the current contents of the Program Counter (PC) required if the Jump instruction is to be followed.

JR NC,e Chapter 5, Page 181

Where:

e is the displacement from the current contents of the Program Counter (PC) required if the Jump instruction is to be followed.

If the Carry Flag C = 1, the program continues to the next instruction and the Jump does not occur. If the Carry Flag C = Ø, e is added to the Program Counter (PC) and the next instruction is fetched from the !ocation identified by the new contents of the Program Counter.

JR NZ,e Chapter 5, Page 181

Where:

e is the displacement from the current contents of the Program Counter (PC) required if the Jump instruction is to be followed.

If the Zero Flag Z = 1 the program continues to the next instruction and the Jump does not occur. If the Zero Flag Z = Ø, e is added to the Program Counter (PC) and the next instruction is fetched from the location identified by the new contents of the Program Counter.

JR Z,e Chapter 5, Page 181

Where:

e is the displacement from the current contents of the Program Counter (PC) required if the Jump instruction is to be followed.

If the Zero Flag Z = Ø the program continues to the next instruction and the Jump does not occur. If the Zero Flag Z = 1, e is added to the Program Counter (PC) and the next instruction is fetched from the location identified by the new contents of the Program Counter.

RET Chapter 5, Page 255

Returns program control to the main program after a subroutine has been executed. Loads the Lower Order byte of the Program Counter (PC) with the contents of the memory location whose address is identified by the Stack Pointer (SP) and the Higher Order byte of the Program Counter with the contents of the next sequential location, i.e. SP + 1.

RET cc Chapter 5, Page 257

Where:

cc specifies the condition which must be met for the Return to become effective, based on the following table:

Condition		**cc (Bin.)**	**Flag**
Non-Zero	NZ	ØØØ	Z
Zero	Z	ØØ1	Z
No Carry	NC	Ø1Ø	C
Carry	C	Ø11	C
Parity Odd	PO	1ØØ	P/V
Parity Even	PE	1Ø1	P/V
Sign Positive	P	11Ø	S
Sign Negative	M	111	S

If the condition specified in the instruction is TRUE, control is returned to the main program. The Lower Order byte of the Program Counter (PC) is loaded with the contents of the memory location whose address is held in the Stack Pointer (SP) and the Higher Order byte of the Program Counter is loaded with the contents of the next sequential memory location (SP + 1).

RETI Chapter 5, Page 259

Returns control to the main program following an Interrupt by placing the contents of the top two bytes of the Memory Stack into the Program Counter (the Top byte of the Memory Stack is placed in the Lower Order byte of the Program Counter and the next byte in the Higher Order byte of the Program Counter).

NOTE: An EI instruction must be executed before the RETI instruction to re-enable interrupts.

RETN Chapter 5, Page 261

Similar to a RET instruction but used at the end of a subroutine servicing a non-maskable interrupt. Returns program control to the main program by loading the Lower Order byte of the Program Counter (PC) with the contents of the top location in the Memory Stack and the Higher Order byte with the contents of the next sequential location (SP + 1). The contents of IFF2 Flip-Flop are also copied back into IFF1, restoring it to its original condition.

RST p Chapter 5, Page 299

Where:

p is the Lower Order byte of an address in low memory where the program is to be restarted.

NOTE: The Higher Order byte of this address is automatically loaded with ØØH, thus restricting the number of possible restart addresses to eight, based on the following values of p:

Hex.		**Bin.**	**Hex.**		**Bin.**
ØØH	—	ØØØ	2ØH	—	1ØØ
Ø8H	—	ØØ1	28H	—	1Ø1
1ØH	—	Ø1Ø	3ØH	—	11Ø
18H	—	Ø11	38H	—	111

The contents of the Program Counter (PC) are loaded on to the top of the Memory Stack (as for the PUSH instruction) and the Program Counter is then loaded with ØØH in the Higher Order byte and the value of p specified in the instruction in the Lower Order byte. The next instruction is then fetched from the nominated location in low memory.

11. Input and Output Group

This Group allows the transfer of single or multiple bytes (up to 256) between CPU registers or memory blocks and any one of 256 Input/Output device addresses.

INPUT AND OUTPUT GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
IN A, (N)	DB N	219 N	N	N	N	N	N	N	2	3	11	5.5		159
IN r, (C)			*	*	*	P	Ø	N	2	3	12	6		
r = A	ED 78	237 120												160
r = B	ED 40	237 064												160
r = C	ED 48	237 072												160
r = D	ED 50	237 080												160
r = E	ED 58	237 088												160
r = H	ED 60	237 096												160
r = L	ED 68	237 104												160
IND	ED AA	237 170	?	*	?	?	1	N	2	4	16	8		169
INI	ED A2	237 162	?	*	?	?	1	N	2	4	16	8		172
INIR	ED B2	237 172	?	1	?	?	1	N	2	5	21	10.5	If Register B ≠ 0	170
										4	16	8	If Register B = 0	
INDR	ED BA	237 186	?	1	?	?	1	N	2	5	21	10.5	If Register B ≠ Ø	235
										4	16	8	If Register B = Ø	
OTDR	ED BB	237 187	?	1	?	?	1	N	2	5	21	10.5	If Register B ≠ Ø	173
										4	16	8	If Register B = Ø	
OTIR	ED B3	237 179	?	*	?	?	1	N	2	5	21	10.5	If Register B ≠ Ø	236
										4	16	8	If Register B = Ø	
OUT (n), A	D3 n	211 n	N	N	N	N	N	N	2	3	11	5.5		239
OUT (C), r			N	N	N	N	N	N	2	3	12	6		
r = A	ED 79	237 121												238
r = B	ED 41	237 065												238
r = C	ED 49	237 073												238
r = D	ED 51	237 081												238
r = E	ED 59	237 089												238
r = H	ED 61	237 097												238
r = L	ED 69	237 105												238
OUTD	ED AB	237 171	?	*	?	?	1	N	2	4	16	8		240
OUTI	ED A3	237 163	?	*	?	?	1	N	2	4	16	8		241

FLAG KEY:				
	N	– Not affected.	1	– SET = 1.
	P	– Contains the Parity of the result (1 = Parity Even).	?	– Unknown.
	V	– Contains the Overflow of the result (1 = Overflow).	*	– Affected according to the result.
	Ø	– RESET = Ø.		

IN A,(N) Chapter 5, Page 159

Where:

(N) is the address of the Input Port, in the range Ø to 255.

N (the address of the Input Port) is placed in the Lower Order byte of the Address Bus and the contents of the Accumulator are placed in the Higher Order byte of that Bus. One byte from the Input Port is placed in the Accumulator.

IN r,(C) Chapter 5, Page 160

Where:

r represents one of the registers A, B, C, D, E, H or L.

The C register contains the address of an Input Port in the range Ø to 255. This Input Port is read and the single byte of data loaded into the nominated register. The Lower Order byte of the address bus is copied from Register C while the Higher Order byte is the previous contents of the B register.

IND Chapter 5, Page 169

This instruction reads, one byte at a time, up to 256 bytes of data from an Input Port and stores that data in consecutive memory locations. The address of the Input Port must be held in the C register (value Ø to 255) and Register B is used as a byte counter so must contain the number of bytes to be read. Register Pair HL must contain the address of the first memory location to be used to store the data. As each byte is read and stored both Register B and Register Pair HL are decremented.

INI Chapter 5, Page 172

Similar to instruction IND except that the contents of Register Pair HL are incremented, rather than decremented, as each byte is stored. Up to 256 bytes of data are read, one byte at a time, from an Input Port and stored in consecutive memory locations. Register C must contain the address (value Ø to 255) of the Input Port and Register B must contain the number of bytes to be read. Register Pair HL must contain the address of the first memory location to be used to store the data. As each byte is read and stored Register B is decremented and Register Pair HL is incremented.

INDR Chapter 5, Page 170

Identical to IND except:

1. If the contents of Register B — 1 = Ø, the next instruction is executed.
2. If the contents of Register B — 1 ≠ Ø, the Program Counter (PC) is decremented by 2 and the INDR instruction is repeated.

   NOTE 1: If the contents of Register b are Ø at the start of this instruction, 256 Bytes of data will be input.

   NOTE 2: Interrupts will be recognised after each loop.

INIR Chapter 5, Page 173

Similar to the INDR instruction except that the contents of Register Pair HL are incremented after each execution instead of being decremented.

OTDR Chapter 5, Page 235

Outputs a pre-determined number of bytes of data, one byte at a time, to an output port selected from up to 256 (i.e., Ø to 255) possible ports. The sequence of events is:

1. The data stored in a memory location whose address is held in the Accumulator is temporarily stored in the CPU.
2. Register B (used as a byte counter) is decremented and the new (decremented) value placed in the Higher Order byte of the Address Bus.
3. The contents of Register C are placed in the Lower Order byte of the Address Bus. This contains the identity of the Output Port to which the data is to be directed, (i.e. a value between Ø and 255).

4. The data byte temporarily stored in the CPU is placed on the Data Bus for output to the nominated Output Port.
5. Register Pair HL is decremented.
6. If Register B is non-zero, the Program Counter (PC) is decremented by 2 and the instruction is executed again. If the value of Register B is zero, the program proceeds with the next sequential instruction.

NOTE 1: If Register B is set to zero prior to the first execution of this instruction then 256 bytes of data will be output.
NOTE 2: Interrupts are permitted after each byte is output.

OTIR Chapter 5, Page 236

Similar to OTDR except that Register Pair HL is incremented instead of decremented after each data byte is output.

OUT (n), A Chapter 5, Page 239

Where:

(n) is the address of one of 256 (i.e. Ø to 255) Output Ports.

Places the Output Port address (n) in the Lower Order byte of the Address Bus and the contents of the Accumulator in the Higher Order byte of the Address Bus. The contents of the Accumulator are then passed to the selected Output Port.

OUT (C),r Chapter 5, Page 238

Where:

r represents one of the registers A, B, C, D, E, H or L.

Outputs the contents of the nominated register to the Output Port whose identity (Ø to 255) is held in the C Register. The contents of the C Register are placed in the Lower Order byte of the Address Bus.

OUTD Chapter 5, Page 240

Outputs one or more (up to 256) bytes of data from consecutive memory locations to an Output Port identified by the contents of Register C. Register B is used as a byte counter and must therefore contain the number of bytes to be output. Register Pair HL contains the address of the first byte to be output. After each data transfer both Register B and Register Pair HL are decremented.

OUTI Chapter 5, Page 241

This instruction is identical to OUTD except that, after each data transfer, Register Pair HL is incremented instead of decremented.

CHAPTER 5

Z8∅ Machine Code Instructions

This chapter contains details of each Z8∅ Machine Code instruction, in Source Code sequence, with the Object Code (Hexadecimal), Bit Pattern, Decimal Code, Flag Register Status, Addressing Mode, Timing and Description of each instruction.

ADC A,n

Description: Adds the contents of the Accumulator plus the carry bit to n and stores the result in the Accumulator.

No. of Bytes: 2

Object Code (Hex.): CE n　　　　Decimal: 2∅6 n

Where n is an 8 Bit value, specified in the instruction.

Bit Pattern

```
    1  1  ∅  ∅  1  1  1  ∅                n
```

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, RESET = ∅ if no overflow.
Subtract	N	1	RESET = ∅.
Carry	C	∅	SET = 1 if Carry from Bit 7.

Cont.

```
Example: LD A,Ø2H
         SCF
         ADC A,Ø27H
```

If the Accumulator contains Ø2H, the Carry Flag is set, and n in the instruction is 27H, then the result stored in the Accumulator will be Ø2H + 27H + Ø1H = 2AH. If the Carry Flag is not set, the result will be Ø2H + 27H + ØØH = 29H.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

ADC A,A

Description: Adds the contents of the Accumulator plus the carry bit to itself and stores the result in the Accumulator.

No. of Bytes: 1

Object Code (Hex.): 8F   Decimal: 143

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, RESET = Ø if no overflow
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 7.

```
Example: LD A,Ø3H
         SCF
         CCF
         ADC A,A
         or
         LD A,Ø3H
         SCF
         ADC A,A
```

If the Accumulator contains Ø3H prior to this instruction being executed, and the Carry Flag is reset, the result will be Ø6H. If the carry bit is set, the result will be Ø7H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

ADC A,r

Where r is any of the registers B, C, D, E, H or L.

Object Code:

	Hex	Decimal
ADC A,B	88	136
ADC A,C	89	137
ADC A,D	8A	138
ADC A,E	8B	139
ADC A,H	8C	14Ø
ADC A,L	8D	141

Description: Adds the contents of the Accumulator plus the carry bit to the contents of any of the other registers and stores the result in the Accumulator.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, RESET = Ø if no Overflow.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from Bit 7, otherwise RESET = Ø

Cont.

Example:
```
LD A,Ø1H
SCF
ADC A,B
or
LD A,Ø1H
SCF
CCF
ADC A,B
```

If the Accumulator contains Ø1H, the Carry Flag is set, and register B contains Ø2H, the result will be Ø1H + Ø1H + Ø2H = Ø4H. If the Carry Flag is reset, the result will be Ø1H + ØØH + Ø2H = Ø3H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

ADC A,(HL)

Description: Adds the contents of the Accumulator plus the Carry Flag to the contents of the memory location whose address is held in Register Pair HL and stores the result in the Accumulator.

No. of Bytes: 2

Object Code (Hex.): 8E Decimal: 142

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 7, otherwise RESET = Ø.

Cont.

Example:

```
LD A,Ø2H
LD L,Ø4H
LD H,Ø5DH
SCF
ADC A,(HL)
or
LD A,Ø2H
LD L,Ø4H
LD H,Ø5H
SCF
CCF
ADC A,(HL)
```

If the Accumulator contains Ø2H, the Carry Flag is reset, the H register contains 5DH and the L Register contains Ø4H then this instruction will add Ø2H to the contents of memory location 5D Ø4. If the contents of that location are Ø3H the result will be Ø2H + ØØH + Ø3H = Ø5H. If the carry flag is set, the result will be Ø2H + Ø1H + Ø3H = Ø6H. The result is stored in the Accumulator, and there is no effect on the contents of the memory location.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

ADC A,(IX+d)
ADC A,(IY+d)

Description: Adds the contents of the Accumulator plus the Carry Flag to the contents of a memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction) and places the result in the Accumulator.

No. of Bytes: 3

Object Code:

	Hex	Decimal
ADC A,(IX+d) ADC A,(IY+d)	DD 8E d FD 8E d	221 142 d 253 142 d

Where d is the displacement, in bytes, from the memory location whose address is identified by the contents of Index Register IX.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET Ø.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 7, otherwise RESET = Ø.

Cont.

```
Example: LD IX,3125H
         LD A,23H
         SCF
         ADC (A,(IX + 3)
         or
         LD IX,3125H
         LD A,23H
         SCF
         CCF
         ADC A,(1X + 3)
```

If the contents of the IX Index Register are 3125H and the value of d is Ø3H, the content of location 3128H is 15H, the value of the Accumulator is 23H, and the Carry Flag is reset, the result placed in the Accumulator will be 15H + ØØH + 23H = 38H. If the Carry Flag is set, the result will be 15H + Ø1H + 23H = 39H

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

ADC HL,rr

Where rr is any of the register pairs BC, DE, HL, SP.

Description: Adds the contents of Register Pair rr to the contents of Register Pair HL plus the Carry Flag, then stores the result in Register Pair HL.

No. of Bytes: 2

Object Code:

	Hex	**Decimal**
ADC HL,BC	ED 4A	237 Ø74
ADC HL,DE	ED 5A	237 Ø9Ø
ADC HL,HL	ED 6A	237 1Ø6
ADC HL,SP	ED 7A	237 122

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 11, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 15, otherwise RESET = Ø

Cont.

```
Example:  LD HL,ØF18H
          LD BC,3291H
          SCF
          ADC HL,BC
```

If the contents of the BC Register Pair are 3291H and that of the HL Register Pair ØF 18H and the Carry Flag is reset, then the result will be 41A9H which is placed in Register Pair HL. If the Carry Flag is set, the result will be 41AAH.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	75

ADD A,n

Description: Adds n to the contents of the Accumulator, then stores the result in the Accumulator.

No. of Bytes: 2

Object Code (Hex.): C6 n Decimal: 198 n

Where n is an 8 Bit value, specified in the instruction.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 7, otherwise RESET = Ø

Example: LD A,2AH
ADD A,33H

If the second byte of the instruction contains 33H and the contents of the Accumulator are 2AH, then the result will be 5DH.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

ADD A, r

Where r is any of the registers A, B, C, D, E, H, or L.

Object Code:

	Hex	Decimal
ADD A,A	87	135
ADD A,B	8∅	128
ADD A,C	81	129
ADD A,D	82	13∅
ADD A,E	83	131
ADD A,H	84	132
ADD A,L	85	133

Description: Adds the contents of the Register r to the contents of the Accumulator and stores the result in the Accumulator. NOTE: in the case of ADD A,A the effect is to double the contents of the Accumulator.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = ∅.
Subtract	N	1	RESET = ∅.
Carry	C	∅	SET = 1 if Carry from Bit 7, otherwise RESET = ∅.

Cont.

Example: LD A,3EH
LD B,Ø9H
ADD A,B

If the contents of the Accumulator are 3EH and the contents of the B register are Ø8H, the result will be 47H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

ADD A,(HL)

Description: Adds the contents of the memory location whose address is held in Register Pair HL to the contents of the Accumulator and stores the result in the Accumulator.

No. of Bytes: 1

Object Code (Hex.): 86 Decimal: 134

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is negative,, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise, RESET = Ø
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 7, otherwise RESET = Ø.

```
Example: LD HL,5AØ2H
         LD (HL),24H
         LD A,16H
         ADD A,(HL)
```

If the contents of Register Pair HL are 5A02H, the contents of that location are 24H and the contents of the Accumulator are 16H, then the result, stored in the Accumulator, is 3AH.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

ADD A,(IX + d)
ADD A,(IY + d)

Description: Adds the contents of the memory location identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction) to the contents of the Accumulator and stores the result in the Accumulator.

No. of Bytes: 3

Object Code:

	Hex	Decimal
ADD A,(IX + d) ADD A,(IY + d)	DD 86 d FD 86 d	221 134 d 253 134 d

Where d is the displacement required from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = ∅
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise, RESET = ∅
Subtract	N	1	RESET = ∅
Carry	C	∅	SET = 1 if Carry from BIT 7, otherwise RESET = ∅.

Cont.

```
Example:  LD IX,122AH
          LD HL,125AH
          LD (HL),15H
          LD A,2AH
          ADD A,(IX + 3ØH)
```

If the contents of Index Register IX are 12 2AH and displacement is 3ØH, the required memory location is 12 5AH. If the contents of that location are 15H and the contents of the Accumulator are 2AH, then the result, stored in the Accumulator, will be 3FH.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

ADD HL,rr

Where rr is any of the register pairs BC, DE, HL, SP.

Description: Adds the contents of Register Pair rr to the contents of Register Pair HL and stores the result in Register Pair HL.

No. of Bytes: 1

Object Code:

	Hex	Decimal
ADD HL,BC	Ø9	ØØ9
ADD HL,DE	19	Ø25
ADD HL,HL	29	Ø41
ADD HL,SP	39	Ø57

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 11, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if carry from Bit 15, otherwise RESET = Ø.

Example: LD BC,15ØAH
LD HL,2112H
ADD HL,BC

If the contents of Register Pair BC are 15ØAH and the contents of Register Pair HL are 21 12H, the result is 36 1CH.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	11	5.5

ADD IX,BC
ADD IY,BC

Description: Adds the contents of Register Pair BC to the contents of Index Register IX or IY and stores the result in Register IX or IY.

No. of Bytes: 2

Object Code:

	Hex	Decimal
ADD IX,BC ADD IY,BC	DD Ø9 FD Ø9	221 ØØ9 253 ØØ9

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 11, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 15, otherwise RESET = Ø.

Example: LD BC,1172H
LD IX,1Ø12H
ADD IX,BC

If the contents of Register Pair BC are 11 72H and the contents of Index Register IX are 1Ø 12H, the result will be 21 84H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

ADD IX,DE
ADD IY,DE

Description: Adds the contents of Register Pair DE to the contents of Index Register IX or IY and stores the result in Index Register IX or IY.

No. of Bytes: 2

Object Code:

	Hex	Decimal
ADD IX,DE ADD IY,DE	DD 19 FD 19	221 Ø25 253 Ø25

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 11, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 15, otherwise RESET = Ø.

Example:
```
LD DE,1321H
LD IX,2243H
ADD IX,DE
```

If the contents of Register Pair DE are 13 21H and the contents of Index Register IX are 22 43H, the result will be 35 64H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

ADD IX,IX

Description: Adds the contents of Index Register IX to the contents of Index Register IX and stores the result in Index Register IX, i.e. doubles the contents of that Index Register.

No. of Bytes: 2

Object Code (Hex.): DD 29 Decimal: 221 Ø41.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 11, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 15, otherwise RESET = Ø.

Example: LD IX,2345H
ADD IX,IX

If the contents of Index Register IX are 23 45H, then the result will be 23 45H + 23 45H = 46 8AH.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

ADD IY,IY

Description: Adds the contents of Index Register IY to the contents of Index Register IY and stores the result in Index Register IY, i.e. doubles the contents of Index Register IY.

No. of Bytes: 2

Object Code (Hex.): FD 29 Decimal: 253 ∅41.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 11, otherwise RESET = ∅
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = ∅
Carry	C	∅	SET = 1 if Carry from BIT 15, otherwise RESET = ∅.

Example: LD IY,1342H
ADD IY,IY

IF the contents of Index Register IY are 13 42H, then the result is 13 42H + 13 42H = 26 84H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

ADD IX,SP
ADD IY,SP

Description: Adds the contents of the Stack Pointer (Register Pair SP) to the contents of Index Register IX or IY and stores the result in Index Register IX or IY.

No. of Bytes: 2

Object Code:

	Hex	Decimal
ADD IX,SP ADD IY,SP	DD 39 FD 39	221 Ø57 253 Ø57

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 11, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if Carry from BIT 15, otherwise RESET = Ø.

Example:
```
LD SP,352BH
LD IX,221AH
ADD IX,SP
```

If the contents of the Stack Pointer are 35 2BH and the contents of Index Register IX are 22 1AH, the result will be 35 2BH + 22 1AH = 5745H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

AND n

Description: Performs a Logical AND on the contents of the Accumulator with n, storing the result in the Accumulator.

No. of Bytes: 2

Object Code (Hex.): E6 n Decimal: 23Ø n

Where n is an 8 Bit value, specified in the second byte of the instruction.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø
Carry	C	Ø	RESET = Ø

Example: LD A,ØA2H
AND 38H

If the contents of the Accumulator are A2(Hex). (Bit Pattern 1Ø1ØØØ1Ø) and the value of n is 38H (Bit Pattern ØØ111ØØØ) this has the effect of masking out Bits 7, 6, 2, 1 and Ø in the Accumulator as follows:

Accumulator — 1Ø1ØØØ1Ø
n — ØØ111ØØØ
Result — ØØ1ØØØØØ = 2ØH

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

AND A

Description: Performs a Logical AND on the contents of the Accumulator with the contents of the Accumulator and stores the result in the Accumulator. In practice, the contents of the Accumulator remain unaltered but the condition of the Flag Register Bits may change.

No. of Bytes: 1

Object Code (Hex.): A7 Decimal: 167.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø
Carry	C	Ø	RESET = Ø.

Example: LD A,ØC3H
AND A

If the contents of the Accumulator are C3(Hex.) (Bit Pattern 11ØØØØ11) the Logical AND will perform as follows:

Accumulator — 11ØØØØ11
Accumulator — 11ØØØØ11
Result — 11ØØØØ11 = C3H

Note that this has no effect on the value of the A register, but may change the values of the flags. This instruction is used specifically for its affects on the flags. For instance, if we want to RESET the Carry Flag, it is quicker and easier to say AND A than SCF followed by CCF.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

AND r

Where r is any of the registers B, C, D, E, H or L.

Object Code:

	Hex	Decimal
AND B	A∅	16∅
AND C	A1	161
AND D	A2	162
AND E	A3	163
AND H	A4	164
AND L	A5	165

Description: Performs a logical AND on the contents of the Accumulator with the contents of any of the other registers and stores the result in the Accumulator.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	RESET = ∅.

Cont.

Example: LD A,ØA1H
LD B,29H
AND B

If the contents of the Accumulator are A1(Hex.) (Bit Pattern 1Ø1ØØØØ1) and the contents of Register B are 29H (Bit Pattern ØØ1Ø1ØØ1) the Logical AND will perform as follows:

Accumulator — 1Ø1ØØØØ1
Register B — ØØ1Ø1ØØ1

Result — ØØ1ØØØØ1 = 21H

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

AND (HL)

Description: Performs a Logical AND on the contents of the Accumulator with the contents of a memory location whose address is held in Register Pair HL, then stores the result in the Accumulator.

No. of Bytes: 1

Object Code (Hex.): A6 Decimal: 166.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø
Carry	C	Ø	RESET = Ø.

```
Example:  LD A,4AH
          LD (HL),ØC8H
          AND (HL)
```

If the contents of the Accumulator are 4A(Hex.) (Bit Pattern Ø1ØØ1Ø1Ø) and the contents of the memory location are C8H (Bit Pattern 11ØØ1ØØØ) the Logical AND will perform as follows:

```
    Accumulator      — Ø1ØØ1Ø1Ø = 4AH
    Memory Location  — 11ØØ1ØØØ = C8H
                       --------
    Result           — Ø1ØØ1ØØØ = 48H
```

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

AND (IX + d)
AND (IY + d)

Description: Performs a Logical AND on the contents of the Accumulator with the contents of a memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), then stores the result in the Accumulator.

No. of Bytes: 3

Object Code:

	Hex	**Decimal**
AND (IX + d) AND (IY + d)	DD A6 d FD A6 d	221 166 d 253 166 d

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø
Carry	C	Ø	RESET = Ø.

Cont.

Example: LD A,7DH
LD (IX + 5),6CH
AND (IX + 5)

If the contents of the Accumulator are 7D(Hex.) (Bit Pattern Ø11111Ø1) and the contents of the nominated memory location are 6CH (Bit Pattern Ø11Ø11ØØ) the Logical AND will perform as follows:

Accumulator — Ø11111Ø1 = 7DH
Memory Location — Ø11Ø11ØØ = 6CH

Result — Ø11Ø11ØØ = 6CH

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

BIT b,r

Description: Tests an individual Bit in the specified Register and sets the Z Flag in the Flag Register to the complement of the specified Bit.

No. of Bytes: 2

Where:

b identifies the Bit to be tested by the instruction in the range Ø to 7.

r identifies one of the Registers A, B, C, D, E, H or L which contains the Bit to be tested.

Object Code: (Hex.): CB xx Decimal 2Ø3 yyy

Where: xx or yyy are taken from the table below:

	A		B		C		D		E		H		L	
Bit	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy
Ø	47	Ø71	4Ø	Ø64	41	Ø65	42	Ø66	43	Ø67	44	Ø68	45	Ø69
1	4F	Ø79	48	Ø72	49	Ø73	4A	Ø74	4B	Ø75	4C	Ø76	4D	Ø77
2	57	Ø87	5Ø	Ø8Ø	51	Ø81	52	Ø82	53	Ø83	54	Ø84	55	Ø85
3	5F	Ø95	58	Ø88	59	Ø89	5A	Ø9Ø	5B	Ø91	5C	Ø92	5D	Ø93
4	67	1Ø3	6Ø	Ø96	61	Ø97	62	Ø98	63	Ø99	64	1ØØ	65	1Ø1
5	6F	111	68	1Ø4	69	1Ø5	6A	1Ø6	6B	1Ø7	6C	1Ø8	6D	1Ø9
6	77	119	7Ø	112	71	113	72	114	73	115	74	116	75	117
7	7F	127	78	12Ø	79	121	7A	122	7B	123	7C	124	7D	125

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Unknown.
Zero	Z	6	SET = 1 if Bit B of Register R is Ø, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

Example: LD C, 1Ø1ØØ1B
BIT 3,C

If bit 3 or the C register is set, BIT 3,C will leave the Z Flag = Ø. (BIT 3,C produces the Object Code CB 59.)

Addressing Mode: Indexed

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

BIT b, (HL)

Where b is any value from Ø to 7.

Object Code:

	Hex	Decimal
BIT Ø,(HL)	CB 46	2Ø3 Ø7Ø
BIT 1,(HL)	CB 4E	2Ø3 Ø78
BIT 2,(HL)	CB 56	2Ø3 Ø86
BIT 3,(HL)	CB 5E	2Ø3 Ø94
BIT 4,(HL)	CB 66	2Ø3 1Ø2
BIT 5,(HL)	CB 6E	2Ø3 11Ø
BIT 6,(HL)	CB 76	2Ø3 118
BIT 7,(HL)	CB 7E	2Ø3 126

Description: Tests the appropriate Bit b of a memory location whose address is held in Register Pair HL and sets the Z Flag in the Flag Register to the complement of that Bit.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Unknown.
Zero	Z	6	SET = 1 if Bit Ø = Ø, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LD HL,26A1H
          LD (HL),Ø
          BIT Ø,(HL)
```

If the contents of Register Pair HL are 26 A1(Hex.) and Bit Ø of memory address 26 A1 contains a Ø, then the Z Flag is SET = 1.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	12	6

BIT b, (IX + d)

Where d is the required displacement from the memory location whose address is held in Index Register IX.

Object Code:

	Hex	Decimal
BIT Ø,(IX + d)	DD CB d 46	221 2Ø3 d Ø7Ø
BIT 1,(IX + d)	DD CB d 4E	221 2Ø3 d Ø78
BIT 2,(IX + d)	DD CB d 56	221 2Ø3 d Ø86
BIT 3,(IX + d)	DD CB d 5E	221 2Ø3 d Ø94
BIT 4,(IX + d)	DD CB d 66	221 2Ø3 d 1Ø2
BIT 5,(IX + d)	DD CB d 6E	221 2Ø3 d 11Ø
BIT 6,(IX + d)	DD CB d 76	221 2Ø3 d 118
BIT 7,(IX + d)	DD CB d 7E	221 2Ø3 d 126

Description: Tests Bit b of the contents of a memory location identified by the contents of Index Register IX (modified by the two's complement displacement d, which is specified in the instruction), then sets the Z Flag in the Flag Register to the complement of that Bit b.

No. of Bytes: 4

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Unknown.
Zero	Z	6	SET = 1 if Bit Ø = Ø, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LD, HL,12ØØH
          LD (HL),5
          LD IX,11FCH
          BIT 2,(IX + 4)
```

If Bit 2 of the nominated memory location contains a 1, then the Z Flag is RESET = Ø.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	2Ø	1Ø

BIT b, (IY + d)

Where D is the required displacement from the memory location whose address is held in Index Register IY.

Object Code:

	Hex	**Decimal**
BIT Ø, (IY + d)	FD CB d 46	253 2Ø3 d Ø7Ø
BIT 1, (IY + d)	FD CB d 4E	253 2Ø3 d Ø78
BIT 2, (IY + d)	FD CB d 56	253 2Ø3 d Ø86
BIT 3, (IY + d)	FD CB d 5E	253 2Ø3 d Ø94
BIT 4, (IY + d)	FD CB d 66	253 2Ø3 d 1Ø2
BIT 5, (IY + d)	FD CB d 6E	253 2Ø3 d 11Ø
BIT 6, (IY + d)	FD CB d 76	253 2Ø3 d 118
BIT 7, (IY + d)	FD CB d 7E	253 2Ø3 d 126

Description: Tests Bit b of the contents of a memory location identified by the contents of Index Register IY (modifed by the two's complement displacement D, which is specified in the instruction), then sets the Z Flag in the Flag Register to the complement of that Bit b.

No. of Bytes: 4

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Unknown.
Zero	Z	6	SET = 1 if Bit Ø = Ø, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LD HL,1Ø1H
          LD IY,1ØØH
          LD (HL),44H
          BIT 3,(IY + 1)
```

If Bit 3 of the nominated memory location contains a Ø, then the Z Flag is SET = 1.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	20	1Ø

CALL nn

Description: Calls a sub-routine whose address is specified in the second and third bytes of the instruction (nn). The existing contents of the Program Counter (PC) are pushed on to the top of the Memory Stack and the sub-routine address nn loaded into the Program Counter. The second byte of the instruction contains the Lower Order byte of the sub-routine address while the third byte contains the Higher Order byte of that address.

NOTE: To return from the sub-routine to the main program, a RET instruction must be included in the sub-routine code.

No. of Bytes: 3

Object Code (Hex.): CD n n Decimal: 2Ø5 n n

Where nn is the memory location to which control is to be transferred.

Flag Register: None of the flags is affected.

Example: If the existing contents of the Program Counter are 25 BA (Hex.) and the top of the Memory Stack is at location 48 18(Hex.), then the Stack Pointer (SP) will contain address 48 18H. If a CALL instruction then quotes a sub-routine address 32 AA, the current contents of the Program Counter will be placed in memory locations 48 16 and 48 17 (i.e. on top of the memory stack) and the contents of the Stack Pointer will be changed to 48 16H. The contents of the second and third bytes of the instruction are then placed in the Program Counter, which will then contain 32 AAH.

Object Code			Before	After
CD AA 32	PC	—	25 BA	32 AA
	SP	—	48 18	48 16
	Loc'n 48 16	—	?	BA
	Loc'n 48 17	—	?	25
	Loc'n 48 18	—	Unchanged	Unchanged

NOTE: The Lower Order byte of the original contents of the Program Counter is placed in the higher of the two new memory locations at the top of the Memory Stack and the Stack Pointer (SP) will therefore contain the address of that Lower Order byte.

Addressing Mode: Immediate.

Cont.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	17	8.5

CALL C,nn

Description: If the C Flag in the Flag Register indicates a Carry (i.e. = 1), this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the C Flag contains Ø the instruction is ignored. If the condition is met (C = 1), the existing contents of the Program Counter (PC) are pushed on the top of the Memory Stack and the sub-routine address nn loaded into the Program Counter. To return from the sub-routine a RET instruction should be included in the sub-routine code.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of that address.

No. of Bytes: 3

Object Code (Hex.): DC n n　　　Decimal: 22Ø n n

Where nn is the memory location to which control is to be transferred if the condition is met, i.e. True

Flag Register: None of the flags is affected.

Example: SCF
　　　　CALL C,2425H

If the C Flag = 1 (Carry), the existing contents of the Program Counter are 42 35 and the top of the Memory Stack is at memory location 46 2B, then he Stack Pointer (SP) will contain address 46 2B. If the CALL C nn instruction quotes address 24 25, then the current contents of the Program Counter (42 35) are placed in memory locations 46 2A (Higher Order byte) and 46 29 (lower Order byte), the Stack Pointer is changed to 46 29 and address 24 25 (nn in the instruction) is placed in the Program Counter.

Object Code			Before	After
D4 25 24	PC	—	42 35	24 25
	SP	—	46 2B	46 29
	Loc'n 46 29	—	?	35
	Loc'n 46 2A	—	?	42
	Loc'n 46 2B	—	Unchanged	Unchanged

Addressing Mode: Immediate.

Timing:	M Cycles	T States	µsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CALL NC,nn

Description: If the C Flag in the Flag Register indicates a No Carry (i.e. = Ø), this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the C Flag contains 1 the instruction is ignored. If the condition is met (C = Ø), the existing contents of the Program Counter (PC) are pushed on the top of the Memory Stack and the sub-routine address nn loaded into the Program Counter. To return from the sub-routine, a RET instruction should be included in the sub-routine code.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte.

No. of Bytes: 3

Object Code (Hex.): D4 n n   Decimal: 212 n n

Where nn is the memory location to which control is to be transferred if the condition is met, i.e. True

Flag Register: None of the flags is affected.

Example: SCF
CCF
CALL NC,1245H

If the C Flag = Ø (No Carry), the existing contents of the Program Counter are 45 A3 and the top of the Memory Stack is at memory location 56 78, then the Stack Pointer (SP) will contain address 56 78. If the CALL NC nn instruction quotes address 12 45, then the current contents of the Program Counter (45 A3) are placed in memory locations 56 77 (Higher Order byte) and 56 76 (Lower Order byte), the Stack Pointer is changed to 56 76 and address 12 45 (nn in the instruction) is placed in the Program Counter.

Object Code			Before	After
D4 45 12	PC	—	45 A3	12 45
	SP	—	56 78	56 76
	Loc'n 56 76	—	?	A3
	Loc'n 56 77	—	?	45
	Loc'n 56 78	—	Unchanged	Unchanged

Addressing Mode: Immediate.

Timing:	M Cycles	T States	μsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CALL P,nn

Description: If the S Flag in the Flag Register indicates a Positive sign condition (i.e. = Ø), this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the S Flag contains a 1 the instruction is ignored. If the condition is met (S Flag = Ø), the existing contents of the Program Counter (PC) are pushed on to the top of the Memory Stack and sub-routine address nn is loaded into the Program Counter. To return from the sub-routine a RET instruction should be included in the sub-routine code.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of that address.

No. of Bytes: 3

Object Code (Hex.): F4 n n   Decimal: 244 n n

Where nn is the memory location to which control is to be transferred if the condition is met, i.e. True.

Flag Register: None of the flags is affected.

Example: LD A,Ø
ADD A,1
CALL P,2244H

If the S Flag = Ø (Sign Positive), the existing contents of the Program Counter are 15 67 and the top of the Memory Stack is at location 32 46, then the Stack Pointer (SP) will contain address 32 46. If the CALL P,nn instruction quotes address 22 44, then the current contents of the Program Counter (15 67) are placed in memory locations 32 45 (Higher Order byte) and 32 44 (Lower Order byte), the Stack Pointer is changed to 32 44 and address 22 44 (nn in the instruction) is placed in the Program Counter.

Object Code			Before	After
F4 44 22	PC	—	15 67	22 44
	SP	—	32 46	32 44
	Loc'n 32 44	—	?	67
	Loc'n 32 45	—	?	15
	Loc'n 32 46	—	Unchanged	

Addressing Mode: Immediate.

Cont.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CALL M,nn

Description: If the S Flag in the Flag Register indicates a Negative condition (i.e. = 1), this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the S Flag contains a Ø the instruction is ignored. If the condition is met (S Flag = 1), the existing contents of the Program Counter (PC) are pushed on to the top of the Memory Stack and sub-routine address nn is loaded into the Program Counter. To return from the sub-routine a RET instruction should be included in the sub-routine code.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of that address.

No. of Bytes: 3

Object Code (Hex.): FC n n Decimal: 252 n n

Where nn is the memory location to which control is to be transferred if the condition is met, i.e. True.

Flag Register: None of the flags is affected.

```
Example: LD A,Ø
         SUB A,1
         CALL M,3814H
```

If the S Flag = 1 (Sign Negative), the existing contents of the Program Counter are 42 24 and the top of the Memory Stack is at location 9A 21, then the Stack Pointer (SP) will contain address 9A 21. If the CALL M,nn instruction quotes address 38 14, then the current contents of the Program Counter (42 24) are placed in memory locations 9A 2Ø (Higher Order byte) and 9A 1F (Lower Order byte), the Stack Pointer is changed to 9A 1F and address 38 14 (nn in the instruction) is placed in the Program Counter.

Object Code			Before	After
FC 14 38	PC	—	42 24	38 14
	SP	—	9A 21	9A 1F
	Loc'n 9A 1F	—	?	38
	Loc'n 9A 2Ø	—	?	14
	Loc'n 9A 21	—	Unchanged	

Addressing Mode: Immediate.

Timing:	M Cycles	T States	μsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CALL Z,nn

Description: If the Z Flag in the Flag Register indicates Zero (i.e. = 1) this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the Z Flag contains a Ø the instruction is ignored. If the condition is met (Z = 1) the existing contents of the Program Counter (PC) are pushed on to the top of the Memory Stack and sub-routine address nn is loaded into the Program Counter. To return from the sub-routine a RET instruction should be included in the sub-routine code.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of that address.

No. of Bytes: 3

Object Code (Hex.): CC n n Decimal: 2Ø4 n n

Where nn is the memory location to which control is to be transferred if the condition is met

Flag Register: None of the flags is affected.

Example: SUB A,A
CALL Z,7639H

If the Z Flag = 1, the existing contents of the Program Counter are 2A 26 and the top of the Memory Stack is at location 58 2C, then the Stack Pointer (SP) will contain address 58 2C. If the CALL Z nn instruction quotes address 76 34, then the current contents of the Program Counter (2A 26) are placed in memory locations 58 2B (Higher Order byte) and 58 SA (Lower Order byte), the Stack Pointer is changed to 58 2A and address 67 34 (nn int he instruction) is placed in the Program Counter.

Object Code			Before	After
CC 34 76	PC	—	2A 26	34 76
	SP	—	58 2C	58 2A
	Loc'n 58 2A	—	?	26
	Loc'n 58 2B	—	?	2A
	Loc'n 58 2C	—	Unchanged	Unchanged

Addressing Mode: Immediate.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CALL NZ,nn

Description: If the Z Flag in the Flag Register indicates a Non-Zero (i.e. = Ø) this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the Z Flag = 1 the instruction is ignored.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte.

If the condition is met, the existing contents of the Program Counter (PC) are pushed on to the top of the Memory Stack and the sub-routine address (nn) loaded into the Program Counter. To return from the sub-routine to the main program, a RET instruction should be included in the sub-routine code.

No. of Bytes: 3

Object Code (Hex.): C4 n n   Decimal: 196 n n

Where nn is the memory location to which control is to be transferred if the condition is met.

Flag Register: None of the flags is affected.

Example: LD A,Ø
ADD A,1
CALL NZ,3521H

If the Z Flag = Ø, the existing contents of the Program Counter are 17 14(Hex.) and the top of the Memory Stack is at memory location 28 1A, then the Stack Pointer (SP) will contain address 28 1A. If the CALL NZ nn instruction quotes sub-routine address 35 21, the current contents of the Program Counter (17 14) are placed in memory locations 28 19 (Higher Order byte) and 28 18 (Lower Order byte), the Stack Pointer is changed to 28 18 and address 35 21 (nn in the instruction) is placed in the Program Counter.

Object Code			Before	After
C4 35 21	PC	—	17 14	35 21
	SP	—	28 1A	28 18
	Loc'n 28 18	—	?	14
	Loc'n 28 19	—	?	17
	Loc'n 28 1A	—	Unchanged	Unchanged

Addressing Mode: Immediate.

Cont.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CALL PE,nn

Description: If the P/V Flag in the Flag Register indicates a Parity Even condition (i.e. = 1), this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the P/V Flag contains a Ø the instruction is ignored. If the condition is met (P/V = 1), the existing contents of the Program Counter (PC) are pushed on to the top of the Memory Stack and sub-routine address nn is loaded into the Program Counter. To return from the sub-routine a RET instruction should be included in the sub-routine code.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of that address.

No. of Bytes: 3

Object Code (Hex.): EC n n   Decimal: 236 n n

Where nn is the memory location to which control is to be transferred if the condition is met, i.e. True.

Flag Register: None of the flags is affected.

```
Example: LD A,Ø
         AND 1BH
         CALL PE,12DFH
```

If the P/V Flag = 1 (Parity Even), the existing contents of the Program Counter e 68 54 and the top of the Memory Stack is at location 35 9A, then the Stack Pointer (SP) will contain address 35 9A. If the CALL PE,nn instruction quotes address 12 DF, then the current contents of the Program Counter (68 54) are placed in memory locations 35 99 (Higher Order byte) and 35 98 and (Lower Order byte), the Stack Pointer is changed to 35 98 and address 12 DF (nn in the instruction) is placed in the Program Counter.

Object Code			Before	After
EC DF 12	PC	—	68 54	12 DF
	SP	—	35 9A	35 98
	Loc'n 35 98	—	?	54
	Loc'n 35 99	—	?	68
	Loc'n 35 9A	—	Unchanged	

Addressing Mode: Immediate.

Timing:	M Cycles	T States	µsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CALL PO,nn

Description: If the P/V Flag in the Flag Register indicates a Parity Odd condition (i.e. = Ø), this instruction CALLS a sub-routine whose address is specified in the second and third bytes of the instruction. If the P/V Flag contains a 1 the instruction is ignored. If the condition is met (P/V = Ø), the existing contents of the Program Counter (PC) are pushed on to the top of the Memory Stack and sub-routine address nn is loaded into the Program Counter. To return from the sub-routine, a RET instruction should be included in the sub-routine code.

NOTE: The second byte of the Object Code instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of that address.

No. of Bytes: 3

Object Code (Hex.): E4 n n Decimal: 228 n n

Where nn is the memory location to which control is to be transferred if the condition is met, i.e. True.

Flag Register: None of the flags is affected.

```
Example: LD A,Ø
         AND 19H
         CALL PO,3A4FH
```

If the P/V Flag = Ø (Parity Odd), the existing contents of the Program Counter are 13 31 and the top of the Memory Stack is at location 18 Ø5, then the Stack Pointer (SP) will contain address 18 Ø5. If the CALL PO,nn instruction quotes address 3A 4F, then the current contents of the Program Counter (13 31) are placed in memory locations 18 Ø4 (Higher Order byte) and 18 Ø3 (Lower Order byte), the Stack Pointer is changed to 18 Ø3 and address 3A 4F (nn in the instruction) is placed in the Program Counter.

Object Code			Before	After
E4 4F 3A	PC	—	13 31	3A 4F
	SP	—	18 Ø5	18 Ø3
	Loc'n 18 Ø3	—	?	31
	Loc'n 18 Ø4	—	?	13
	Loc'n 18 Ø5	—	Unchanged	Unchanged

Addressing Mode: Immediate.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
Condition True	5	17	8.5
Condition Untrue	3	1Ø	5

CCF

Description: Complements the Carry (C) Flag in the Flag Register, i.e. if the existing content is 1, it is changed to Ø; if the existing content is Ø, it is changed to 1.

No. of Bytes: 1

Object Code (Hex.): 3F Decimal: Ø63

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Previous carry status
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø
Carry	C	Ø	SET = 1 if previous content was Ø, otherwise RESET = Ø.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

CP n

Description: Compares the contents of the Accumulator with the 8 Bit value n and sets a flag according to the result.

No. of Bytes: 2

Object Code (Hex.): FE n Decimal: 254 n

Where n is an 8 Bit value, specified in the instruction.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is Ø, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET Ø.
Subtract	N	1	SET = 1
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Example: LD A,127
CP 129

If the contents of the Accumulator are 127 (Decimal) and the value on n in the instruction is 129, then n (129) is subtracted from 127 giving a result of −2. The S Flag and the N Flag are both SET = 1 and Flags Z, H, P/V and C are all RESET = Ø. The contents of the Accumulator remain unchanged and the result is discarded.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

CP A

Description: Compares the contents of the Accumulator with the contents of the Accumulator and sets a flag or flags according to the result. The contents of the Accumulator remain unchanged and the result is discarded.

NOTE: The result of this instruction must always be zero.

No. of Bytes: 1

Object Code (Hex.): BF Decimal: 191

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is Ø, otherwise RESET = Ø. In practice this will always be SET = 1.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET Ø. In practice this will always be RESET = Ø.
Subtract	N	1	SET = 1
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø. In practice this will always be RESET = Ø.

Example: LD A,23H
CP A

If the contents of the Accumulator are 23H the result is calculated as 23H − 23H = Ø. Flags Z, H, N and C are SET = 1 and flags S and P/V are RESET = Ø.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

CP r

Where r is one of the registers B, C, D, E, H, L.

Description: Compares the contents of Register B with the contents of the Accumulator and sets a flag or flags according to the result. The contents of the register and the Accumulator remain unchanged while the result is discarded.

No. of Bytes: 1

Object Code:

	Hex	Decimal
CP B	B8	184
CP C	B9	185
CP D	BA	186
CP E	BB	187
CP H	BC	188
CP L	BD	189

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø.
Subtract	N	1	SET = 1
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Cont.

Example: LD A,17H
LD B,∅2H
CP B

If the contents of the Accumulator are 17H and the contents of Register B are ∅2H, the result is calculated as 17H − ∅2H = 15H. Flags H, N and C are SET = 1 and flags S, Z and P/V are RESET = ∅.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

CP (HL)

Description: Compares the contents of a memory location whose address is held in Register Pair HL by subtracting the contents of that memory location from the Accumulator then sets a flag or flags according to the result. The contents of the register and the Accumulator remain unchanged while the result is discarded.

No. of Bytes: 1

Object Code (Hex.): BE Decimal: 19Ø

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø.
Subtract	N	1	SET = 1
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Example:
```
LD A,34H
LD (HL),21H
CP (HL)
```

If the contents of the Accumulator are 34H and the contents of the memory location are 21H, the result is calculated as 34H — 21H = 13H. Flags H and N are SET = 1 while flags S, Z, P/V and C are RESET = 0.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

CP (IX + d)
CP (IY + d)

Description: Compares the contents of the Accumulator with the contents of a memory location identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction). The contents of the memory location are subtracted from the Accumulator and a flag or flags set according to the result. The contents of both the Accumulator and the memory remain unchanged while the result is discarded.

No. of Bytes: 3

Object Code:

	Hex	**Decimal**
CP (IX + d)	DD BE d	221 19∅ d
CP (IY + d)	FD BE d	253 19∅ d

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = ∅
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = ∅.
Subtract	N	1	SET = 1
Carry	C	∅	SET = 1 if no Borrow, otherwise RESET = ∅.

Cont.

```
Example:  LD A,12H
          LD (1ØØØH),A
          LD A,17H
          LD IY,ØFØØH
          CP (IY + 1ØØH)
```

If the contents of the Accumulator are 17H and the contents of the nominated location are 12H, the result is calculated as 17H − 12H = Ø5H. Flags H and N are SET = 1 while flags S, Z, P/V and C are RESET = Ø.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	µsec @ 2 MHz.
5	19	9.5

CPD

Description: The contents of the Accumulator are compared with the contents of a memory location whose address is held in Register Pair HL. The contents of the memory location are subtracted from the Accumulator and a flag or flags set depending on the result. The contents of the memory location and the Accumulator remain unchanged while the result is discarded. The contents of both Register Pair HL and Register Pair BC (Byte Counter) are decremented.

No. of Bytes: 2

Object Code (Hex.): ED A9 Decimal: 237 169

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is zero, i.e. A = (HL), otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of Register Pair BC − 1 (i.e. the Byte Counter) = Ø, otherwise RESET = Ø.
Subtract	N	1	SET = 1
Carry	C	Ø	Not affected.

Example:
```
LD A,16H
LD (HL),12H
CPD
```

If the contents of the Accumulator are 16H and the contents of the memory location are 12H, the result is calculated as 16H − 12H = Ø4H. Flags H and N are SET = 1, flags S, Z and P/V are RESET = Ø while flag C is unaffected.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

CPDR

Description: The contents of a memory location whose address is held in Register pair HL are subtracted from the contents of the Accumulator. If the result is zero (i.e. A = (HL)), the zero bit is set and both Register Pair HL and Register Pair BC are decremented and the instruction is terminated. The instruction is also terminated if the new value of Register Pair BC is zero, even if the contents-of the memory location and the Accumulator are not equal. If the new value of Register Pair BC is not zero, AND the contents of the memory location do not equal the contents of the Accumulator, the Program Counter is decremented (by 2) and the instruction is repeated, i.e. the Program Counter is returned to the value it contained when the CPDR instruction was initiated.

NOTE 1: If the Register Pair BC is initialised to Ø prior to this instruction being initiated it will fail the BC = Ø test and cycle through all 64K of memory.

NOTE 2: Data interrupts can be recognised after each time the instruction is processed.

No. of Bytes: 2

Object Code (Hex.): ED B9 Decimal: 237 185

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the contents of the memory location and the Accumulator are equal, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of Register Pair BC<>Ø, otherwise RESET = Ø.
Subtract	N	1	SET = 1
Carry	C	Ø	Not affected.

Cont.

Example: If the contents of the Accumulator are 25H and the contents of the memory location whose address is held in Register Pair HL are 22H, then the Program Counter is returned to the point where the instruction was initiated while Register Pair HL and Register Pair BC are decremented. The instruction is then repeated (provided Register Pair BC does not contain zero), using the PRECEDING memory location. If the contents of this new location equal the contents of the Accumulator, then Flag Z will be SET = 1 and the instruction terminated.

Addressing Mode: Indirect.

Timing:

	M Cycles	T States	μsec @ 2 MHz.

BC = Ø or
A = (HL)
	4	16	8

BC<>Ø *and* A<>(HL)	5	21	9.5

CPI

Description: The contents of the memory location whose address is held in Register Pair HL are subtracted from the Accumulator and a flag or flags set depending on the result. Register pair HL is INCREMENTED while Register Pair BC is DECREMENTED. The contents of the memory location and the Accumulator remain unchanged while the result is discarded.

No. of Bytes: 2

Object Code (Hex.): ED A1 Decimal: 237 161

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the result is Ø, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	RESET = Ø if new value of Register Pair BC = Ø, otherwise SET = Ø.
Subtract	N	1	SET = 1
Carry	C	Ø	Not affected.

```
Example:  LD A,ØA3H
          LD (HL),A
          LD BC,1
          CPI
```

If the contents of both the Accumulator and the nominated location are A3H, the result is calculated as A3H − A3H = ØØH. Flags Z, H and N are SET = 1 (also P/V if the new value of Register Pair BC = Ø while flag S is RESET = Ø. Flag C is not affected.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

CPIR

Description: The contents of a memory location whose address is held in Register Pair HL are subtracted from the contents of the Accumulator. If the result zero, i.e. A = (HL), the zero flag is set, Register Pair HL is INCREMENTED and Register Pair BC is DECREMENTED, then the instruction is terminated. The instruction is also terminated if the new value of Register Pair BC is zero, even if the contents of the memory location are not equal to the contents of the Accumulator. If the new value of Register Pair BC is not zero, AND the contents of the memory location do not equal the contents of the Accumulator, the Program Counter is decremented (by 2) and the instruction is repeated, i.e. the Program Counter is returned to the value it contained when the CPIR instruction was initiated.

NOTE 1: If Register Pair BC is initialised to Ø prior to this instruction being initiated it will fail the BC = Ø test and cycle through all 64K of memory.

NOTE 2: Data interrupts can be recognised after each time the instruction is processed.

No. of Bytes: 2

Object Code (Hex.): ED B1 Decimal: 237 177

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø
Zero	Z	6	SET = 1 if the contents of the memory location and the Accumulator are equal, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	RESET = Ø if new value of Register Pair BC = Ø, otherwise SET = 1.
Subtract	N	1	SET = 1
Carry	C	Ø	Not affected.

Cont.

```
Example: LD A,ØA3H
         LD (HL),95H
         LD BC,2
         CPIR
```

If the contents of the Accumulator are A3H and the contents of the memory location, whose address is held in Register Pair HL, are 95H, then the Program Counter is returned to the point where the instruction was initiated while Register Pair HL is INCREMENTED and Register Pair BC is DECREMENTED. Provided Register Pair BC does not then contain zero, the instruction is repeated, using the NEXT memory location (now pointed to by the contents of Register Pair HL). If the contents of this new location equal the contents of the Accumulator, then Flag Z will be SET = 1 and the instruction terminated.

Addressing Mode: Indirect.

Timing:

	M Cycles	T States	μsec @ 2 MHz.

BC = Ø or
A = (HL)
	4	16	8

BC <> Ø *and* A <> Ø	5	21	9.5

CPL

Description: Complements the contents of the Accumulator.

No. of Bytes: 1

Object Code (Hex.): 2F Decimal: Ø47

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	SET = 1.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	SET = 1
Carry	C	Ø	Not affected.

```
Example:  LD A,3DH
          CPL
```

If the contents of the Accumulator are 3DH (Bit Pattern ØØ1111Ø1) they are changed to C2H (Bit Pattern 11ØØØØ1Ø) and Flags H and N are both SET = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

DAA

Description: Adjusts the Accumulator to obtain the correct Bit Pattern for Binary Coded Decimal (BCD). This is achieved by conditionally adding 6 to either the left or right half byte of the Accumulator, based on the status of flags after an arithmetic operation.

No. of Bytes: 1

Object Code (Hex.): 27 Decimal: Ø39

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the Most Significant Bit (MSB) of the Accumulator = 1 after the instruction is executed, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the value of the Accumulator = Ø after the instruction is executed.
—	—	5	Not used.
Half Carry	H	4	See Operation Table below.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the Accumulator has Parity Even after the instruction is executed.
Subtract	N	1	Not affected.
Carry	C	Ø	See Operation Table below.

Cont.

Operation Table:

		Initial Value of			Value	Final
N	C	Lower Digit	H	Upper Digit	Added	Value
		(Bits 3 — Ø)		(Bits 7 — 4)	to Acc.	of C.
Ø	Ø	Ø—9	Ø	Ø—9	ØØ	Ø
(ADD,	Ø	A—F	Ø	Ø—8	Ø6	Ø
ADC,	Ø	Ø—3	1	Ø—9	Ø6	Ø
INC)	Ø	Ø—9	Ø	A—F	6Ø	1
	Ø	A—F	Ø	9—F	66	1
	Ø	Ø—3	1	A—F	66	1
	1	Ø—9	Ø	Ø—2	6Ø	1
	1	A—F	Ø	Ø—2	66	1
	1	Ø—3	1	Ø—3	66	1
1	Ø	Ø—9	Ø	Ø—9	ØØ	Ø
(SUB,	Ø	6—F	1	Ø—8	FA	Ø
SBC,	1	Ø—9	Ø	7—F	AØ	1
DEC,	1	6—F	1	6—F	9A	1

```
Example:  LD A,ØBBH
          INC A
          DAA
```

Assuming that the preceding arithmetic operation was NOT a subtract, then the value of the N Flag will be Ø. If, as a result of that operation, the contents of the Accumulator are BC (Hex.) and the value of the H Flag is Ø, then 66H is added to the Accumulator, making the value of the contents 22(BCD). The C Flag is made = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2MHz.
1	4	2

DEC r

Decrements Register contents.

Where r is any of the registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
DEC A	3D	Ø61
DEC B	Ø5	ØØ5
DEC C	ØD	Ø13
DEC D	15	Ø21
DEC E	1D	Ø29
DEC H	25	Ø37
DEC L	2D	Ø45

Description: Subtracts 1 from specified Register.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of the Accumulator were 8Ø(Hex.) before the instruction was carried out, otherwise RESET = Ø.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

Cont.

Example: LD A,8AH
DEC A

If the original contents of the Accumulator are 8A(Hex.), then after the instruction is carried out the contents of the Accumulator will be 89(Hex.), Flags H and N will be SET = 1 and Flags S, Z and P/V will be RESET = Ø.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

DEC (HL)

Description: Decrements the contents of a memory location whose address is held in Register Pair HL.

No. of Bytes: 1

Object Code (Hex.): 35 Decimal: Ø53

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of the memory location were 8Ø(Hex.) before the instruction was processed, otherwise RESET = Ø.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

Example: LD HL,24ACH
LD (HL),45H
DEC (HL)

If, before the instruction was processed, the contents of Register Pair HL were 24 AC and the contents of memory location 24 AC were 45(Hex.), then after the in instruction is processed the contents of Register Pair HL will remain unchanged, the contents of memory location 24 AC will be 44(Hex.), Flags H and N will be SET = 1 and Flags S, Z and P/V will be RESET = Ø.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	11	5.5

DEC (IX + d)
DEC (IY + d)

Description: Decrements the contents of a memory location identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction).

No. of Bytes: 3

Object Code:

	Hex	Decimal
DEC (IX + d) DEC (IY + d)	DD 35 d FD 35 d	221 Ø53 d 253 Ø53 d

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of the memory location were 8Ø(Hex.) before the instruction was processed, otherwise RESET = Ø.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

Cont.

Example: LD A,∅A9H
LD (36ADH),A
LD IX,36ABH
DEC (IX + 2)

If, before the instruction was processed, the contents of Index Register IX were 36 AB, the contents of memory location 36 AD were A9(Hex.) and the value of d in the instruction was ∅2(Hex.), then after the instruction was processed, the contents of the Index Register IX remain unchanged, the contents of memory location 36 AD will be A8(Hex.), Flags H and N will be SET = 1 and Flags S, Z and P/V will be RESET = ∅.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

DEC rr

Where rr is any of the register pairs BC, DE, HL or SP.

Object Code:

	Hex	Decimal
DEC BC	ØB	Ø11
DEC DE	1B	Ø27
DEC HL	2B	Ø43
DEC SP	3B	Ø59

Description: Decrements the 16-Bit contents of the Register Pair BC, DE, HL or SP.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD BC,ØAC11H
DEC BC

If the contents of Register Pair BC and AC 11, then the effect of this instruction will be to decrement those contents to AC 1Ø.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	6	3

DEC IX
DEC IY

Description: Decrements the contents of Index Register IX or IY.

No. of Bytes: 2

Object Code:

	Hex	Decimal
DEC IX DEC IY	DD 2B FD 2B	221 Ø43 253 Ø43

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD IX,45H
DEC IX

If the original contents of the register are 45(Hex.) then after the instruction is processed those contents will be 44(Hex.)

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	10	5

DI

Description: Resets the Interrupt Flip-Flops, thus disabling the Maskable Interrupt function.

No. of Bytes: 1

Object Code (Hex.): F3 Decimal: 243

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

DJNZ,d

Description: Decrements the contents of Register B and performs a Jump instruction if the new contents of that register are non-zero by adding displacement d to the Program Counter (PC), which then contains the address of the next instruction to be carried out. If the new contents of Register B are zero, the Jump instruction is ignored and the next sequential instruction is obeyed.

No. of Bytes: 2

Object Code (Hex.): 1Ø d−2   Decimal: Ø16 d−2

Where d is the displacement required from the current contents of the Program Counter (PC) if the Jump instruction is to be obeyed.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

```
Example:  LD BC,Ø1
          DJNZ 6
```

If the contents of the Program Counter are 1Ø 11, the contents of Register B are Ø1, and displacement d in the instruction is Ø6, then the effect of this instruction is to decrement the contents of Register B to ØØ, the Jump instruction is ignored and the contents of the Program Counter are incremented by 2 to 1Ø 13. If B were not zero, the program counter would be set to 1Ø17.

Addressing Mode: Immediate.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
B <> Ø	3	13	6.5
B = Ø	2	8	4

EI

Description: Sets the Interrupt Flip-Flops thereby enabling the Maskable Interrupt function.

No. of Bytes: 1

Object Code (Hex.): FB Decimal: 251

NOTE: The Maskable Interrupt function is not enabled until this instruction has been completed.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Addressing Mode: Implicit.
Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

EX AF,AF'

Description: Exchanges the contents of Register Pair AF with the contents of Register AF'

No. of Bytes: 1

Object Code (Hex.): Ø8 Decimal: ØØ8

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affeced.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: If the contents of Register Pair AF are 34H and the contents of Register Pair AF' are ABH, then after this instruction is processed Register Pair AF will contain ABH and Register Pair AF' will contain 34H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

EX DE,HL

Description: Exchanges the contents of Register Pair DE with the contents of Register Pair HL.

No. of Bytes: 1

Object Code (Hex.): EB Decimal: 235

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

```
Example: LD DE,23H
         LD HL,67H
         EX DE,HL
```

If the contents of Register Pair DE are 23H and the contents of Register Pair HL are 67H, then after this instruction is processed Register Pair DE will contain 67 H and Register Pair HL will contain 23H.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

EX (SP),HL

Exchange contents of Register Pair HL with the top of the Stack.

Object Code:

	Hex	Decimal
EX (SP),HL	E3	227

Description: Exchanges the Low Order byte of Register Pair HL (i.e. the contents of Register L) with the contents of the memory location whose address is pointed to by the contents of the Stack Pointer (SP) and exchanges the High Order byte of Register Pair HL with the contents of the next sequential memory location. The contents of the Stack Pointer remain unchanged.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example:
```
LD BC,ØFAACH
LD (1824H),BC
LD SP,1824
LD HL,7A2BH
EX (SP),HL
```

If the contents of Register Pair HL are 7A 2B, the Stack Pointer contains the address of memory location 18 24, memory location 18 24 contains AC and memory location 18 25 contains FA, then after this instruction is processed the contents of Register Pair HL will be FA AC, the contents of memory location 18 24 will be 2B and the contents of memory location 18 25 will be 7A.

Addressing Mode: Indirect.

Cont.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

EX (SP),IX
EX (SP),IY

Exchange contents of an Index Register and top of Stack.

Object Code:

	Hex	Decimal
Ex (SP),IX Ex (SP),IY	DD E3 FD E3	221, 227 253, 227

Description: Exchanges the Low Order byte of designated Index Register with the contents of the memory location whose address is held in the Stack Pointer (SP) and exchanges the High Order byte of that Index Register with the contents of the next sequential memory location. The contents of the Stack Pointer remain unaltered.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LD IX,89ADH
          LD SP,34A6H
          LD (SP),Ø219H
          EX (SP),IX
```

If the contents of Register Pair IX are 89 AD, the Stack Pointer contains the address of memory location 34 A6, memory location 34 A6 contains 19 and memory location 34 A7 contains 02, then after this instruction is processed the contents of Index Register IX will be 02 19, the contents of memory location 34 A6 will be AD and the contents of memory location 34 A7 will be 89.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

EXX

Description: Exchanges the contents of Register Pairs BC, DE and HL with the contents of the equivalent Register Pairs BC', DE' and HL'.

No. of Bytes: 1

Object Code (Hex.): D9 Decimal: 217

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

Example: If the contents of Register Pairs BC, DE and HL are 19 9∅, 2∅ 34 and DA AD respectively, and the contents of Register Pairs BC', DE' and HL' are AB CD, EF 12 and 34 56 respectively, then after this instruction has been processed the contents of each of these Register Pairs are:

BC – AB CD	DE – EF 12	HL – 34 56
BC' – 19 9∅	DE' – 2∅ 34	HL' – DA AD

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

HALT

Description: CPU suspends operations, executing NOP's until either an interrupt or a reset is received.

No. of Bytes: 1

Object Code (Hex.): 76 Decimal: 118

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2 + Indefinite NOP's

IM Ø

Description: Sets Interrupt Mode Ø allowing the interrupting device to insert an instruction on to the Data Bus for immediate execution.

No. of Bytes: 2

Object Code (Hex.): ED 46   Decimal: 237 Ø7Ø

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

IM 1

Description: Sets Interrupt Mode 1, i.e. the C.P.U. will execute a Restart to memory location ØØ 38(Hex.) when an Interrupt occurs.

No. of Bytes: 2

Object Code (Hex.): ED 56 Decimal: 237 Ø86

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

IM 2

Description: Sets Interrupt Mode 2. When an interrupt occurs a single byte is provided by the interrupting device and this is used as the Low Order byte of a memory location address to which control is to be transferred as a result of the interrupt. The contents of the Interrupt Register (I) are used as the High Order byte of that address.

No. of Bytes: 2

Object Code (Hex.): ED 5E Decimal: 237 Ø94

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

IN A,(n)

Input to Accumulator from Port n.

Object Code:

	Hex	Decimal
IN A,(n)	DB n	219 n

Description: Loads the Accumulator with a single byte of data from the Input Port identified by n in the instruction. The value of n is placed in the Lower Order byte of the address bus and the contents of the Accumulator are placed in the High Order byte of that address bus while the instruction is being processed.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD A,Ø
IN A,(3)

If the second byte of the instruction contains Ø3H as the value of n, and the accumulator contains ØØH, a single data byte will be loaded from Input Port 3 to the Accumulator.

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	11	5.5

IN r,(C)

Input to Register r where r is any of the registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
IN A, (C)	ED 78	237 12Ø
IN B, (C)	ED 4Ø	237 Ø64
IN C, (C)	ED 48	237 Ø72
IN D, (C)	ED 5Ø	237 Ø8Ø
IN E, (C)	ED 58	237 Ø88
IN H, (C)	ED 6Ø	237 Ø96
IN L, (C)	ED 68	237 1Ø4

Description: The address (Range Ø - 255) of an Input Port is held in Register C and this address is placed in the Lower Order byte of the address bus. The previous contents of Register B are used as the Higher Order byte in the address bus. A singlebyte of data is read from the nominated Input Port and placed in Register r.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the input data is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the input data is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4 otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Parity Even, RESET = Ø if Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

```
Example: LD A,21H
         LD C,Ø9H
         IN A,(C)
```

If the B register contains 21H and Register C contains Ø9H the address bus will be loaded with 21 Ø9, which identifies Input Port 9. If Input Port 9 holds a data byte, value A2H, that value is placed in the Accumulator, replacing the original contents (21H).

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	12	6

INC r

Increment Register contents where r is any of the Registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
INC A	3C	Ø6Ø
INC B	Ø4	ØØ4
INC C	ØC	Ø12
INC D	14	Ø2Ø
INC E	1C	Ø28
INC H	24	Ø36
INC L	2C	Ø44

Description: Add 1 to the specified register.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of the Accumulator were 7F(Hex.) before the instruction was executed, otherwise RESET = Ø.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

Example: LD A,18H
INC A

If the contents of the Accumulator are 18H the effect of INC A is to increment those contents to 19H, then RESET flags S, Z, H, P/V and N = Ø.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

INC rr

Where rr is any of the register pairs BC, DE, HL or SP.

Object Code:

	Hex	Decimal
INC BC	Ø3	ØØ3
INC DE	13	Ø19
INC HL	23	Ø35
INC SP	33	Ø51

Description: Increments the 16 bit contents of the Register Pairs BC, DE, HL, or SP.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD BC,412H
INC BC

If the contents of register pair BC are 412H, then INC BC will change this to 413H. None of the flags will be changed.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	6	3

INC (HL)

Description: Increments the contents of a memory location whose address is held in Register Pair HL.

No. of Bytes: 1

Object Code (Hex.): 34 Decimal: ∅52

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of the nominated location were 7F(Hex.) before this instruction was processed, otherwise RESET = ∅.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Not affected.

```
Example: LD HL,1815H
         LD (HL),1FH
         INC (HL)
```

If the contents of Register Pair HL were 18 15, and the contents of memory location 18 15 were 1F, the effect of this instruction is to increment the contents of memory location 18 15 to 2∅(Hex.), SET flag H = 1 and RESET flags S, Z, P/V and N = ∅.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	11	5.5

INC (IX + d)
INC (IY + d)

Description: Increments the contents of the memory location identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction).

No. of Bytes: 3

Object Code:

	Hex	Decimal
INC (IX + d) INC (IY + d)	DD 34 d FD 34 d	221 Ø52 d 253 Ø52 d

Where d is the displacement required from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if Carry from Bit 3, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the contents of the nominated location were 7F(Hex.) before the instruction was processed, otherwise RESET = Ø.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

Example: LD IX,56A2H
LD HL,56A8H
LD (HL),7FH
INC (IX + 6)

If d in the instruction is Ø6H and the contents of Index Register IX are 56 A2, this instruction will increment the contents of memory location 56 A8. If the contents of that location were 7F they will be incremented to 8Ø(Hex.), flags S, H and P/V will be SET = 1 and flags Z and N will be RESET = Ø.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

INC IX
INC IY

Increment contents of an Index Register.

Object Code:

	Hex	Decimal
INC IX INC IY	DD 23 FD 23	221 ∅35 253 ∅35

Description: The contents of the designated Index Register is increased by one.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

Example: LD IY,8∅4H
INC IY

If the contents of the IY register are 8∅4H, the effect of INC IY will be to change this to 8∅5H. None of the flags will be changed.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	1∅	5

IND

Description: The address (Range ∅ - 255) of an Input Port is held in Register C and this address is placed in the Lower Order byte of the address bus. The contents of Register B (which is used as a Byte Counter) are placed in the Higher Order byte of the address bus. A single byte of data is read from the designated Input Port and stored in the memory location whose address is held in Register Pair HL, then both Register B and Register Pair HL are decremented.

No. of Bytes: 2

Object Code (Hex.): ED AA Decimal: 237 17∅

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Unknown.
Zero	Z	6	SET = 1 if the contents of Register B are zero AFTER the instruction is processed, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	Unknown.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	SET = 1.
Carry	C	∅	Not affected.

Example:
```
LD C,∅4H
LD HL,1824H
LD B,∅1H
IND
```

If the contents of Register C are ∅4(Hex.), this identifies Input Port 4. If the contents of Register pair HL are 18 24 and the contents of Register B are ∅1H, this instruction will transfer the data byte from Input Port 4 to memory location 18 24, decrement Register Pair HL to 18 23, decrement Register B to ∅∅ and SET flags Z and N = 1.

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

INDR

Description: The address (Range Ø - 255) of an Input Port is held in Register C and this address is placed in the Lower Order byte of the address bus. The contents of Register B (which is used as a Byte Counter) are placed in the Higher Order byte of the address bus. A single byte of data is read from the designated Input Port and stored in the memory location whose address is held in Register Pair HL, then both Register B and Register Pair HL are decremented. If the new contents of Register B = Ø the Program Counter (PC) is decremented by 2 and the instruction is repeated. If the new contents of Register B = Ø then the instruction is terminated.

NOTE 1: If the contents of Register B are set = Ø prior to this instruction being processed, 256 bytes of data will be input and stored in consecutive memory locations.

NOTE 2: Interrupts can be accepted after each iteration of this instruction.

No. of Bytes: 2

Object Code (Hex.): ED BA Decimal: 237 186

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Unknown.
Zero	Z	6	SET = 1
—	—	5	Not used.
Half Carry	H	4	Unknown.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LD C,Ø6H
          LD HL,241ØH
          LD B,Ø8H
          INDR
```

If the contents of Register C are Ø6, this identifies Input Port 6. If the contents of Register Pair HL are 24 1Ø and those of Register B are Ø8H, this instruction will transfer 8 bytes of date from Input Port 6 and store them in memory locations 24 1Ø to 24 Ø3. Register B will be decremented progressively to zero while Register Pair HL will also be progressively decremented to 24 Ø3. Flags Z and N will be SET = 1.

Addressing Mode: External.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
B = Ø	4	16	8
B <> Ø	5	21	1Ø.5

INI

Description: The address (Range Ø - 255) of an Input Port is held in Register C and this address is placed in the Lower Order byte of the address bus while the contents of Register B (which is used as a Byte Counter) are placed in the Higher Order byte of the address bus. A single byte of data is read from the designated Input Port and stored in the memory location whose address is held in Register Pair HL, then Register B is Decremented and Register Pair HL is Incremented.

No. of Bytes: 2

Object Code (Hex.): ED A2 Decimal: 137 162

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Unknown.
Zero	Z	6	SET = 1 if the contents of Register B are zero AFTER the instruction is processed, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	Unknown.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

```
Example: LD C,Ø1H
         LD HL,1613H
         LD B,18H
         INI
```

If the contents of Register C are Ø1(Hex.), this identifies Input Port 1. If the contents of Register pairl HL are 16 13 and those of Register B are 18H, this instruction will transfer one data byte from Input Port 1 to memory location 16 13, Increment Register Pair HL to 16 14, decrement Register B to 17H, and SET flag N = 1 and RESET flag Z = Ø.

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

INIR

Description: The address (Range Ø - 255) of an Input Port is held in Register C and this address is placed in the Lower Order byte of the address bus. The contents of Register B (which is used as a Byte Counter) are placed in the Higher Order byte of the address bus. A single byte of data is read from the designated Input Port and stored in the memory location whose address is held in Register Pair HL, then Register B is Decremented and Register pair HL is Incremented. If the new contents of Register B = Ø the Program Counter (PC) is decremented by 2 and the instruction is repeated. If the new contents of Register B = Ø then the instruction is terminated.

NOTE 1: If the contents of Register B are set = Ø prior to this instruction being processed, 256 bytes of data will be input and stored in consecutive memory locations.

NOTE 2: Interrupts can be accepted after each iteration of this instruction.

No. of Bytes: 2

Object Code (Hex.): ED B2 Decimal: 237 178

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Unknown.
Zero	Z	6	SET = 1
—	—	5	Not used.
Half Carry	H	4	Unknown.
—	—	3	Not used.
Parity/Overflow	P/V	2	Unknown.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

Cont.

Example: LD C,ØAH
LD HL,23Ø2H
LD B,Ø5H
INIR

If the contents of Register C are ØA, this identifies Input Port 1Ø. If the contents of Register Pair Hl are 23 Ø2 and those of Register B are ØH, this instruction will transfer 5 bytes of data from Input Port 1Ø and store them in memory locations 23 Ø2 to 23 Ø6. Register B will be decremented progressively to zero while Register Pair HL will be incremented progressively to 23 Ø6. Flags Z and N will be SET =1.

Addressing Mode: External.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
B = Ø	4	16	8
B <> Ø	5	21	1Ø.5

JP nn

Description: Unconditional Jump to a memory location specified in the second and third bytes of the instruction.
NOTE: The contents of the Program Counter are NOT saved.

No. of Bytes: 3

Object Code (Hex.): C3 n n Decimal: 195 n n

Where n n is the memory location to which control is to be transferred.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: JP 2E14H
If the second and third bytes in this instruction contain 2E 14, the contents of the Program Counter (PC) will be replaced by 2E 14 and the next instruction will be fetched from that memory location.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	1Ø	5

JP (HL)

Jump to address contained in register pair HL.

Object Code:

	Hex	Decimal
JP (HL)	E9	233

Description: Unconditional jump to a memory location whose address is held in Register Pair HL. The contents of that register pair are loaded into the Program Counter and the next instruction fetched from that location.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD HL,142BH
JP (HL)

If the contents of Register Pair HL are 14 2B that data will be placed in the Program Counter (PC) by this instruction and the next instruction will be fetched from memory location 14 2B.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

JP (IX)
JP (IY)

Jump to address contained in the designated Index Register.

Object Code:

	Hex	Decimal
JP (IX)	DD E9	221, 233
JP (IY)	FD E9	253, 233

Description: Unconditional jump to a memory location whose address is held in the designated Index Register. The contents of that Index Register is loaded into the Program Counter and the next instruction fetched from that location.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD IX,1F34H
JP (IX)

If the contents of Index Register IX are 1F 34, that data will be placed in the Program Counter (PC) by this instruction and the next instruction will be fetched from memory location 1F 34.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

JP cc,nn

Jump to address nn if condition cc is met, where nn is the memory location to which control is to be transferred and cc can be NZ, Z, NC, C, PO, PE, P or M.

Object Code:

	Hex	**Decimal**
JP NZ,nn	C2 n n	194 n n
JP Z,nn	CA n n	202 n n
JP NC,nn	D2 n n	210 n n
JP C,nn	DA n n	218 n n
JP PO,nn	E2 n n	226 n n
JP PE,nn	EA n n	234 n n
JP P,nn	F2 n n	242 n n
JP M,nn	FA n n	250 n n

Description: A Conditional Jump is obeyed only if the condition in the Flag Register is met. The address specified in the second and third bytes of the instruction is loaded into the Program Counter (PC) and the next instruction is fetched from that memory location. For detailed explanations of the various conditions, see the conditional CALL instructions, such as CALL NZ,nn, CALL Z, nn, etc.

NOTE 1: The second byte of the instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of that address.

NOTE 2: The previous contents of the Program Counter are NOT saved.

Condition	**Flag**
Non zero	Z
Zero	Z
Non carry	C
Carry	C
Parity odd	P/O
Parity even	P/E
Sign positive	P
Sign negative	M

No. of Bytes: 3

Cont.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

```
Example:  LD A,Ø
          ADD A,1
          JP NZ,18A2H
```

If nn in the instruction contains 18 A2(Hex.) and the Z flag in the Flag Register = 1, the instruction is ignored and the next sequential instruction is obeyed.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	1Ø	5

JR d

Description: Adds the value of d−2 to the contents of the Program Counter (PC) and stores the result in the Program Counter. The next instruction is fetched from the memory location whose address is the new contents of the Program Counter.

NOTE 1: The value of d specified in the Object Code instruction must be two less than the required displacement because the Program Counter will already be incremented by 2 on reading this instruction. The Source Code value of d is decremented automatically by the assembler process.

No. of Bytes: 2

Object Code (Hex.): 18 d−2   Decimal: Ø24d−2

Where d is the required displacement from the current contents of the Program Counter (d may be negative).

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: JR 9

A Source Code statement of JR 9 will result in an Object Code instruction of 18 Ø7 (Hex.). If the contents of the Program Counter are 1A 28 immediately prior to this instruction being read, the contents of that Program Counter will become 1A 2A when the instruction is read, then 1A 31 when the instruction is obeyed, giving a total displacement of 9 from the original contents of the Program Counter.

Addressing Mode: Relative.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	12	6

JR cc,d

Where: cc is one of the condition codes NZ, Z, NC or C.
d is the required displacement from the current contents of the Program Counter. (NOTE: d may be negative).

Object Code:

	Hex	Decimal
JR NZ,d	2Ø d−2	Ø32 d−2
JR Z,d	28 d−2	Ø4Ø d−2
JR NC,d	3Ø d−2	Ø48 d−2
JR C,d	38 d−2	Ø56 d−2

Description: A Conditional Jump instruction which is obeyed only if the condition stated is true. If the condition is met, this instruction adds the value d−2 to the contents of the Program Counter (PC) and stores the result in the Program Counter. The next instruction is then fetched from the memory location whose address is the new contents of the Program Counter. If the condition is not met, this instruction is ignored and the next sequential instruction is executed. For detailed descriptions of the conditions, see the conditional call instructions, such as CALL NZ,nn and CALL Z,nn.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example: SCF
JR C,4

A Source Code statement of JR C,4 will result in an Object Code instruction of 38 Ø2(Hex.). If the contents of the Program Counter are 2B 62 before this instruction is read, the contents of that Program Counter will become 2B 64 when the instruction is read, then 2B 66 if the instruction is obeyed, giving a total displacement of 4 from the original contents of the Program Counter.

Addressing Mode: Relative.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
Condition true	3	12	6
Condition false	2	7	3.5

LD A,I

Object Code: (Hex) ED 57 (Decimal) 237 87.

Description: Loads the Accumulator with the contents of the I register. The I register is unaltered.

No. of Bytes: 2

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET=1 if result negative, otherwise RESET=∅.
Zero	Z	6	SET=1 if result is zero, otherwise RESET=∅.
—	—	5	Not used.
Half Carry	H	4	RESET=∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	Set to equal the contents of Interrupt Flip Flop 2.
Subtract	N	1	RESET=∅.
Carry	C	∅	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	9	4.5

LD A,R

Object Code: (Hex) ED 5F (Decimal) 237 95.

Description: Loads the Accumulator with the contents of the R register. The R register is unaltered.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET=1 if result negative, otherwise RESET=∅.
Zero	Z	6	SET=1 if result is zero, otherwise RESET=∅.
—	—	5	Not used.
Half Carry	H	4	RESET=∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	Set to equal the contents of the Interrupt Flip Flop 2.
Subtract	N	1	RESET=∅.
Carry	C	∅	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	9	4.5

LD A,(nn)

Description: Loads the contents of a memory location whose address is specified as n n in the instruction into the Accumulator, leaving the contents of that memory location unaltered.

NOTE 1: In the Object Code, the second byte of the instruction contains the Lower Order byte of the address and the third byte contains the Higher Order byte of the address.

No. of Bytes: 3

Object Code (Hex.): 3A n n   Decimal: ∅58 n n

Where nn is the address of a memory location.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

Example: An instruction LD A,(3D18) will result in an Object Code (Hex.) instruction 3A 18 3D. The contents of memory location 3D 18 will be loaded into the Accumulator, leaving the same value unchanged in memory location 3D 18.

Addressing Mode: Direct.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	13	6.5

LD A,(BC)

Description: Loads the Accumulator with the contents of a memory location whose address is held in Register Pair BC, leaving the contents of that memory location unaltered.

No. of Bytes: 1

Object Code (Hex.): ∅A Decimal: ∅1∅

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

```
Example: LD HL,142AH
         LD (HL),∅ADH
         LD BC,142AH
         LD A,(BC)
```

If Register Pair BC contains 14 2A, and the contents of memory location 14 2A are AD, this instruction will load AD into the Accumulator, leaving the same value in memory location 14 2A.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

LD A,(DE)

Description: Loads the Accumulator with the contents of a memory location whose address is held in Register Pair DE, leaving the contents of that memory location unaltered.

No. of Bytes: 1

Object Code (Hex.): 1A Decimal: Ø26

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

```
Example: LD HL,4D23H
         LD (HL),68H
         LD DE,4D23H
         LD A,(DE)
```

If Register Pair DE contains 4D 23, and the contents of memory location 4D 23 are 68, this instruction will load 68 into the Accumulator, leaving the same value in memory location 4D 23.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

LD r,n

Where r is one of A,B,C,D,E,H,L.

Description: Loads the value of n into register r.

No. of Bytes: 2

Object Code:

	Hex	Decimal
LD A,n	3E n	Ø62 n
LD B,n	Ø6 n	ØØ6 n
LD c,n	ØE n	Ø14 n
LD D,n	16 n	Ø22 n
LD E,n	1E n	Ø3Ø n
LD H,n	26 n	Ø38 n
LD L,n	2E n	Ø46 n

Where n is an 8 Bit integer, specified in the instruction.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: The Source Code statement LD B,14H will load the value 14(Hex.) into the accumulator.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

LD r,r′

Where r and r′ are any of the Registers A,B,C,D,E,H or L.

Description: Loads Register r with the contents of Register r′. Register r′ is unaltered.

No. of Bytes: 1

Object Code: LD r,r′ produces the object code xx(Hex.) or yyy(Decimal.), where xx and yyy are taken from the table below.

		r						
		A	B	C	D	E	H	L
		xx yyy	xx yyy	xx yyy	xx yyy	xx yyy	xx yyy	xx yyy
	A	7F 127	47 Ø71	4F Ø79	57 Ø87	5F Ø95	67 1Ø3	6F 111
r′	B	78 12Ø	4Ø 064	48 Ø72	5Ø Ø8Ø	58 Ø88	6Ø Ø96	68 1Ø4
	C	79 121	41 Ø65	49 Ø73	51 Ø81	59 Ø89	61 Ø97	69 1Ø5
	D	7A 122	42 Ø66	4A Ø74	52 Ø82	5A Ø9Ø	62 Ø98	6A 1Ø6
	E	7B 123	43 Ø67	4B Ø75	53 Ø83	5B Ø91	63 Ø99	6B 1Ø7
	H	7C 124	44 Ø68	4C Ø76	54 Ø84	5C Ø92	64 1ØØ	6C 1Ø8
	L	7D 125	45 Ø69	4D Ø77	55 Ø85	5D Ø93	65 1Ø1	6D 1Ø9

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD A,53H
LD L,A

If the contents of the Accumulator are 53H, this instruction will load 53H into Register L, leaving the same value in the Accumulator.

Cont.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

LD r,(HL)

Where r is any of registers A,B,C,D,E,H or L.

Description: Loads Register r with the contents of the memory location whose address is held in Register Pair HL, leaving the contents of that memory location unaltered. Note that in the cases of LD H,(HL) and LD L,(HL), the contents of the HL Register Pair will be altered.

No. of Bytes: 1

Object Code:

	Hex	**Decimal**
LD A,(HL)	7E	126
LD B,(HL)	46	Ø7Ø
LD C,(HL)	4E	Ø178
LD D,(HL)	56	Ø86
LD E,(HL)	5E	Ø94
LD H,(HL)	66	1Ø2
LD L,(HL)	6E	11Ø

Where n is an 8 Bit integer, specified in the instruction.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD HL, 4732H
LD (HL), 56H
LD E,(HL)

If the Register Pair HL contains 47 32H, and the content of memory location 4732H is 56H, this instruction will load 56H into Register E, leaving the same value in memory location 47 43H.

Cont.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

LD r,(IX + d)
LD r,(IY + d)

Where r is one of the Registers A,B,C,D,E,H or L, and d is an 8 bit integer.

Description: Loads register r with the contents of the memory location whose address is indentified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), leaving the contents of that memory location unaltered.

No. of Bytes: 3

Object Code:

	Hex	Decimal
LD A,(IX+d)	DD 7E d	221 126 d
LD A,(IY+d)	FD 7E d	253 126 d
LD B,(IX+d)	DD 46 d	221 Ø7Ø d
LD B,(IY+d)	FD 46 d	253 Ø7Ø d
LD C, (IX+d)	DD 4E d	221 Ø78 d
LD C,(IY+d)	FD 4E d	253 Ø78 d
LD D,(IX+d)	DD 56 d	221 Ø86 d
LD D,(IY+d)	FD 56 d	253 Ø86 d
LD E,(IX+d)	DD 5E d	221 Ø94 d
LD E,(IY+d)	FD 5E d	253 Ø94 d
LD H,(IX+d)	DD 66 d	221 1Ø2 d
LD H,(IY+d)	FD 66 d	253 1Ø2 d
LD L,(IX+d)	DD 6E d	221 11Ø d
LD L,(IY+d)	FD 6E d	253 11Ø d

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

```
Example: LD HL, 3224H
         LD (HL), 62H
         LD IX, 3221H
         LC C,(IX+3)
```

If Index Register IX contains 3221 (Hex.), and d in the instruction is 3, the required memory location is 3224 (Hex.). If the content of memory location 3224 is 62 (Hex.), this instruction will load 62 into register C, leaving the same value in memory location 32 24.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

LD I,A

Load Interrupt Vector Register from Accumulator.

Object Code:

	Hex	**Decimal**
LD I,A	ED 47	237 Ø71

Description: Loads the contents of the Accumulator into the Interrupt Vector Register (Register I), leaving the contents of the Accumulator unaltered.

No. of Bytes: 2

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD A,24H
LD I,A

If the Accumulator contains 24, this instruction loads 24 into Register 1, leaving the contents of the Accumulator unaltered.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	9	4.5

LD R,A

Description: Loads the contents of the Accumulator into the Memory Refresh Register (Register R), leaving the contents of the Accumulator unaltered.

No. of Bytes: 2

Object Code (Hex.): ED 4F Decimal: 237 Ø79

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD A,38
LD R,A
If the contents of the Accumulator are 38, this instruction will load 38 into Register R, leaving the same value in the Accumulator.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	9	4.5

LD rr, nn

Load Immediate into Register pair rr 16 bits of data nn, where rr is any of the Register Pairs BC, DE, HL or SP and nn is a two byte integer.

Object Code:

	Hex	Decimal
LD BC,nn	Ø1 n n	ØØ1 n n
LD DE,nn	11 n n	Ø17 n n
LD HL,nn	21 n n	Ø33 n n
LD SP,nn	31 n n	Ø49 n n

Description: Loads specified Register Pair with the two byte integer nn specified in the instruction. The second byte of the Object Code instruction is the Lower Order byte of the integer nn and the third byte of the Object Code instruction is the Higher Order byte of integer nn.

No. of Bytes: 3

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: The Source Code statement LD HL,244EH will produce the Object Code instruction 21 4E 24(Hex.), which will load Register Pair HL with the data 24 4E(Hex.).

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	1Ø	5

LD IX,nn
LD IY,nn

Description: Loads Index Register IX or IY with the two byte integer nn specified in the instruction. The third byte of the Object Code instruction is the Lower Order byte of the integer nn, and is loaded into the Lower Order byte of the Index Register, while the fourth byte of the Object Code instruction is the Higher Order byte of nn and is loaded into the Higher Order byte of the Index Register.

No. of Bytes: 4

Object Code:

	Hex	Decimal
LD IX,nn LD IY,nn	DD 21 n n FD 21 n n	221 Ø33 n n 253 Ø33 n n

Where nn is a two Byte integer, specified in the instruction.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: The Source Code statement LD IX,1Ø2ØH will produce the Object Code instruction DD 21 2Ø 1Ø(Hex.), which will load Index Register IX with the data 1Ø 2Ø(Hex.).

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	14	7

LD rr,(nn)

Load Register Pair from memory where rr is either BC, DE, HL or SP.

Object Code:

	Hex	Decimal
LD BC,(nn)	ED 4B n n	237 Ø75 n n
LD DE,(nn)	ED 5B n n	237 Ø91 n n
LD HL,(nn)	ED 6B n n	237 1Ø7 n n
LD SP,(nn)	ED 7B n n	237 123 n n

Description: Loads Register Pair rr with the contents of the memory location whose address is specified in the instruction AND the contents of that memory location + 1. The contents of the specified memory location are loaded into the Lower Order byte of Register Pair rr and the contents of the next memory location into the Higher Order byte of that Register pair.

No. of Bytes: 4

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example: LD HL,3145H
LD (HL),68H
LD BC,(3145H)

Source Code statement LD BC,(3145) will become Object Code instruction ED 4B 45 31. If the contents of memory location 31 45 are 68, and those of memory location 31 46 are A3, this instruction will load A3 into Register B and 68 into Register C, making the contents of Register Pair BC = A3 68.

Addressing Mode: Direct.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	20	1∅

LD IY,(nn)

LD IX,(nn)

Description: Loads Index Register IX or IY with the contents of a memory location whose address is specified in the instruction AND the contents of the next sequential memory location. The contents of the specified memory location are loaded into the Lower Order byte of Index Register IX or IY and the contents of the next memory location into the Higher Order byte of that Register.

No. of Bytes: 4

Object Code:

	Hex	Decimal
LD IX,(nn) LD IY,(nn)	DD 2A n n FD 2A n n	221 ∅42 n n 253 ∅42 n n

Where (nn) is the address of a memory location.

Flag Regjster:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

Cont.

Example: LD HL,1812H
LD (HL),6AH
LD IX,(1812 H)

The Source Code statement LD IX,(1812) will produce Object Code instruction DD 2A 12 18. If the contents of memory location 18 12 are 6A, and the contents of memory location 1813 are 24, this instruction will load 6A into the Lower Order byte of Index Register IX and 24 into the Higher Order byte of that Register, making the contents 24 6A.

Addressing Mode: Direct.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	2Ø	1Ø

LD SP, HL

Move contents of Register Pair HL to Stack Pointer.

Object Code:

	Hex	Decimal
LD SP, HL	F9	249

Description: Loads the Stack Pointer with the contents of Register Pair HL, leaving the contents of Register Pair HL unaltered.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD HL,5B24H
LD SP,HL

If the contents of Register Pair HL are 5B 24, this instruction will load 5B 24 into the Stack Pointer (SP), leaving the same value in Register Pair HL.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	6	3

LD SP, IX
LD SP, IY

Move contents of Index Register to Stack Pointer.

Object Code:

	Hex	Decimal
LD SP, IX LD SP, IY	DD F9 FD F9	221 249 253 249

Description: Loads the Stack Pointer (SP) with the contents of specified Index Register, leaving the contents of Index Register unaltered.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD IX,26A5
LD SP,IX

If Index Register IX contains 26 A5, this instruction will load the Stack Pointer with the data 26 A5, leaving the same value in Index Register IX.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	1Ø	5

LD (nn),A

Store Accumulator in memory location nn where nn is a two byte address.

Object Code:

	Hex	Decimal
LD (nn),A	32 n n	Ø5Ø n n

Description: Loads the contents of the Accumulator into the memory location whose address is specified in the second and third bytes of the Object Code instruction, leaving the contents of the Accumulator unaltered.

No. of Bytes: 3

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD A,9CH
LD (1A49H),A

If nn is specified in the Source Code statement as 1A 49, this will produce the Object Code instruction 32 49 1A (Note that the Lower Order byte of the address appears in the second byte of the Object Code instruction). If the contents of the Accumulator are 9C, this instruction will load 9C into memory location 1A, 49, leaving the same value in the Accumulator.

Addressing Mode: Direct.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	13	6.5

LD (nn),rr

Store Register Pair into memory location nn where rr can be any of the Registers BC, DE, HL or SP.

NOTE: The Lower Order byte of the address is held in the third byte of the Object Code instruction and the Higher Order byte of that address is held in the fourth byte of that instruction.

Object Code:

	Hex	**Decimal**
LD (nn),BC	ED 43 n n	237 Ø67 n n
LD (nn),DE	ED 53 n n	237 Ø83 n n
LD (nn),HL	ED 63 n n	237 Ø99 n n
LD (nn),SP	ED 73 n n	237 115 n n

Description: Loads the Lower Order byte of the contents of the specified Register Pair into the memory location whose address is specified in the instruction, and the Higher Order byte of that Register Pair into the next sequential memory location, leaving the contents of the Register Pair unaltered.

No. of Bytes: 4

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example: LD BC,6789H
LD (3456),BC

If nn is specified in the Source Code statement as 34 56, LD (3456),BC will produce the Object Code instruction ED 43 56 34. If the contents of Register Pair BC are 67 89, this instruction will load the value 89 into memory location 34 56 and the value 67 into memory location 34 57, leaving the value 67 89 in Register Pair BC.

Addressing Mode: Direct.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	2Ø	1Ø

LD (nn),IX
LD (nn),IY

Store Index Register into memory location nn where nn is the 2 byte address.

Object Code:

	Hex	**Decimal**
LD (nn),IX LD (nn),IY	DD 22 n n FD 22 n n	221 Ø34 n n 253 Ø34 n n

Description: Loads the Lower Order byte of the contents of the specified Index Register into the memory location whose address is specified in the instruction, and the Higher Order byte of that Index Register into the next sequential location, leaving the contents of the Index Register unaltered.

No. of Bytes: 4

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example: LD IX,7766H
LD (11AAH),IX

If nn is specified in the Source Code statement as 11 AA, LD (11AA),IY will produce the Object Code instruction FD 22 AA. If the contents of Index Register IY are 77 66', this instruction will load 66 into memory location 11 AA and 77 into memory location 11 AB, leaving the value 77 66 in Index Register IY.

Addressing Mode: Direct.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	2∅	1∅

LD (rr),A

Load Accumulator into memory location addressed by Register Pair rr where rr is Register Pairs BC or DE.

Object Code:

	Hex	Decimal
LD(BC),A LD(DE),A	Ø2 12	ØØ2 Ø18

Description: Loads the contents of the Accumulator into a memory location whose address is held in Register Pair rr, leaving the contents of the Accumulator unaltered.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

```
Example: LD BC,1A24H
         LD A,4AH
         LD (BC),A
```

If the contents of Register Pair BC are 1A 24, and the contents of the Accumulator are 4A, this instruction will load 4A into memory location 1A 24, leaving the same value in the Accumulator.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

LD (HL),n

Load Immediate into memory n, where n is an 8 bit integer.

Object Code:

	Hex	Decimal
LD (HL),n	36 n	Ø54 n

Description: Loads the value n into a memory location whose address is held in Register Pair HL.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD HL,223CH
LD (HL),1CH

The Source Code statement LD HL,1CH will produce the Object Code instruction 36 1C(Hex.). If the contents of Register Pair HL are 22 3C, this instruction will load the value 1C(Hex.) into memory location 22 3C.

Addressing Mode: Immediate/Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	1Ø	5

LD (HL),r

Load memory location from Register r where r is any of the Registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
LD (HL),A	77	119
LD (HL),B	7Ø	112
LD (HL),C	71	113
LD (HL),D	72	114
LD (HL),E	73	115
LD (HL),H	74	116
LD (HL),L	75	117

Description: Loads the contents of Register r into a memory location whose address is held in Register Pair HL, leaving the contents of Register r unaltered.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LD HL,48E1H
          LD A,87H
          LD (HL),A
```

If the contents of Register Pair HL are 48 E1, and the contents of the Accumulator are 87, this instruction will load 87 into memory location 48 E1, leaving the same value in the Accumulator.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

LD (IX + d),n
LD (IY + d),n

Description: Loads the integer n into a memory location which is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), leaving the contents of that memory location unaltered.

No. of Bytes: 4

Object Code:

	Hex	**Decimal**
LD (IX + d),n LD (IY + d),n	DD 36 d n FD 36 d n	221 ∅54 d n 253 ∅54 d n

Where: d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

Example: LD IX,2A35H
LD (IX+3),5H

If the contents of Index Register IX are 2A 35 and d and n are specified in he instruction as 3 and 5 respectively, this instruction will load the value ∅5(Hex.) into memory location 2A 38.

Addressing Mode: Indexed/Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	19	9.5

LD (IX+d),r
LD (IY+d),r

Load memory from Register r using Index Register IX or IY, where r can be any of the registers A, B, C, D, E, H or L and d is the required displacement from the memory location whose address is held in the Index Register.

Object Code:

	Hex	Decimal
LD (IY+d),A	FD 77 d	253 119 d
LD (IY+d),B	FD 7Ø d	253 112 d
LD (IY+d),C	FD 71 d	253 113 d
LD (IY+d),D	FD 72 d	253 114 d
LD (IY+d),E	FD 73 d	253 115 d
LD (IY+d),H	FD 74 d	253 116 d
LD (IY+d),L	FD 75 d	253 117 d

	Hex	Decimal
LD (IX+d),A	DD 77 d	221 119 d
LD (IX+d),B	DD 70 d	221 112 d
LD (IX+d),C	DD 71d	221 113 d
LD (IX+d),E	DD 73 d	221 115 d
LD (IX+d),H	DD 74 d	221 116 d
LD (IX+d),L	DD 75d	221 117 d

Description: Loads the contents of Register r into a memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), leaving the contents of the Register unaltered.

No. of Bytes: 3

Cont.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD IX, 34A1H
LD A,48H
LD (IX+6),A

If the contents of Index Register IX are 34 A1, and d in the instruction is 6, the required memory location is 34 A7. If the contents of the Accumulator are 48, this instruction will load 48 into memory location 34 A7, leaving the same value in the Accumulator.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

LDD

Data transfer between memory locations. Decrement source and destination addresses.

Object Code:

	Hex	**Decimal**
LDD	ED A8	237 168

Description: Transfers one byte of data from the memory location whose address is held in Register Pair HL to the memory location whose address is held in Register Pair DE, then decrements Register Pairs BC (which is used as a byte counter), DE and HL.

No. of Bytes: 2

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the new contents of Register Pair BC ≠ ∅, otherwise RESET = ∅.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Not affected.

Cont.

```
Example:  LD HL,2145H
          LD DE,6785H
          LD BC,Ø1H
          LDD
```

If the contents of Register Pair HL are 21 45 and the contents of Register Pair DE are 67 85, this instruction will transfer the contents of memory location 21 45 to memory location 67 85, leaving the same value in memory location 21 45. It will also decrement Register Pair HL to 21 44, Register Pair DE to 67 84 and, if the original contents of Register Pair BC were Ø1, that Register Pair will be decremented to ØØ, then Flags H, P/V and N will be RESET = Ø.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

LDDR

Data transfer between memory locations until counter is zero. Decrement source and destination registers.

Object Code:

	Hex	Decimal
LDDR	ED B8	237 184

Description: Transfers one byte of data from the memory location whose address is held in Register Pair HL to the memory location whose address is held in Register Pair DE, then decrements Register Pairs BC (which is used as a byte counter), DE and HL. If the new contents of Register Pair BC = Ø the instruction is terminated, otherwise the Program Counter (PC) is decremented by 2 and the instruction is repeated.

NOTE 1 If the initial value of Register Pair is set to zero, this instruction will cycle through all 64K of memory.

NOTE 2 Interrupts can be accepted after each transfer is complete.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	RESET = Ø.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

Example: LD HL,468ØH
LD DE,2435H
LD BC,Ø3H
LDDR

If the contents of Register Pair HL are 46 8Ø, the contents of Register Pair DE are 24 35 and the contents of Register Pair BC are ØØØ3, this instruction will transfer the contents of memory location 46 8Ø to memory location 24 35, then decrement the contents of Register Pairs HL to 46 7F, DE to 24 34 and BC to ØØ Ø2 and RESET Flags H, P/V and N = Ø. Because the new contents of Register Pair BC = Ø, the Program Counter will be decremented by 2 (which returns it to the address of this instruction) and the LDDR instruction is repeated using the new memory location addresses in Register Pairs HL and DE.

Addressing Mode: Indirect.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
BC ≠ Ø	5	21	1Ø.5
BC = Ø	4	16	8

LDI

Data transfer between memory locations. Increment source and destination addresses.

Object Code:

	Hex	Decimal
LDI	ED A∅	237 16∅

Description: Transfers one byte of data from the memory location whose address is held in Register Pair HL to the memory location whose address is held in Register Pair DE, then increments Register Pairs HL and DE and decrements Register Pair BC (which is used as a byte counter).

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the new contents of Register Pair BC = ∅, otherwise RESET = ∅.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Not affected.

Cont.

Example:
```
LD HL,4567H
LD DE,32A5H
LD BC,1628H
LDI
```

If the contents of Register Pair HL are 45 67 and the contents of Register Pair DE are 32 A5 and the contents of Register Pair BC are 16 28, this instruction will transfer the contents of memory location 45 67 to memory location 32 A5, leaving the same value in location 45 67, then increment the contents of Register Pairs HL and DE to 45 68 and 32 A6 respectively and decrement the contents of Register Pair BC to 16 27. Flags H and N will be RESET = Ø and Flag P/V will be SET = 1.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

LDIR

Data transfer between memory locations until counter is zero. Increment source and destination registers.

Object Code:

	Hex	Decimal
LDIR	ED BØ	237 176

Description: Transfers one byte of data from the memory location whose address is held in Register Pair HL to the memory location whose address is held in Register Pair DE, then increments Register Pairs HL and DE and decrements Register Pair BC (which is used as a byte counter). If the new contents of Register Pair BC = Ø the instruction is terminated, otherwise the Program Counter (PC) is decremented by 2 and the instruction is repeated, using the new addresses in Register Pairs HL and DE.

NOTE 1 If the initial value of Register Pair BC is set to zero, this instruction will loop through all 64K of memory.

NOTE 2 Interrupts can be accepted after each transfer is complete.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	RESET = Ø.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

Example: LD HL,4668H
LD DE,2332H
LD BC,Ø11H
LDIR

If the contents of Register Pair HL are 46 68, the contents of Register Pair DE are 23 32 and the contents of Register Pair BC are ØØ 11, this instruction will transfer the contents of memory location 46 68 to memory location 23 32, leaving the same value in location 46 68, then increment the contents of Register Pairs HL and DE to 46 69 and 23 33 respectively and decrement the contents of Register Pair BC to ØØ 1Ø. Flags H, P/V and N will be RESET = Ø.

Addressing Mode: Indirect.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
BC ≠ Ø	5	21	1Ø.5
BC = Ø	4	16	8

NEG

Description: Negates the contents of the Accumulator by subtracting those contents from zero (two's complement) and storing the result in the Accumulator.
NOTE: If the contents of the Accumulator are 8∅(Hex.), those contents will not be changed by this instruction.

No. of Bytes: 2

Object Code (Hex.): ED 44 Decimal: 237 ∅68

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if the original value of the Accumulator was 8∅(Hex.), otherwise RESET = ∅.
Subtract	N	1	SET = 1.
Carry	C	∅	SET = 1 if the original value of the Accumulator was NOT ∅∅, otherwise RESET = ∅.

Example: LD A,∅2H
NEG

If the original contents of the Accumulator are ∅2(Hex.), this instruction will make those contents equal FE(Hex.), then SET Flags S, N and C = 1 and RESET Flags Z, H and P/V = ∅.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

NOP

Description: Nothing occurs for one Machine Cycle.

No. of Bytes: 1

Object Code (Hex.): ØØ Decimal: ØØØ

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

OR n

OR Accumulator with data n, where n is an 8 bit integer.

Object Code:

Where n is an 8 Bit integer, specified in the instruction.

	Hex	Decimal
OR n	F6 n	246 n

Description: Performs a Bit by Bit logical OR between the contents of the Accumulator and the integer n, then stores the result in the Accumulator.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result :s negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	RESET = Ø.

Cont.

Example: LD A,6AH
OR 15H

If the contents of the Accumulator are 6AH (Bit Pattern ∅11∅1∅1∅) and n in the intructions is 15H (Bit Pattern ∅∅∅1∅1∅1) the result will be 7FH (Bit Pattern ∅1111111) and this is stored in the Accumulator, while Flags S, Z, P/V, N, H and C are RESET = ∅.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

OR r

Or Register r with the Accumulator where r is any of the Registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
OR A	B7	183
OR B	BØ	176
OR C	B1	177
OR D	B2	178
OR E	B3	179
OR H	B4	18Ø
OR L	B5	181

Description: Performs a Bit by Bit logical OR between the contents of the Accumulator and the contents of specified register, then stores the result in the Accumulator leaving the contents of the specified register unaltered. Note that this instruction will never change the value of the A register, but will change the value of some of the flags. As with AND A, OR A is used only for setting flags to useful values.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	RESET = Ø.

Cont.

Example: LD A,21H
OR A

If the contents of the Accumulator are 21(Hex.) the logical OR is performed as follows:

	Hex	Binary
Accumulator	21	ØØ1ØØØØ1
Accumulator	21	ØØ1ØØØØ1
Result	21	ØØ1ØØØØ1

Flag P/V is SET = 1 and Flags S, Z, N, H and C are RESET = Ø.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

OR (HL)

Description: Performs a Bit by Bit logical OR between the contents of the Accumulator and the contents of a memory location whose address is held in Register Pair HL. The contents of both Register Pair HL and the memory location remain unaltered.

No. of Bytes: 1

Object Code (Hex.): B6 Decimal: 182

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	RESET = Ø.

```
Example: LD A,24H
         LD HL,A367H
         LD (HL),12H
         OR (HL)
```

If the contents of the Accumulator are 24(Hex.), the contents of Register Pair HL are A3 67 and the contents of memory location A3 67 are 12, the logical OR is performed as follows:

	Hex	Binary
Accumulator	24	ØØ1ØØ1ØØ
Location A3 67	12	ØØØ1ØØ1Ø
Result	36	ØØ11Ø11Ø

Flag P/V is SET = 1 while Flags S, Z, N, H and C are RESET = Ø.

Addressing Mode: Indirect.

Cont.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

OR (IX + d)
OR (IY + d)

Description: Performs a Bit by Bit logical OR between the contents of the Accumulator and the contents of a memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), then stores the result in the Accumulator. The contents of both Index Register IX and IY and the memory location remain unaltered.

No. of Bytes: 3

Object Code:

	Hex	Decimal
OR (IX + d)	DD B6 d	221 182 d
OR (IY + d)	FD B6 d	253 182 d

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	RESET = ∅.

Cont.

```
Example:  LD IX,21Ø5H
          LD HL,21Ø8H
          LD (HL),12H
          LD A,ØA3H
          OR (IX+3)
```

If the contents of Index Register IX are 21 Ø5 and d in the instruction is 3, the required memory location is 21 Ø8. If the contents of the Accumulator are A3 and the contents of memory location 21 Ø8 are 12, the logical OR performs as follows:

	Hex	Binary
Accumulator	A3	1Ø1ØØØ11
Location 21 Ø8	12	ØØØ1ØØ1Ø
Result	B3	1Ø11ØØ11

Flag S is SET = 1, while Flags Z, H, P/V, N and C are RESET = Ø.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

OTDR

Description: Outputs, to the device identified by the contents of Register C, the contents of a memory location whose address is held in register Pair HL, then decrements register B (which is used as a byte counter) and Register Pair HL. If Register B is then <> ∅, the Program Counter (PC) is decremented by 2 and the instruction is repeated.

NOTE: Register C supplies Bits ∅ to 7 to the Address Bus and Register B provides Bits 8 to 15 (after Register B is decremented.

No. of Bytes: 2

Object Code (Hex.): ED BB Decimal: 237 187

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not known.
Zero	Z	6	SET = 1
—	—	5	Not used.
Half Carry	H	4	Not known.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not known.
Subtract	N	1	SET = 1.
Carry	C	∅	Not affected.

Example:
```
LD C,21H
LD HL,43A1H
LD B,1
OTDR
```

If Register C contains 21(Hex.) and Register Pair HL contains 43 A1, this instruction will output the contents of memory location 43 A1 to device number 21H, then decrements Register B and Register Pair HL. If the new contents of Register B = ∅, the instruction is terminated, otherwise the Program Counter reverts to the address of the instruction which is then repeated (Register Pair HL will now contain 43 A∅).

Addressing Mode: External.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
B <> ∅	5	21	1∅.5
B = ∅	4	16	8

OTIR

Description: Outputs, to the device identified by the contents of Register C, the contents of a memory location whose address is held in register Pair HL, then decrements register B (which is used as a byte counter) and increments Register Pair HL. If Register B is then <> Ø, the Program Counter (PC) is decremented by 2 and the instruction is repeated.

NOTE: Register C supplies Bits Ø to 7 to the Address Bus and Register B provides Bits 8 to 15 (after Register B is decremented).

No. of Bytes: 2

Object Code (Hex.): ED B3 Decimal: 237 179

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not known.
Zero	Z	6	SET = 1
—	—	5	Not used.
Half Carry	H	4	Not known.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not known.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

Example:
```
LD C,8H
LD HL,3564H
LD B,1ØH
OTIR
```

If Register C contains Ø8(Hex.) and Register Pair HL contains 35 64, this instruction will output the contents of memory location 35 64 to device number 8, then decrements Register B and increments Register Pair HL to 35 65. If the new contents of Register B are zero, the instruction is terminated, otherwise theProgram Counter reverts to the address of this instruction which is then repeated using the new memory location address which is now held in Register Pair HL.

Addressing Mode: External.

Cont.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
B <> Ø	5	21	1Ø.5
B = Ø	4	16	8

OUT (C),r

Output from Register r where r is any of the registers A, B, C, D, E, H or L..

Object Code:

	Hex	Decimal
OUT (C),A	ED 79	237 113
OUT (C),B	ED 41	237 ∅65
OUT (C),C	ED 49	237 ∅73
OUT (C),D	ED 51	237 ∅81
OUT (C),E	ED 59	237 ∅89
OUT (C),H	ED 61	237 ∅97
OUT (C),L	ED 69	237 1∅5

Description: Output from Register r to I/O Port addressed by Register C.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

```
Example: LD A,18H
         LD C,∅AH
         OUT (C),A
```

If the contents of the Accumulator are 18(Hex.) and the contents of Register C are ∅A(Hex.), OUT (C),A will output 18(Hex.) to Port number ∅AH, leaving the original values in both the Accumulator and Register C.

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	12	6

OUT (n),A

Output A from the Accumulator to Port n, where n is any value from Ø–255.

Object Code: (Hex.) D3 n   Decimal: 211 n

Description: Output from the Accumulator to Port n.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

```
Example:  LD A,18H
          OUT (ØAH),A
```

If the contents of the Accumulator are 18(Hex.) and the value of n is ØA(Hex.), this instruction will output 18(Hex.) to Port number ØAH leaving the original value in the Accumulator.

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	11	5.5

OUTD

Description: Outputs the contents of a memory location, whose address is held in Register Pair HL, to the Port (one of 256) whose address is held in Register C. The contents of the memory location and Register C remain unchanged while the contents of Register B (which is used as a byte counter) and Register Pair HL are both decremented.

No. of Bytes: 2

Object Code (Hex.): ED AB Decimal: 237 171

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not known.
Zero	Z	6	SET = 1 if the new value of Register B = Ø, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	Not known.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not known.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

```
Example: LD HL,2134H
         LD C,Ø8H
         LD (HL),12H
         LD B,Ø
         OUTD
```

If the contents of Register Pair HL are 21 34 and the contents of Register C are Ø8(Hex.), the requirement is for the contents of memory location 21 34 to be output to Port number 8. If thecontents of memory location 21 34 are 12(Hex.), this instruction will output 12(Hex.) to Port number 8, decrement Register Pair HL to 21 33, decrement Register B, SET Flag N = Ø and either SET Flag Z = 1 (if the new value ofRegister B = Ø) or RESET that flag = Ø.

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

OUTI

Description: Outputs the contents of a memory location, whose address is held in Register Pair HL, to the Port (one of 256) whose address is held in Register C. The contents of the memory location and Register C remain unchanged while the contents of Register B (which is used as a byte counter) are decremented, and Register Pair HL is incremented.

No. of Bytes: 2

Object Code (Hex.): ED A3 Decimal: 237 163

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not known.
Zero	Z	6	SET = 1 if the new value of Register B = Ø, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	Not known.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not known.
Subtract	N	1	SET = 1.
Carry	C	Ø	Not affected.

Example:
```
LD HL,2134H
LD (HL),12H
LD C,Ø8H
LD B,1
OUTI
```

If the contents of Register Pair HL are 21 34, and the contents of Register C are Ø8(Hex.), the requirement is for the contents of memory location 21 34 to be output to Port number 8. If the contents of memory location 21 34 are 12(Hex.), this instruction will output 12(Hex.) to Port number 8, increment Register Pair HL to 21 35, decrement Register B, SET Flag N = Ø and either SET Flag Z = 1 (if the new value of Register B = Ø) or RESET that flag = Ø.

Addressing Mode: External.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	16	8

POP rr

Read from top of Stack into Register Pair rr where rr is any of the Register Pairs AF, BC, DE or HL.

Object Code:

	Hex	Decimal
POP AF	F1	241
POP BC	C1	193
POP DE	D1	2Ø9
POP HL	E1	225

Description: Loads the contents of the memory location, whose address is held in the Stack Pointer (SP), into the Lower Order Byte of the designated Register Pair and the contents of the next memory location (SP+1) into the Higher Order byte of that Register Pair. The Stack Pointer is incremented twice while the contents of both memory locations remain unaltered.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

```
Example: LD BC,Ø568H
         LD (1234),BC
         LD SP,1234
         POP AF
```

If the Stack Pointer (SP) contains 12 34, and memory location 12 34 contains 68, that value (68) is loaded into Register F then the Stack Pointer is incremented to 12 35 and the contents of memory location 12 35 (say Ø5H), loaded into the Accumulator after which the Stack Pointer is incremented again to 12 36.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	1Ø	5

POP IX
POP IY

Read from top of Stack into Index Register.

Object Code:

	Hex	Decimal
POP IX POP IY	DD E1 FD E1	221 225 253 225

Description: Loads the contents of the memory location, whose address is held in the Stack Pointer (SP), into the Lower Order Byte of the designated Index Register and the contents of the next memory location (SP+1) into the Higher Order byte of that Index Register. The Stack Pointer is incremented twice while the contents of both memory locations remain unaltered.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example:
```
LD BC,3714H
LD (4589H),BC
LD SP,4589H
POP IX
```

If the Stack Pointer contains 45 89, and memory location 45 89 contains 14, that value (14) is loaded into the Lower Order byte of Index Register IX then the Stack Pointer is incremented to 45 8A and the contents of memory location 45 8A loaded into the Higher Order byte of Index Register IX. If the contents of location 45 8A are 37, the contents of Index Register IX will be 37 14. The Stack Pointer is then again incremented to 45 8B.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	14	7

PUSH rr

Write contents of Register Pair rr to the top of the Stack, where rr can be AF, BC, DE or HL.

Object Code:

	Hex	Decimal
PUSH AF	F5	245
PUSH BC	C5	197
PUSH DE	D5	213
PUSH HL	E5	229

Description: Pushes the contents of the specified Register Pair on to the top of the memory Stack. The Stack Pointer is decremented and the contents of the Higher Order byte of the Register Pair loaded into the memory location whose address is now held in the Stack Pointer (SP), then the Stack Pointer is again decremented and the contents of the Lower Order byte of the Register Pair loaded into the memory location whose address is the new contents of the Stack Pointer. The contents of the Register Pair remain unaltered.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example: LD SP,3462H
LD BC,AABBH
PUSH BC

If the contents of the Stack Pointer are 34, 62, PUSH BC will decrement this to 34 61 and load the contents of the B Register into memory location 34 61, decrement the Stack Pointer again to 34 6Ø and load the contents of the C Register into memory location 34 6Ø.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	11	5.5

PUSH IX
PUSH IY

Write contents of Index Register to the top of the Stack.

Object Code:

	Hex	Decimal
PUSH IX PUSH IY	DD E5 FD E5	221 229 253 229

Description: Pushes the contents of the specified Index Register on to the top of the memory Stack. The Stack Pointer (SP) is decremented and the contents of the Higher Order byte of the Index Register loaded into the memory location whose address is now held in the Stack Pointer, then the Stack Pointer is again decremented and the contents of the Lower Order byte of the Index Register loaded into the memory location whose address is the new contents of the Stack Pointer. The contents of the Index Register remain unaltered.

No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example:
```
LD SP,5834H
LD IX,∅AABBH
PUSH IX
```

If the contents of the Stack Pointer are 58 34, this instruction will decrement this to 58 33 and load the contents of the Higher Order byte of Index Register IX into the memory location 58 33, decrement the Stack Pointer again, to 58 32, then load the contents of the Lower Order byte of Index Register IX into memory location 58 32.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

RES b,r

No. of Bytes: 2

Object Code (Hex.): CB xx Decimal: 2Ø3 yyy

Where: b is the specified Bit (Range Ø — 7) to be RESET.
r is the nominated Register (A, B, C, D, E, H or L) containing b.
xx and yyy are taken from the table below:

	A		B		C		D		E		H		L	
Bit	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy
Ø	87	135	8Ø	128	81	129	82	13Ø	83	131	84	132	85	133
1	8F	143	88	136	89	137	8A	138	8B	139	8C	14Ø	8D	141
2	97	151	9Ø	144	91	145	92	146	93	147	94	148	95	149
3	9F	159	98	152	99	153	9A	154	9B	155	9C	156	9D	157
4	A7	167	AØ	16Ø	A1	161	A2	162	A3	163	A4	164	A5	165
5	AF	175	A8	168	A9	169	AA	17Ø	AB	171	AC	172	AD	173
6	B7	183	BØ	176	B1	177	B2	178	B3	179	B4	18Ø	B5	181
7	BF	191	B8	184	B9	185	BA	186	BB	187	BC	188	BD	189

Description: RESETS = Ø the specified Bit in the nominated Register.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD E,ØFFH
RES 3,E

The Source Code statement RES 3,E, will produce the Object Code instruction CB 9B(Hex.) which will RESET = Ø Bit 3 in Register E.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

RES b, (HL)

Description: RESETS = Ø the specified Bit in the memory location whose address is held in Register Pair HL.

No. of Bytes: 2

Object Code (Hex.): CB xx Decimal: 2Ø3 yyy

Where b is the specified Bit (range Ø to 7) to be RESET.

xx and yyy are taken from the table below:

Bit	xx	yyy
Ø	86	134
1	8E	142
2	96	15Ø
3	9E	158
4	A6	166
5	AE	174
6	B6	182
7	BE	19Ø

Description: RESETS = Ø the specified Bit in the memory location whose address is held in Register Pair HL.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LP HL,1ØØØH
          LD (HL),ØFFH
          RES 5,(HL)
```

The Source Code statement RES 5,(HL), will produce the Object Code instruction CB AE(Hex.) which will RESET = Ø Bit 5 in the memory location whose address is held in Register Pair HL.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

RES b,(IX+d)
RES b,(IY+d)

Description: RESETS = ∅ the specified bit in the memory location whose address is held in the specified Index Register (modified by displacement d, which is specified in the instruction).

No. of Bytes:

Object Code:

	Hex	Decimal
RES b,(IX+d) RES b,(IY+d)	DD CB d xx FD CB d xx	221 203 d yyy 253 2∅3 d yyy

Where:

b is the specified bit (range ∅ to 7) to be RESET.
d is the required displacement from the memory location whose address is held in the specified Index Register.
xx and yyy are taken from the table below.

Bit	xx	yyy
∅	86	134
1	8E	142
2	96	15∅
3	9E	158
4	A6	166
5	AE	174
6	B6	182
7	BE	19∅

Cont.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected
Carry	C	∅	Not affected.

```
Example:  LD HL,4569H
          LD (HL),∅FFH
          LD IX,4567H
          RES 4,(IX+2)
```

If the contents of Index Register IX are 4567, and d in the instruction is 2, the required memory location is 4569. The Source Code statement RES 4,(IX+2) will produce the Object Code instruction DD CB 2 A6(Hex.) which will RESET = ∅ bit 4 in memory location 4569.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	µsec @ 2 MHz.
6	23	11.5

RET

Return from subroutine.

Object Code:

	Hex	Decimal
RET	C9	2Ø1

Description: Returns control to the main program after a sub-routine has been called and followed. When the sub-routine was called the contents of the Program Counter (PC) at that time were stored in two consecutive memory locations and the address of the higher of those locations was placed in the Stack Pointer (SP). This instruction loads the contents of the memory location whose address is held in the Stack Pointer into the Lower Order byte of the Program Counter, then increments the Stack Pointer and loads the contents of the memory location now pointed to by the Stack Pointer into the Higher Order byte of the Program Counter then the Stack Pointer is incremented again.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example: If the contents of the Stack Pointer are 21 14, and the contents of memory location 21 14 are 3A, the value 3A is loaded into the Lower Order byte of the Program Counter, the Stack Pointer is incremented to 21 15 and the contents of memory location 21 15 (say 48) are loaded into the Higher Order byte of the Program Counter, making the contents of the Program Counter 48 3A. The Stack Pointer is then again incremented to 21 16. The next instruction will be fetched from memory location 48 3A.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
3	10	5

RET cc

Return from subroutine if condition cc is satisfied where cc can be NZ, Z, NC, C, PO, PE, P or M.

Object Code:

	Hex	Decimal
RET NZ	CØ	192
RET Z	C8	2ØØ
RET NC	DØ	2Ø8
RET C	D8	216
RET PO	EØ	224
RET PE	E8	232
RET P	FØ	24Ø
RET M	F8	248

Description: Conditionally returns control to the calling routine provided the condition is met. If this condition is not met, this instruction is ignored. If the condition is met, i.e. TRUE, this instruction loads the contents of the memory location whose address is held in the Stack Pointer into the Lower Order byte of the Program Counter, increments the Stack Pointer then loads the contents of the memory location now pointed to by the Stack Pointer into the Higher Order byte of the Program Counter, then again increments the Stack Pointer.

Condition	Flag
Non zero	Z
Zero	Z
Non carry	C
Carry	C
Parity odd	P/O
Parity even	P/O
Sign positive	S
Sign negative	S

No. of Bytes: 1

Cont.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Assuming that the C Flag is SET = 1, if the contents of the Stack Pointer are 65 23, the contents of memory location 65 23 are 4B and the contents of memory location 65 24 are 87, RET C will load 4B into the Lower Order byte of the Program Counter, increment the Stack Pointer to 65 24, load 87 into the Higher Order byte of the Program Counter and again increment the Stack Pointer (to 65 25). The new contents of the Program Counter will then be 87 4B, and the next instruction will be fetched from that location.

```
Example: LD BC,874BH
         LD (6523H),BC
         LD SP,6523H
         SCF
         RET C
```

Addressing Mode: Indirect.

Timing:

	M Cycles	T States	μsec @ 2 MHz.
Condition Met	3	11	5.5
Condition Not Met	1	5	2.5

RETI

Description: Returns control to the calling routine after an interrupt has been received and serviced. Loads the contents of the memory location whose address is held in the Stack Pointer to the Lower Order byte of the Program Counter, increments the Stack Pointer, then loads the contents of the memory location now pointed to by the Stack Pointer into the Higher Order byte of the Program Counter. Finally, the Stack Pointer is again incremented and the IFF1 and IFF2 Flip Flops are RESET = Ø.

NOTE: An EI instruction must be obeyed prior to the RETI instruction in order to re-enable interrupts.

No. of Bytes: 2

Object Code (Hex.): ED 4D   Decimal: 237 Ø77

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

```
Example: LD SP,436AH
         LD BC,78A3H
         LD (436AH),BC
         EI
         RETI
```

If the Stack Pointer contains 43 6A, the contents of memory location 43 6A are A3 and the contents of memory location 43 6B are 78, this instruction will load A3 into the Lower Order byte of the Program Counter, increment the Stack Pointer to 43 6B, load 78 into the Higher Order byte of the Program Counter, then again increment the Stack Pointer (to 43 6C). The new contents of the Program Counter will be 78 A3, and the next instruction will be fetched from that memory location.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	14	7

RETN

Description: Returns control to the main program after a Non-Maskable Interrupt has been received and serviced. Loads the contents of the memory location whose address is held in the Stack Pointer to the Lower Order byte of the Program Counter, increments the Stack Pointer, then loads the contents of the memory location now pointed to by the Stack Pointer into the Higher Order byte of the Program Counter. The Stack Pointer is again incremented, then the contents of the IFF2 Flip-Flop (Storage flip-flop) are copied into the IFF1 Flip-Flop, restoring it to the condition which existed before the Non-Maskable Interrupt.

No. of Bytes: 2

Object Code (Hex.): ED 45 Decimal: 237 ∅69

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	∅	Not affected.

```
Example:  LD SP,3179H
          LD BC, ∅B42H
          LD (3179H),BC
          RETN
```

If the Stack Pointer contains 31 79, the contents of memory location 31 79 are 42 and the contents of memory location 31 7A are ∅B, this instruction will load 42 into the Lower Order byte of the Program Counter, increment the Stack Pointer to 31 7A, load ∅B into the Higher Order byte of the Program Counter, then again increment the Stack Pointer (to 31 7B). The contents of the IFF2 Flip-Flop will be copied in to the IFF1 FLip-FLop. The new contents of the Program Counter will be ∅B 42 and the next instruction will be fetched from that memory location.

Cont.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	14	7

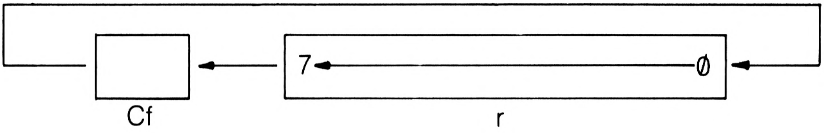
RL r

Rotate Register r left where r is any of the registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
RL A	CB 17	2Ø3 23
RL B	CB1Ø	2Ø3 16
RL C	CB11	2Ø3 17
RL D	CB12	2Ø3 18
RL E	CB13	2Ø3 19
RL H	CB14	2Ø3 2Ø
RL L	CB15	2Ø3 21

Description: Rotate contents of Register r left one bit through carry status.



No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit 7 of Register B.

Cont.

Example: LD B,3AH
SCF
CCF
RL B

If Register B contains 3A(Hex.) and the C Flag = Ø, the effect of RL B will be:

	Register B		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	3A	Ø Ø 1 1 1 Ø 1 Ø	Ø
New Contents	74	Ø 1 1 1 Ø 1 Ø Ø	Ø

Flags S, Z, H and N are RESET = Ø, Flag P/V is SET = 1 and Flag C will contain the Ø previously held in Bit 7 of Register B.

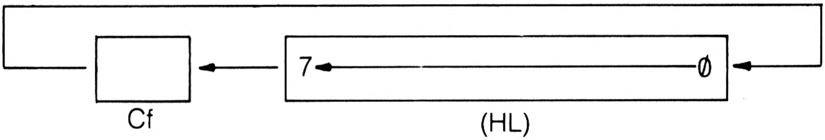
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

RL (HL)

Description: Rotates Left the contents of the memory location whose address is held in Register Pair HL through the C (Carry) Flag in the Flag Register. Each Bit is shifted Left one position, i.e. the contents of Bit Ø are moved into Bit 1, the contents of Bit 1 are moved into Bit 2, etc. The contents of Bit 7 are moved into the C Flag and the previous contents of the C Flag are moved into Bit Ø.



No. of Bytes: 2

Object Code (Hex.): CB 16 Decimal: 2Ø3 Ø22

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit 7 of the memory location.

Cont.

Example: LD HL,2A15H
LD (HL),58H
RL (HL)

If Register Pair HL contains 2A 15, the contents of memory location 2A 15 are 58, and the C Flag = 1, the effect of this instruction will be:

	Memory Location									
		Bits								C
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	58	Ø	1	Ø	1	1	Ø	Ø	Ø	1
New Contents	B1	1	Ø	1	1	Ø	Ø	Ø	1	Ø

Flags Z, H and N are RESET = Ø, Flags S and P/V are SET = 1 and Flag C will contain the Ø previously held in Bit 7 of the memory location.

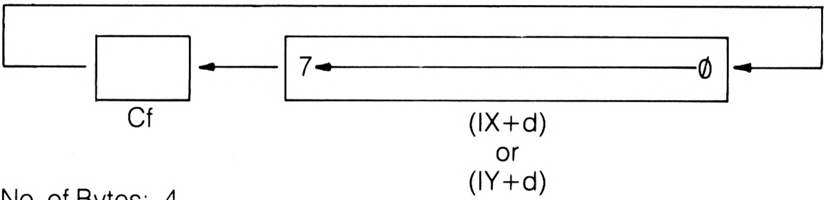
Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

RL (IX + d)
RL (IY + d)

Description: Rotates Left the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction) through the C (Carry) Flag in the Flag Register. Each Bit is shifted Left one position, i.e. the contents of Bit Ø are moved into Bit 1, the contents of Bit 1 are moved into Bit 2, etc. The contents of Bit 7 are moved into the C Flag and the previous contents of the C Flag are moved into Bit Ø.



No. of Bytes: 4

Object Code

	Hex	Decimal
RL (IX + d) RL (IY + d)	DD CB d 16 FD CB d 16	221 2Ø3 d Ø22 253 2Ø3 d Ø22

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit 7 of the memory location.

Cont.

```
Example: LD IX,5643H
         LD A,89
         LD (5649H),A
         SCF
         CCF
         RL (IX+6)
```

If the contents of index Register IX are 56 43, and d in the instruction is Ø6(Hex.), the required memory location is 56 49. If the contents of that memory location are 89 and the C Flag = Ø, the effect of this instruction will be:

	Memory Location		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	89	1 Ø Ø Ø 1 Ø Ø 1	Ø
New Contents	12	Ø Ø Ø 1 Ø Ø 1 Ø	1

Flags S, Z, H and N are RESET = Ø, Flag P/V is SET = 1 and Flag C will contain the 1 previously held in Bit 7 of the memory location.

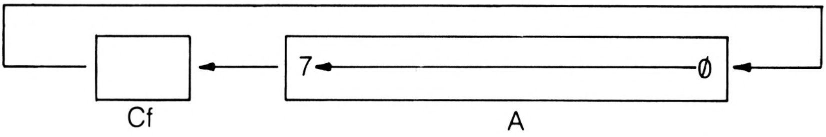
Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

RLA

Description: Rotates Left the contents of the Accumulator through the C (Carry) Flag. Each Bit is shifted Left one position, i.e. the contents of Bit Ø are moved into Bit 1, the contents of Bit 1 are moved into Bit 2, etc. The contents of Bit 7 are moved into the C Flag and the previous contents of the C Flag are moved into Bit Ø.



NOTE: This instruction has the same effect as instruction RL A but is faster in execution, and has a different effect on the Flag Register. It is provided for compatibility with the Intel 8Ø8Ø.

No. of Bytes: 1

Object Code (Hex.): 17 Decimal: Ø23

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit 7 of the Accumulator.

Cont.

```
Example: LD A,57
         SCF
         RLA
```

If the contents of the Accumulator are 57, and the C Flag = 1, the effect of this instruction will be:

		Accumulator								
		Bits								C
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	57	Ø	1	Ø	1	Ø	1	1	1	1
New Contents	AF	1	Ø	1	Ø	1	1	1	1	Ø

Flags H and N will be RESET = Ø, and Flag C will contain the Ø previously held in Bit 7 of the Accumulator.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

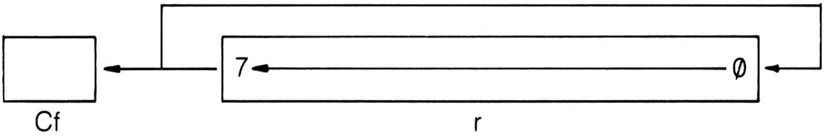
RLC r

Rotate contents of Register r left circular where r is any of the registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
RLC A	CB Ø7	2Ø3 ØØ7
RLC B	CB ØØ	2Ø3 ØØØ
RLC C	CB Ø1	2Ø3 ØØ1
RLC D	CB Ø2	2Ø3 ØØ2
RLC E	CB Ø3	2Ø3 ØØ3
RLC H	CB Ø4	2Ø3 ØØ4
RLC L	CB Ø5	2Ø3 ØØ5

Description: Rotate contents of Register r left circular one bit, copying bit 7 into the carry status. That is, bit 7 is copied into bit Ø, and also into the carry flag.



No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit 7 of the Accumulator.

Cont.

Example: LD A,ØB6H
RLC A

If the contents of the Accumulator are B6, the effect of this instruction will be:

	Accumulator		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	B6	1 Ø 1 1 Ø 1 1 Ø	?
New Contents	6D	Ø 1 1 Ø 1 1 Ø 1	1

Flags S, Z, H, P/V and N are RESET = Ø and Flag C will contain the data previously held in Bit 7 of the Accumulator, which is identical to that now held in Bit Ø of the Accumulator.

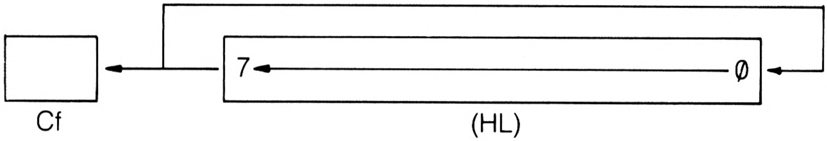
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

RLC (HL)

Description: Rotates Left the contents of the memory location whose address is held in Register Pair HL. Each Bit is shifted Left one position, i.e. the contents of Bit ∅ are moved into Bit 1, the contents of Bit 1 are moved into Bit 2, etc. The contents of Bit 7 are moved into Bit ∅ *and* into the C (Carry) Flag in the Flag Register.



No. of Bytes: 2

Object Code (Hex.): CB ∅6 Decimal: 2∅3 ∅∅6

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Contains the data previously held in Bit 7 of the memory location.

Cont.

Example: LD HL,1745H
LD (HL),5AH
RLC (HL)

If the contents of Register Pair HL are 17 45, and the contents of memory location 17 45 are 5A, the effect of this instruction will be:

	Memory Location									
		Bits								C
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	5A	Ø	1	Ø	1	1	Ø	1	Ø	?
New Contents	B4	1	Ø	1	1	Ø	1	Ø	Ø	Ø

Flags Z, H and N are RESET = Ø, Flags S and P/V are SET = 1 and Flag C will contain the data previously held in Bit 7 of the memory location, which is identical to that now held in Bit Ø of the memory location.

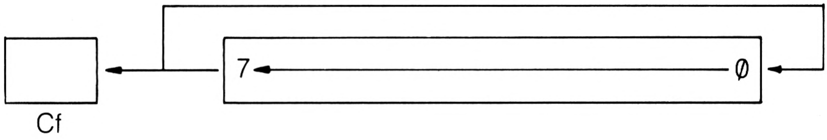
Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

RLC (IX + d)
RLC (IY + d)

Description: Rotates Left the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction). Each Bit is shifted Left one position. i.e. the contents of Bit ∅ are moved into Bit 1, the contents of Bit 1 are moved into Bit 2, etc. The contents of Bit 7 are moved into Bit ∅ *and* into the C Flag in the Flag Register.



No. of Bytes: 4

Object Code

	Hex	**Decimal**
RLC (IX + d) RLC (IY + d)	DD CB d ∅6 FD CB d ∅6	221 2∅3 d ∅∅6 253 2∅3 d ∅∅6

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Contains the data previously held in Bit 7 of the memory location.

Cont.

```
Example:  LD IX,4521H
          LD A,27H
          LD (452BH),A
          RLC (IX+ØAH)
```

If the contents of Index Register IX are 45 21, and d in the instruction is ØA(Hex.), the required memory location is 45 2B. If the contents of Memory Location 45 2B are 27(Hex.) the effect of this instruction will be:

		Memory Location	
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	27	Ø Ø 1 Ø Ø 1 1 1	?
New Contents	4E	Ø 1 Ø Ø 1 1 1 Ø	Ø

Flags S, Z, H and N are RESET = Ø, Flag P/V will be SET = 1 and Flag C will contain the data previously held in Bit 7 of the memory location, which is identical to that now held in Bit Ø of the memory location.

Addressing Mode: Indexed.

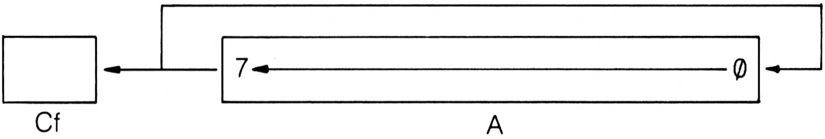
Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

RLCA

Description: Rotates Left the contents of the Accumulator. Each Bit is shifted Left one position, i.e. the contents of Bit ∅ are moved into Bit 1, the contents of Bit 1 are moved into Bit 2, etc. The contents of Bit 7 are moved into Bit ∅ *and* into the C (Carry) Flag in the Flag Register.

NOTE: This instruction is identical to RLC A, except for the effect on the Flag Register, but is faster in execution. It is provided for compatibility with the Intel 8∅8∅.



No. of Bytes: 1

Object Code (Hex.): ∅7 Decimal: ∅∅7

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Contains the data previously held in Bit 7 of the Accumulator.

Cont.

Example: LD A,37H
RLCA

If the contents of the Accumulator are 37(Hex.), the effect of this instruction will be:

	Accumulator		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	37	Ø Ø 1 1 Ø 1 1 1	?
New Contents	6E	Ø 1 1 Ø 1 1 1 Ø	Ø

Flags H and N are RESET = Ø and Flag C will contain the data previously held in Bit 7 of the Accumulator, which is identical to that now held in Bit Ø of the Accumulator.

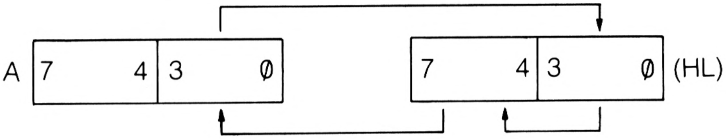
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

RLD

Description: Rotates Left Decimal the Lower Order 4 bits of the Accumulator with the Higher Order 4 bits and the Lower Order 4 bits of the memory location whose address is held in Register Pair HL. The Higher Order 4 bits of the specified location is moved into the Lower Order 4 bits of the Accumulator, the Lower Order 4 bits of the Accumulator is moved into the Lower Order 4 bits of the memory location, and the Lower Order 4 bits of the memory location is moved into the Higher Order 4 bits of the same memory location.



No. of Bytes: 2

Object Code (Hex.): ED 6F Decimal: 237 111

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result in the Accumulator is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result in the Accumulator is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if for Parity Even in the Accumulator result, RESET = Ø for Parity Odd in the Accumulator result.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

Example: LD HL1ØØØH
LD (HL),28H
LD A,6EH
RLD

If the contents of the Accumulator are 6E(Hex.) and the contents of the nominated memory location are 28(Hex.) the effect of this instruction will be:

Original Contents		New Contents	
Accumulator	Location	Accumulator	Location
6 E	28	62	8 E

Flags S, Z, H, P/V and N are RESET = Ø.

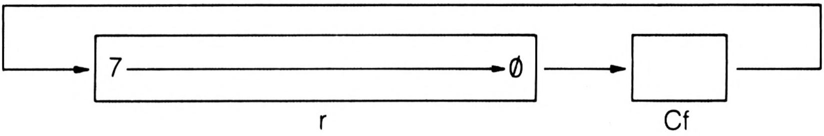
Addressing Mode: Indirect

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	18	9

RR r

Description: Rotates Right the contents of Register r through the C (Carry) Flag in the Flag Register. Each Bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit ∅ are moved into the C Flag and the previous contents of the C Flag are moved into Bit 7.



No. of Bytes: 2

Object Code

	Hex	Decimal
RR A	CB 1F	2∅3 ∅31
RR B	CB 18	2∅3 ∅24
RR C	CB 19	2∅3 ∅25
RR D	CB 1A	2∅3 ∅26
RR E	CB 1B	2∅3 ∅27
RR H	CB 1C	2∅3 ∅28
RR L	CB 1D	2∅3 ∅29

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Contains the data previously held in Bit ∅ of the memory location.

Cont.

```
Example:  LD B,3AH
          SCF
          CCF
          RR B
```

If Register B contains 3A(Hex.) and the C Flag = Ø, the effect of this instruction will be:

	Register B		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	3A	Ø Ø 1 1 1 Ø 1 Ø	Ø
New Contents	1D	Ø Ø Ø 1 1 1 Ø 1	Ø

Flags S, Z, H and N are RESET = Ø, Flag P/V is SET = 1 and Flag C contains the Ø previously held in Bit Ø of Register B.

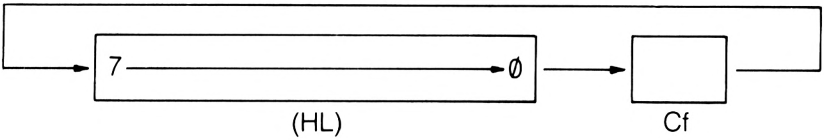
Addressing Mode: Implicit.

Timing:

M Cycles	T States	usec @ 2 MHz.
2	8	4

RR (HL)

Description: Rotates Right the contents of the memory location whose address is held in Register Pair HL through the C (Carry) Flag in the Flag Register. Each Bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit ∅ are moved into the C Flag and the previous contents of the C Flag are moved into Bit 7.



No. of Bytes: 2

Object Code (Hex.): CB 1E Decimal: 2∅3 ∅3∅

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Contains the data previously held in Bit ∅ of the memory location

Cont.

Example:
```
LD HL,2A15H
LD (HL),58H
SCF
RR (HL)
```

If Register Pair HL contains 2A 15(Hex.), the contents of memory location 2A 15 are 58(Hex.) and the C Flag = 1, the effect of this instruction will be:

	Memory Location		C
		Bits	
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	58	Ø 1 Ø 1 1 Ø Ø Ø	1
New Contents	AC	1 Ø 1 Ø 1 1 Ø Ø	Ø

Flags Z, H and N will be RESET = Ø, Flags S and P/V will be SET = 1 and the C Flag will contain the Ø previously held in Bit Ø of the memory location.

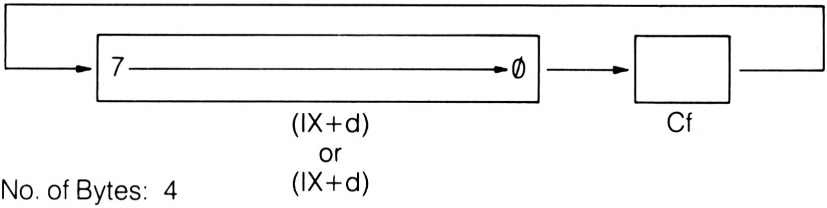
Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

RR (IX + d)
RR (IY + d)

Description: Rotates Right the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction) through the C (Carry) Flag in the Flag Register. Each Bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit Ø are moved into the C Flag and the previous contents of the C Flag are moved into Bit 7.



No. of Bytes: 4

Object Code:

	Hex	Decimal
RR (IX + d) RR (IY + d)	DD CB d 1E FD CB d 1E	221 2Ø3 d Ø3Ø 253 2Ø3 d Ø3Ø

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the memory location

Cont.

```
Example:  SCF
          CCF
          LD IX,5643H
          LD A,89H
          LD (5649H),A
          RR (IX+6)
```

If the contents of Index Register IX are 56 43, and d in the instruction is Ø6(Hex.), the required memory location is 56 49. If the contents of that memory location are 89 and the C Flag = Ø, the effect of this instruction will be:

	Memory Location									C
		Bits								
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	89	1	Ø	Ø	Ø	1	Ø	Ø	1	Ø
New Contents	44	Ø	1	Ø	Ø	Ø	1	Ø	Ø	1

Flags S, Z, H and N are RESET = Ø, Flag P/V is SET = 1 and the C Flag contains the 1 previously held in Bit Ø of the memory location.

Addressing Mode: Indexed.

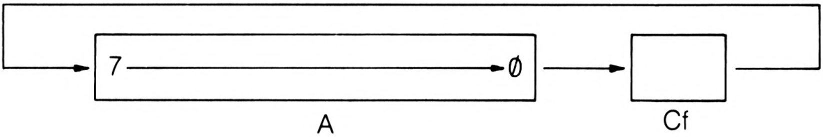
Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

RRA

Description: Rotates Right the contents of the Accumulator through the C (Carry) Flag. Each Bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit Ø are moved into the C Flag and the previous contents of the C Flag are moved into Bit 7.

NOTE: This instruction is provided for compatibility with the Intel 8Ø8Ø. It is similar to instruction RR A, except that the effect on the Flag Register is different and it is faster in execution.



No. of Bytes: 1

Object Code (Hex.): 1F Decimal: Ø31

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the Accumulator.

Cont.

Example: LD A,57H
SCF
RRA

If the contents of the Accumulator are 57, and the C Flag = 1, the effect of this instruction will be:

	Accumulator									
		Bits								C
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	57	Ø	1	Ø	1	Ø	1	1	1	1
New Contents	AB	1	Ø	1	Ø	1	Ø	1	1	1

Flags H and N will be RESET = Ø and Flag C will contain the 1 previously held in Bit Ø of the Accumulator.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

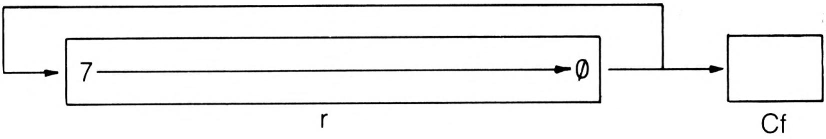
RRC r

Rotate contents of Register r circular where r is any of the registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
RRC A	CB ØF	2Ø3 Ø15
RRC B	CB ØB	2Ø3 ØØ8
RRC C	CB Ø9	2Ø3 ØØ9
RRC D	CB ØA	2Ø3 Ø1Ø
RRC E	CB ØB	2Ø3 Ø11
RRC H	CB ØC	2Ø3 Ø12
RRC L	CB ØD	2Ø3 Ø13

Description: Rotates Right the contents of Register r. Each Bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit Ø are moved into Bit 7 *and* into the C (Carry) Flag in the Flag Register.



No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the Accumulator.

Cont.

Example: LD A,ØB6H
RRC A

If the contents of the Accumulator are B6(Hex.), the effect of this instruction will be:

	Accumulator		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	B6	1 Ø 1 1 Ø 1 1 Ø	?
New Contents	5B	Ø 1 Ø 1 1 Ø 1 1	Ø

Flags S, Z, H, P/V and S are RESET = Ø and Flag C will contain the Ø previously held in Bit Ø of the Accumulator, which is identical to that now held in Bit 7 of the Accumulator.

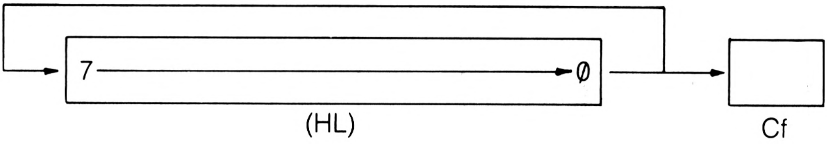
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

RRC (HL)

Description: Rotates Right the contents of the memory location whose address is held in Register Pair HL. Each Bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit Ø are moved into Bit 7 *and* into the C (Carry) Flag in the Flag Register.



No. of Bytes: 2

Object Code (Hex.): CB ØE   Decimal: 2Ø3 Ø14

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the memory location.

Cont.

Example: LD HL,1745H
LD (HL),5A
RRC (HL)

If the contents of Register Pair HL are 17 45, and the contents of memory location 17 45 are 5A, the effect of this instruction will be:

	Memory Location									C
		Bits								
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	5A	Ø	1	Ø	1	1	Ø	1	Ø	?
New Contents	2C	Ø	Ø	1	Ø	1	1	Ø	Ø	Ø

Flags S, Z, H, P/V and N are RESET = Ø and Flag C contains the data previously held in Bit Ø of the memory location, which is identical to that now held in Bit 7 of the memory location.

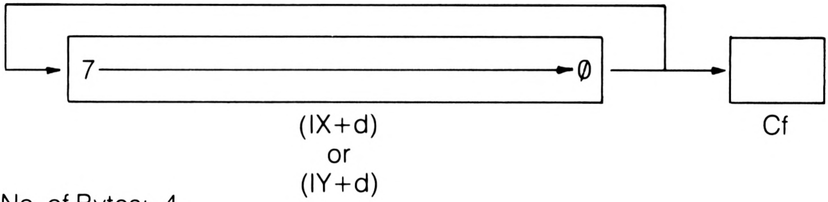
Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

RRC (IX + d)
RRC (IY + d)

Description: Rotates Right the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction). Each bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit Ø are moved into Bit 7 *and* into the C (Carry) Flag in the Flag Register.



No. of Bytes: 4

Object Code:

	Hex	**Decimal**
RRC (IX + d) RRC (IY + d)	DD CB d ØE FD CB d ØE	221 2Ø3 d Ø14 253 2Ø3 d Ø14

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the memory location.

Cont.

```
Example: LD IX,4521H
         LD A,27H
         LD (452BH),A
         RLC (IX+ØAH)
```

If the contents of Index Register IX are 45 21, and d in the instruction is ØA(Hex.), the required memory location is 45 2B. If the contents of memory location 45 2B are 27(Hex.) the effect of this instruction will be:

	Memory Location		C
		Bits	
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	27	Ø Ø 1 Ø Ø 1 1 1	?
New Contents	93	1 Ø Ø 1 Ø Ø 1 1	1

Flags Z, H and N are RESET = Ø, Flags S and P/V are SET = Ø and Flag C will contain the 1 previously held in Bit Ø of the memory location, which is identical to that now held in Bit 7 of the memory location.

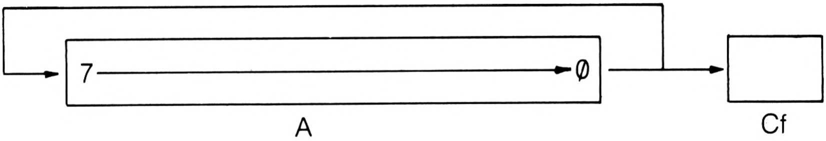
Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

RRCA

Description: Rotates Right the contents of the Accumulator. Each Bit is shifted Right one position, i.e. the contents of Bit 7 are moved into Bit 6, the contents of Bit 6 are moved into Bit 5, etc. The contents of Bit Ø are moved into Bit Ø *and* into the C (Carry) Flag in the Flag Register.



NOTE: This instruction is identical to RRC A, except for the effect on the Flag Register, but is faster in execution. It is provided for compatibility with the Intel 8Ø8Ø.

No. of Bytes: 1

Object Code (Hex.): ØF Decimal: Ø15

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the Accumulator.

Cont.

Example: LD A,37H
RRCA

If the contents of the Accumulator are 37(Hex.), the effect of this instruction will be:

	Accumulator		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	37	Ø Ø 1 1 Ø 1 1 1	?
New Contents	9B	1 Ø Ø 1 1 Ø 1 1	1

Flags H and N are RESET = Ø and Flag C contains the 1 previously held in Bit Ø of the Accumulator, which is identical to that now held in Bit 7 of the Accumulator.

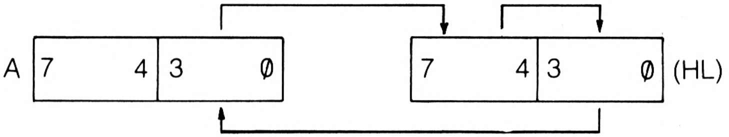
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

RRD

Description: Rotates Right Decimal the Lower Order 4 bits of the Accumulator with the Higher Order and Lower Order 4 bits of the memory location whose address is held in Register Pair HL. The Lower Order 4 bits of the Accumulator is moved into the Higher Order 4 bits of the specified memory location, the Higher Order byte of the memory location is moved into the Lower Order 4 bits of the same location and the Lower Order 4 bits of that memory location is moved into the Lower Order 4 bits of the Accumulator.



No. of Bytes: 2

Object Code (Hex.): ED 67 Decimal: 237 1Ø3

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result in the Accumulator is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result in the Accumulator is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if for Parity Even in the Accumulator result, RESET = Ø for Parity Odd in the Accumulator result.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Not affected.

Cont.

```
Example:  LD HL,1ØØØH
          LD (HL),28H
          LD A,6EH
          RRD
```

If the contents of the Accumulator are 6E(Hex.) and the contents of the nominated location are 28(Hex.) the effect of this instruction will be:

Original Contents		New Contents	
Accumulator	Location	Accumulator	Location
6 E	28	68	E 2

Flags S, Z, H, P/V and N are RESET = Ø.

Addressing Mode: Indirect

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	18	9

RST n

Description: Restart from memory location ØØ n. Pushes the contents of the Program Counter on to the top of the memory Stack by first decrementing the Stack Pointer (SP) and loading the Higher Order byte of the Program Counter (PC) into the memory location whose address is now held in the Stack Pointer, then decrementing the Stack Pointer again and loading the Lower Order byte of the Program Counter into the memory location whose address is the new contents of the Stack Pointer. Finally, the value ØØ n is loaded into the Program Counter and the next instruction is fetched from that address.

NOTE: The RST instructions transfer control to specific addresses in low memory. It can be used for a fast response to an interrupt

No. of Bytes: 1

Object Code:

	Hex	Decimal
RST ØØ	C7	199
RST Ø8	CF	2Ø7
RST 1Ø	D7	215
RST 18	DF	223
RST 2Ø	E7	231
RST 28	EF	239
RST 3Ø	F7	247
RST 38	FF	255

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

Example: RST ØØ — If the contents of the Program Counter are 64 B1, and the contents of the Stack Pointer are 32 75, the effect of this instruction will be:

	Program Counter			Location	
	Higher Byte	Lower Byte	Stack Pointer	Address	Contents
Original Contents	64	B1	32 75	32 75	?
New Contents	ØØ	ØØ	32 73	32 75	?(Not Changed)
				32 74	64
				32 73	B1

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2MHz
3	11	5.5

SBC A,n

Description: Subtracts from the Accumulator the integer n, summed with the contents of the Carry Flag in the Flag Register. The result is stored in the Accumulator.

No. of Bytes: 2

Object Code (Hex.): DE n Decimal: 222 n

Where n is an 8 Bit integer, specified in the instruction.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø.
Subtract	N	1	SET = 1.
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

```
Example: LD A,45H
         SCF
         SBC A,4
```

If the contents of the Accumulator are 45(Hex.), the C(Carry) Flag = 1 and n in the instruction is 4, this instruction will subract 4 + 1 (=5) from the contents of the Accumulator and store 4Ø(Hex.), the result, in the Accumulator. Flags S, Z and P/V are RESET = Ø and Flags N and C are SET = 1.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

SBC A,A

Description: Subtracts from the Accumulator the contents of the Accumulator, summed with the contents of the C (Carry) Flag in the Flag register. The result is stored in the Accumulator. Note that the result in the Accumulator will always be ∅H or FFH (negative one in twos complement notation), depending on the contents of the carry flag.

No. of Bytes: 1

Object Code (Hex.): 9F Decimal: 159

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = ∅.
Subtract	N	1	SET = 1.
Carry	C	∅	SET = 1 if no Borrow, otherwise RESET = ∅.

```
Example: LD A,28H
         SCF
         CCF
         SBC A,A
```

If the contents of the Accumulator are 28(Hex.) and the C Flag = ∅, this instruction will subtract 28 + ∅(=28) from the Accumulator and store the result (∅) in the Accumulator. Flags S and P/V are RESET = ∅ and Flags Z, H, N and C are SET = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

SBC A,r

Subtract Register r with carry from the Accumulator where r is any of the registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
SBC A,B	98	152
SBC A,C	99	153
SBC A,D	9A	154
SBC A,E	9B	155
SBC A,H	9C	156
SBC A,L	9D	157

Description: Subtracts from the Accumulator the contents of Register r and the contents of the C (Carry) Flag in the Flag Register, then stores the result in the Accumulator.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø.
Subtract	N	1	SET = 1.
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Cont.

```
Example:  LD A,ØA9H
          LD B,16H
          SCF
          SBC A,B
```

If the contents of the Accumulator are A9(Hex.), the contents of Register B are 16(Hex.) and the C Flag = 1, the effect of this instruction will be:

	Accumulator	Register B	C Flag
Original Contents	A9	16	1
Subtract	16		
(Register B)	——		
	93		
Subtract	1		
(C Flag)	——		
New Contents	92	16	1
	——		

Flags Z and P/V are RESET = Ø while Flags S, H, N and C are SET = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

SBC A,(HL)

Description: Subtracts from the Accumulator the contents of the memory location whose address is held in Register Pair HL and the contents of the C (Carry) Flag in the Flag Register, then stores the result in the Accumulator.

No. of Bytes: 1

Object Code (Hex.): 9E Decimal: 158

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø.
Subtract	N	1	SET = 1.
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Cont.

Example:

```
LD HL,ØAF34H
LD (HL),24H
LD A,25H
SCF
SBC A,(HL)
```

If the contents of Register Pair HL are AF 34, the required location is AF 34. If the contents of the Accumulator are 25(Hex.), the contents of memory location AF 34 are 24(Hex.) and the C Flag = 1, the effect of this instruction will be:

	Accumulator	Memory Location	C Flag
Original Contents	25	24	1
Subtract			
(Memory Location)	24		
Subtract	Ø1		
(C Flag)	1		
New Contents	ØØ	24	1

Flags S and P/V are RESET = Ø while Flags Z, H, N and C are SET = 1.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

SBC A,(IX + d)
SBC A,(IY + d)

Description: Subtracts from the Accumulator the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction) and the contents of the C (Carry) Flag in the Flag Register, then stores the result in the Accumulator.

No. of Bytes: 3

Object Code:

	Hex	Decimal
SBC A,(IX + d)	DD 9E d	221 158 d
SBC A,(IY + d)	FD 9E d	253 158 d

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = ∅
Subtract	N	1	SET = 1.
Carry	C	∅	SET = 1 if no Borrow, otherwise RESET = ∅.

Cont.

Example:

```
SCF
CCF
LD HL,ØA244H
LD (HL),12H
LD IX,ØA234H
LD A,28H
SBC A,(IX+1ØH)
```

If the contents of Index Register IX are A2 34, and d in the instruction is 16(1Ø Hex.), the required memory location is A2 44. If the contents of the Accumulator are 28(Hex.), the contents of memory location A2 44 are 12(Hex.) and the C Flag = Ø, the result of this instruction will be:

	Accumulator	Memory Location A2 44	C Flag
Original Contents Subtract (Index Register IX) Subtract (C Flag)	28 12 — 16 Ø	12	Ø
New Contents	16	12	Ø

Flags S, Z and P/V are RESET = Ø, while Flags H, N and C are SET = 1.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

SBC HL,rr

Where rr is any of the Register Pairs BC, DE, HL, SP.

Description: Subtracts from the contents of Register Pair HL the contents of the specified register pair and the contents of the C (Carry) Flag in the Flag Register, then stores the result in Register Pair HL.

No. of Bytes: 2

Object Code:

	Hex	Decimal
SBC HL,BC	ED 42	237 Ø66
SBC HL,DE	ED 52	237 Ø82
SBC HL,HL	ED 62	237 Ø98
SBC HL,SP	ED 72	237 114

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 12, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø
Subtract	N	1	SET = 1.
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Cont.

Example:

```
LD HL,2816H
LD BC,2715H
SCF
SBC HL,BC
```

If the contents of Register Pair HL are 28 16(Hex.), the contents of Register Pair BC are 27 15(Hex.) and the C Flag = 1, the effect of this instruction will be:

	Register Pair HL	Register Pair BC	C Flag
Original Contents	28 16	27 15	1
Subtract	27 15		
(Register Pair HL)	——		
	Ø1 Ø1		
Subtract	1		
(C Flag)			
New Contents	Ø1 ØØ	27 15	1

Flags S, Z and P/V are RESET = Ø while Flags H, N and C are SET = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

SCF

Description: SETS the C (Carry) Flag in the Flag Register = 1.

No. of Bytes: 1

Object Code (Hex.): 37 Decimal: Ø55

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	SET = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

SET b,r

Description: The specified Bit in the nominated Register is SET = 1.

No. of Bytes: 2

Object Code (Hex.): CB xx Decimal: 2Ø3 yyy

Where: b is the Bit (Range Ø — 7) to be SET = 1 and r is the Register (A, B, C, D, E, H or L) which contains that bit.
xx or yyy are taken from the table below:

	A		B		C		D		E		H		L	
Bit	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy	xx	yyy
Ø	C7	199	CØ	192	C1	193	C2	194	C3	195	C4	196	C5	197
1	CF	2Ø7	C8	2ØØ	C9	2Ø1	CA	2Ø2	CB	2Ø3	CC	2Ø4	CD	2Ø5
2	D7	215	DØ	2Ø8	D1	2Ø9	D2	21Ø	D3	211	D4	212	D5	213
3	DF	223	D8	216	D9	217	DA	218	DB	219	DC	22Ø	DD	221
4	E7	231	EØ	224	E1	225	E2	226	E3	227	E4	228	E5	229
5	EF	239	E8	232	E9	233	EA	234	EB	235	EC	236	ED	237
6	F7	247	FØ	24Ø	F1	241	F2	242	F3	243	F4	244	F5	245
7	FF	255	F8	248	F9	249	FA	25Ø	FB	251	FC	252	FD	253

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example: LD E,Ø
SET 2,E

The Source Code statement SET 2,E, will result in the Object Code (Hex.) instruction CB D3 which will SET = 1 Bit 2 in Register E.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

SET b,(HL)

Description: The nominated Bit in the memory location whose address is held in Register Pair HL is SET = 1.

No. of Bytes: 2

Object Code (Hex.): CB xx Decimal: 2Ø3 yyy

Where: xx or yyy are taken from the table below:

Bit	xx	yyy
Ø	C6	198
1	CE	2Ø6
2	D6	214
3	DE	222
4	E6	23Ø
5	EE	238
6	F6	246
7	FE	254

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Example:
```
LD HL,1ØØØH
LD (HL),Ø
SET 5,(HL)
```

The Source Code statement SET 5,(HL) will produce the Object Code (Hex.) instruction CD EE, which will SET = 1 Bit 5 in the memory location whose address is held in Register Pair HL.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	µsec @ 2 MHz.
4	15	7.5

SET b,(IX + d)
SET b,(IY + d)

Description: SETs = 1 the nominated Bit in the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction).

No. of Bytes: 4

Object Code:

	Hex	**Decimal**

SET b,(IX + d)
SET b,(IY + d)
	DD CB d xx
	FD CB d xx
		221 2Ø3 d yyy
		253 2Ø3 d yyy

Where: b is the Bit (Range Ø — 7) to be SET = 1, and D is the required displacement from the memory location whose address is held in Index Register IX.
xx or yyy are taken from the table below:

Bit	xx	yyy
Ø	C6	198
1	CE	2Ø6
2	D6	214
3	DE	222
4	E6	23Ø
5	EE	238
6	F6	246
7	FE	254

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	Not affected.
Zero	Z	6	Not affected.
—	—	5	Not used.
Half Carry	H	4	Not affected.
—	—	3	Not used.
Parity/Overflow	P/V	2	Not affected.
Subtract	N	1	Not affected.
Carry	C	Ø	Not affected.

Cont.

```
Example: LD HL,348EH
         LD (HL),Ø
         LD IX,348AH
         SET 2,(IX+4)
```

The Source Code statement SET 2,(IX + 4) will produce the Object Code (Hex.) instruction DD CB 4 D6. If the contents of Index Register IX are 34 8A, the required memory location is 34 8E (i.e. 34 8A + 4). This instruction will SET = 1 Bit 2 in memory location 34 8E.

Addressing Mode: Indexed.

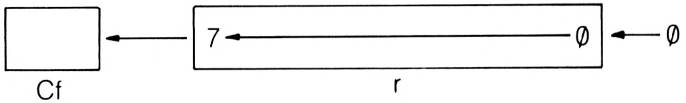
Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

SLA r

Where r is any of the registers A, B, C, D, E, H, L.

Description: Shifts Left the contents of the specified register, through the C (Carry) Flag in the Flag Register. Bit 0 is RESET = 0, the previous contents of Bit 0 are moved into Bit 1, the previous contents of Bit 1 are moved to Bit 2, etc. The previous contents of Bit 7 are moved into the C (Carry) Flag in the Flag Register. The previous contents of the Carry Flag are destroyed.



No. of Bytes: 2

Object Code:

	Hex	Decimal
SLA A	CB 27	2∅3 39
SLA B	CB 2∅	2∅3 32
SLA C	CB 21	2∅3 33
SLA D	DB 22	2∅3 34
SLA E	CB 23	2∅3 35
SLA H	CB 24	2∅3 36
SLA L	CB 25	2∅3 37

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Contains the data previously held in Bit 7 of the Accumulator.

Cont.

Example: LD A,93H
SLA H

If the contents of the Accumulator are 93(Hex.), the effect of this instruction will be:

	Accumulator		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	93	1 Ø Ø 1 Ø Ø 1 1	?
New Contents	26	Ø Ø 1 Ø Ø 1 1 Ø	1

Flags S, Z, H, P/V and N are RESET = Ø while Flag C contains the 1 previously held in Bit 7 of the Accumulator.

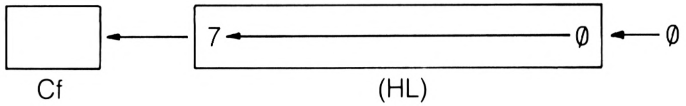
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

SLA (HL)

Description: Shifts Left the contents of the memory location whose address is held in Register Pair HL, through the C (Carry) Flag in the Flag Register. Bit Ø is RESET = Ø, the previous contents of Bit Ø are moved into Bit 1, the previous contents of Bit 1 are moved into Bit 2, etc. The previous contents of Bit 7 are moved into the C Flag in the Flag Register. The previous contents of the carry flag are destroyed.



No. of Bytes: 2

Object Code (Hex.): CB 26 Decimal: 2Ø3 Ø38

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit 7 of the memory location.

Cont.

Example:

```
LD HL,ØCD45H
LD (HL),23H
SLA (HL)
```

If the contents of Register Pair HL are CD 45, and the contents of memory location CD 45 are 23(Hex.), the effect of this instruction will be:

	Memory Location CD 45		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	23	Ø Ø 1 Ø Ø Ø 1 1	?
New Contents	46	Ø 1 Ø Ø Ø 1 1 Ø	Ø

Flags S, Z, H, P/V and N are RESET = Ø, while Flag C contains the Ø previously held in Bit 7 of memory location CD 45.

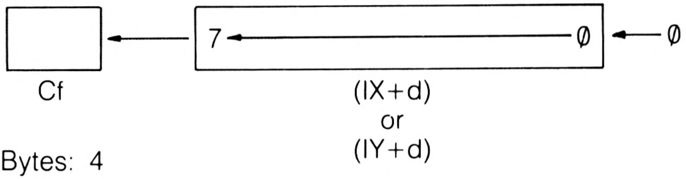
Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

SLA (IX + d)
SLA (IY + d)

Description: Shifts Left the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), through the C (Carry) Flag in the Flag Register. Bit Ø is RESET = Ø, the previous contents of Bit Ø are moved into Bit 1, the previous contents of Bit 1 are moved into Bit 2, etc. The previous contents of Bit 7 are moved into the C Flag in the Flag Register. The previous contents of the carry flag are destroyed.



No. of Bytes: 4

Object Code:

	Hex	**Decimal**
SLA (IX + d) SLA (IY + d)	DD CB d 26 FD CB d 26	221 203 d 38 253 203 d 38

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit 7 of the memory location.

Cont.

```
Example:  LD HL,283AH
          LD (HL),16H
          LD IX,2834
          SLA (IX+6)
```

If the contents of Index Register IX are 28 34 and d in the instruction is 6, the required location is 28 3A. If the contents of memory location 28 3A are 16(Hex.), the effect of this instruction will be:

	Memory Location 28 3A		C
		Bits	
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	16	Ø Ø Ø 1 Ø 1 1 Ø	?
New Contents	2C	Ø Ø 1 Ø 1 1 Ø Ø	Ø

Flags S, Z, H, P/V and N are RESET = Ø, while Flag C contains the Ø previously held in Bit 7 of memory location 28 3A.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

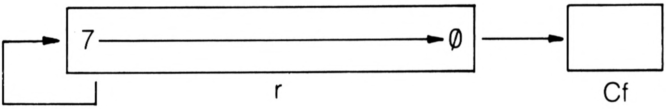
SRA r

Arithmetic shift contents of Register r right, where r is any of the Registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
SRA A	CB 2F	2Ø3 Ø47
SRA B	CB 28	2Ø3 Ø4Ø
SRA C	CB 29	2Ø3 Ø41
SRA D	CB 2A	2Ø3 Ø42
SRA E	CB 2B	2Ø3 Ø43
SRA H	CB 2C	2Ø3 Ø44
SRA L	CB 2D	2Ø3 Ø45

Description: Shift Register r right one bit. Bit 7 is unchanged. Bit Ø is moved into the carry flag. Bit 7 is moved into bit 6, but is not itself changed. Bit 6 is moved into bit 5. Bit 5 is moved into bit 4, etc.



No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the Accumulator.

Cont.

Example: LD A,93H
SRA A

If the contents of the Accumulator are 93(Hex.), the effect of this instruction will be:

	Accumulator		C
		Bits	
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	93	1 Ø Ø 1 Ø Ø 1 1	?
New Contents	C9	1 1 Ø Ø 1 Ø Ø 1	1

Flags Z, H and N are RESET = Ø, Flags S and P/V are SET = 1 while Flag C contains the 1 previously held in Bit Ø of the Accumulator.

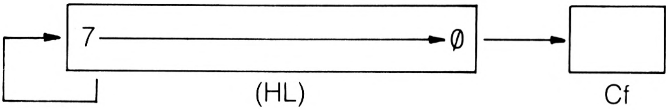
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

SRA (HL)

Description: Shifts Right the contents of the memory location whose address is held in Register Pair HL, through the C (Carry) Flag in the Flag Register. The contents of Bit 7 remain unchanged but are copied into Bit 6, the previous contents of Bit 6 are moved into Bit 5, the previous contents of Bit 5 are moved into Bit 4, etc. The previous contents of Bit Ø are moved into the C (Carry) Flag in the Flag Register.



No. of Bytes: 2

Object Code (Hex.): CB 2E   Decimal: 2Ø3 Ø46

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the memory location.

Cont.

```
Example: LD HL,ØCD45H
         LD (HL),23H
         SRA (HL)
```

If the contents of Register Pair HL are CD 45, and the contents of memory location CD 45 are 23(Hex.), the effect of this instruction will be:

	Memory Location CD 45		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	23	Ø Ø 1 Ø Ø Ø 1 1	?
New Contents	11	Ø Ø Ø 1 Ø Ø Ø 1	1

Flags S, Z, H and N are RESET = Ø, Flag P/V is SET = 1 while Flag C contains the 1 previously held in Bit Ø of memory location CD 45.

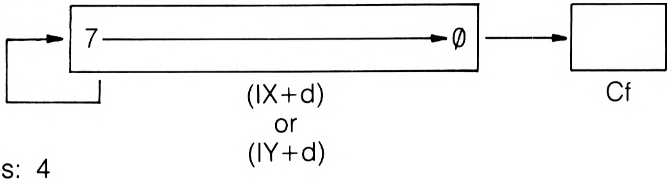
Addressing Mode: Indirect

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

SRA (IX + d)
SRA (IY + d)

Description: Shifts Right the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), using the C (Carry) Flag in the Flag Register. The contents of Bit 7 remain unchanged but are copied into Bit 6, the previous contents of Bit 6 are moved into Bit 5, the previous contents of Bit 5 are moved into Bit 4, etc. The previous contents of Bit Ø are moved into the C (Carry) Flag in the Flag Register.



No. of Bytes: 4

Object Code:

	Hex	Decimal
SRA (IX + d) SRA (IY + d)	DD CB d 2E FD CB d 2E	221 2Ø3 d Ø46 253 2Ø3 d Ø46

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the memory location.

Cont.

Example: LD HL,283AH
LD (HL),16H
LD IX,2834H
SRA (IX+6)

If the contents of Index Register IX are 28 34 and D in the instruction is 6, the required location is 28 3A. If the contents of memory location 28 3A are 16(Hex.), the effect of this instruction will be:

	Memory Location 28 3A		
		Bits	C
	Hex.	7 6 5 4 3 2 1 Ø	Flag
Original Contents	16	Ø Ø Ø 1 Ø 1 1 Ø	?
New Contents	ØB	Ø Ø Ø Ø 1 Ø 1 1	Ø

Flags S, Z, H, P/V and N are RESET = Ø, while Flag C contains the Ø previously held in Bit Ø of memory location 28 3A.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	usec @ 2 MHz.
6	23	11.5

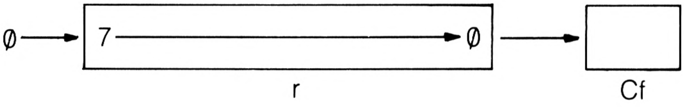
SRL r

Shift contents of Register r right logical, where r is any of the Registers A, B, C, D, E, H or L.

Object Code:

	Hex	Decimal
SRL A	CB 3F	2Ø3 Ø63
SRL B	CB 38	2Ø3 Ø56
SRL C	CB 39	2Ø3 Ø57
SRL D	CB 3A	2Ø3 Ø58
SRL E	CB 3B	2Ø3 Ø59
SRL H	CB 3C	2Ø3 Ø6Ø
SRL L	CB 3D	2Ø3 Ø61

Description: Shift contents of Register r right one bit. Bit 7 is RESET = Ø. Bit Ø is moved to the carry flag.



No. of Bytes: 2

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the Accumulator.

Cont.

Example: LD A,93H
SRL A

If the contents of the Accumulator are 93(Hex.), the effect of this instruction will be:

	Accumulator									C
		Bits								
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	93	1	Ø	Ø	1	Ø	Ø	1	1	?
New Contents	49	Ø	1	Ø	Ø	1	Ø	Ø	1	1

Flags S, Z, H, P/V and N are RESET = Ø, while Flag C contains the 1 previously held in Bit Ø of the Accumulator.

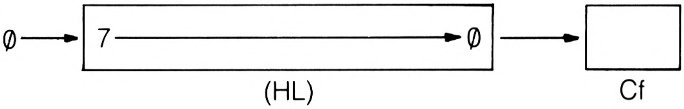
Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	8	4

SRL (HL)

Description: Logical Shift Right of the contents of the memory location whose address is held in Register Pair IX. Bit 7 is RESET = ∅, the previous contents of Bit 7 are moved into Bit 6, the previous contents of Bit 6 are moved into Bit 5, etc. The previous contents of Bit ∅ are moved into the C (Carry) Flag in the Flag Register.



No. of Bytes: 2

Object Code (Hex.): CB 3E Decimal: 2∅3 ∅62

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	Contains the data previously held in Bit ∅ of the memory location.

Cont.

Example: LD HL,ØCD45H
LD (HL),23H
SRL (HL)

If the contents of Register Pair HL are CD 45, and the contents of memory location CD 45 are 23(Hex.), the effect of this instruction will be:

	Memory Location CD 45									C
		Bits								
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	23	Ø	Ø	1	Ø	Ø	Ø	1	1	?
New Contents	11	Ø	Ø	Ø	1	Ø	Ø	Ø	1	1

Flags S, Z, H and N are RESET = Ø, Flag P/V is SET = 1, while Flag C contains the 1 previously held in Bit Ø of memory location CD 45.

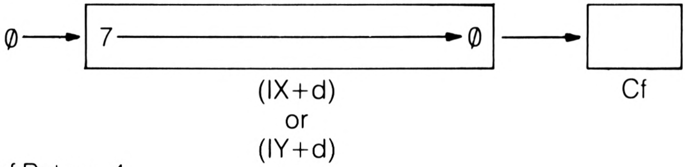
Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
4	15	7.5

SRL (IX + d)
SRL (IY + d)

Description: Logical Shift Right of the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction. Bit 7 is RESET = Ø, the previous contents of Bit 7 are moved into Bit 6, the previous contents of Bit 6 are moved into Bit 5, etc. The previous contents of Bit Ø are moved into the C (Carry) Flag in the Flag Register.



No. of Bytes: 4

Object Code:

	Hex	Decimal
SRL (IX + d) SRL (IY + d)	DD CB d 3E FD CB d 3E	221 2Ø3 d Ø62 253 2Ø3 d Ø62

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	Contains the data previously held in Bit Ø of the memory location.

Cont.

```
Example:  LD HL,283AH
          LD (HL),16H
          LD IX,2834H
          SRL (IX+6)
```

If the contents of Index Register IX are 28 34 and d in the instruction is 6, the required location is 28 3A. If the contents of memory location 28 3A are 16(Hex.), the effect of this instruction will be:

	Memory Location 28 3A									
		Bits								C
	Hex.	7	6	5	4	3	2	1	Ø	Flag
Original Contents	16	Ø	Ø	Ø	1	Ø	1	1	Ø	?
New Contents	ØB	Ø	Ø	Ø	Ø	1	Ø	1	1	Ø

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
6	23	11.5

SUB n

Description: Subtracts the integer n from the contents of the Accumulator and stores the result in the Accumulator.

No. of Bytes: 2

Object Code (Hex.): D6 n   Decimal: 214 n

Where n is an 8 Bit integer, specified in the instruction.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = ∅
Subtract	N	1	SET = 1.
Carry	C	∅	SET = 1 if no Borrow, otherwise RESET = ∅.

Example: LD A,45H
SUB 4

If the contents of the Accumulator are 45(Hex.) and n in the instruction is 4, the effect of this instruction will be:

	Accumulator (Hex.)
Original Contents Subtract n	45 4
New Contents	41

Flags S, Z and P/V are RESET = ∅ while Flags H, N and C are SET = 1.

Addressing Mode: Immediate.

Cont.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

SUB A

Description: Subtracts the contents of the Accumulator from the contents of the Accumulator and stores the result in the Accumulator. Note that this will always leave a result of zero in the Accumulator.

No. of Bytes: 1

Object Code (Hex.): 97 Decimal: 151

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = ∅
Subtract	N	1	SET = 1.
Carry	C	∅	SET = 1 if no Borrow, otherwise RESET = ∅.

Example: LD A,28
SUB A

If the contents of the Accumulator are 28(Hex.), the effect of this instruction will be:

	Accumulator (Hex.)
Original Contents Subtract	28 28
New Contents	∅∅

Flags S and P/V are RESET = ∅ while Flags Z, H, C and N are SET = 1.

Addressing Mode: Implicit

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

SUB r

Subtract Register r from the Accumulator, where r is any of the Registers B, C, D, E, H or L.

Object Code:

	Hex	Decimal
SUB B	9Ø	144
SUB C	91	145
SUB D	92	146
SUB E	93	147
SUB H	94	148
SUB L	95	149

Description: Subtract the contents of Register r from the contents of the Accumulator, contents of Register r unchanged.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø.
Subtract	N	1	SET = 1.
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Cont.

```
Example:  LD A,ØA9H
          LD B,16H
          SUB B
```

If the contents of the Accumulator are A9(Hex.), and the contents of Register B are 16(Hex.), the effect of this instruction will be:

	Accumulator	Register B
Original Contents Subtract (Register B)	A9 16	16
New Contents	93	16

Flags S, Z, and P/V are RESET = Ø, while Flags H, N and C are SET = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

SUB (HL)

Description: Subtracts from the Accumulator the contents of the memory location whose address is held in Register Pair HL, then stores the result in the Accumulator. The contents of the memory location remain unchanged.

No. of Bytes: 1

Object Code (Hex.): 96 Decimal: 15Ø

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = Ø
Subtract	N	1	SET = 1.
Carry	C	Ø	SET = 1 if no Borrow, otherwise RESET = Ø.

Cont.

```
Example: LD HL,ØAF34H
         LD (HL),24H
         LD A,25H
         SUB (HL)
```

If the contents of Register Pair HL are AF 34, the required memory locatin is AF 34. If the contents of the Accumulator are 25(Hex.), and the contents of memory location AF 34 are 24(Hex.), the effect of this instruction will be:

	Accumulator	Memory Location AF 34
Original Contents	25	24
Subtract (Memory Location)	24	
New Contents	Ø1	24

Flags S, Z and P/V are RESET = Ø, while Flags H, N and C are SET = 1.

Addressing Mode: Indirect.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

SUB (IX + d)
SUB (IY + d)

Description: Subtracts from the Accumulator the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), then stores the result in the Accumulator. The contents of the memory location remain unchanged.

No. of Bytes: 3

Object Code:

	Hex	**Decimal**
SUB (IX + d) SUB (IY + d)	DD 96 d FD 96 d	221 15∅ d 253 15∅ d

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	SET = 1 if no Borrow from Bit 4, otherwise RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 if Overflow, otherwise RESET = ∅
Subtract	N	1	SET = 1.
Carry	C	∅	SET = 1 if no Borrow, otherwise RESET = ∅.

Cont.

```
Example: LD HL,ØA244H
         LD (HL),12H
         LD IX,ØA234H
         LD A,28H
         SUB (IX+1ØH)
```

If the contents of Index Register IX are A2 34, and d in the Source Code is 16(1ØHex.), the required memory location is A2 44. If the contents of the Accumulator are 28(Hex.), and the contents of memory location A2 44are 12(Hex.), the effect of this instruction will be:

	Accumulator	Memory Location A2 44
Original Contents	28	12
Subtract (Memory Location A2 44)	12	
New Contents	16	12

Flags S, Z and P/V are RESET = Ø, while Flags H, N and C are SET = 1.

Addressing Mode: Indexed.

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

XOR n

Description: Performs a Bit by Bit logical Exclusive OR between the contents of the Accumulator and integer n, then stores the result in the Accumulator. For any corresponding bit positions, if the two contents are equal, i.e. both = 1 or both = Ø, the result, for that bit position, will be Ø, but if the two contents are not equal, i.e. one = Ø and the other = 1, the result for that bit position will be 1.

NOTE: The XOR instruction can be used to complement the Accumulator by specifying n as 255, i.e. FF(Hex.).

No. of Bytes: 2

Object Code (Hex.): EE n Decimal: 238 n

Where n is an 8 Bit integer, specified in the instruction.

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	RESET = Ø

Cont.

Example: LD A,67H
XOR 5EH

If the contents of the Accumulator are 67(Hex.), and n is specified in the Source Code as 94 (5E Hex.), the effect of this instruction will be:

		Bits							
	Hex.	7	6	5	4	3	2	1	Ø
Accumulator	67	Ø	1	1	Ø	Ø	1	1	1
Value of n	5E	Ø	1	Ø	1	1	1	1	Ø
Result	39	Ø	Ø	1	1	1	Ø	Ø	1

Flags S, H, Z, N and C are RESET = Ø, while the P/V flag is SET = 1.

Addressing Mode: Immediate.

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

XOR A

Description: Performs a Bit by Bit logical Exclusive OR between the contents of the Accumulator and the contents of the Accumulator. For any corresponding bit positions, if the two contents are equal, i.e. both = 1 or both = Ø, the result, for that bit position, will be Ø, but if the two contents are not equal, the result for that bit position will be 1.

NOTE: The effect of this instruction will be to make the contents of the Accumulator equal ØØ(Hex.).

No. of Bytes: 1

Object Code (Hex.): AF   Decimal: 175

Flag Register:

Flag	**Code**	**Bit**	**Effect**
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	RESET = Ø

Cont.

Example: LD A,F4H
XOR A

If the contents of the Accumulator are F4(Hex.), the effect of this instruction will be:

		Bits							
	Hex.	7	6	5	4	3	2	1	Ø
Accumulator	F4	1	1	1	1	Ø	1	Ø	Ø
Accumulator	F4	1	1	1	1	Ø	1	Ø	Ø
Result	ØØ	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø

Flags S, N and C are RESET = Ø, while Flags Z, H and P/V are SET = 1.

Addressing Mode: Implicit

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

XOR r

Exclusive OR Register r with the Accumulator where r is any of the registers B, C, D, E, H or L.

Object Code:

	Hex	Decimal
XOR B	A8	168
XOR C	A9	169
XOR D	AA	17∅
XOR E	AB	171
XOR H	AC	172
XOR L	AD	173

Description: Exclusive OR Accumulator with the specified Register r. Contents of Register r unchanged.

No. of Bytes: 1

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	RESET = ∅.

Cont.

Example: LD A,ØC4H
LD B,ØA7H
XOR B

If the contents of the Accumulator are C4(Hex.), and the contents of Register B are A7(Hex.), the effect of this instruction will be:

		Bits							
	Hex.	7	6	5	4	3	2	1	Ø
Accumulator	C4	1	1	Ø	Ø	Ø	1	Ø	Ø
Register B	A7	1	Ø	1	Ø	Ø	1	1	1
Result	63	Ø	1	1	Ø	Ø	Ø	1	1

Flags S, H, Z, N and C are RESET = Ø, while the P/V flag is SET = 1.

Addressing Mode: Implicit.

Timing:

M Cycles	T States	μsec @ 2 MHz.
1	4	2

XOR (HL)

Description: Performs a Bit by Bit logical Exclusive OR between the contents of the Accumulator and the contents of the memory location whose address is held in Register Pair HL, then stores the result in the Accumulator. For any two corresponding bit positions, if the contents are equal, i.e. both = 1 or both = ∅, the result, for that bit position, will be ∅, but if the two contents are not equal, the result will be 1.

No. of Bytes: 1

Object Code (Hex.): AE Decimal: 174

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = ∅.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = ∅.
—	—	5	Not used.
Half Carry	H	4	RESET = ∅.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = ∅ for Parity Odd.
Subtract	N	1	RESET = ∅.
Carry	C	∅	RESET = ∅

Cont.

```
Example: LD HL,ØAD45H
         LD (HL),ØB6H
         LD A,9DH
         XOR (HL)
```

If the contents of Register Pair HL are AD 45, the contents of memory location AD 45 are B6, and the contents of the Accumulator are 9D(Hex.), the effect of this instruction will be:

		Bits							
	Hex.	7	6	5	4	3	2	1	Ø
Accumulator	9D	1	Ø	Ø	1	1	1	Ø	1
Memory Location AD 45	B6	1	Ø	1	1	Ø	1	1	Ø
Result	2B	Ø	Ø	1	Ø	1	Ø	1	1

Flags S, H, Z, N and C are RESET = Ø, while the P/V flag is SET = 1.

Addressing Mode: Indirect

Timing:

M Cycles	T States	μsec @ 2 MHz.
2	7	3.5

XOR (IX + d)
XOR (IY + d)

Description: Performs a Bit by Bit logical Exclusive OR between the contents of the Accumulator and the contents of the memory location whose address is identified by the contents of Index Register IX or IY (modified by displacement d, which is specified in the instruction), then stores the result in the Accumulator. For any two corresponding bit positions, if the contents are equal, i.e. both = 1 or both = Ø, the result, for that bit position, will be Ø, but if the two contents are not equal, the result for that bit position will be 1.

No. of Bytes: 3

Object Code:

	Hex	Decimal
XOR (IX + d) XOR (IY + d)	DD AE d FD AE d	221 174 d 253 174 d

Where d is the required displacement from the memory location whose address is held in Index Register IX or IY.

Flag Register:

Flag	Code	Bit	Effect
Sign	S	7	SET = 1 if the result is negative, otherwise RESET = Ø.
Zero	Z	6	SET = 1 if the result is zero, otherwise RESET = Ø.
—	—	5	Not used.
Half Carry	H	4	RESET = Ø.
—	—	3	Not used.
Parity/Overflow	P/V	2	SET = 1 for Parity Even, RESET = Ø for Parity Odd.
Subtract	N	1	RESET = Ø.
Carry	C	Ø	RESET = Ø

Cont.

```
Example:  LD HL,45BDH
          LD (HL),18H
          LD IX,45ADH
          LD A,22H
          XOR (IX+1ØH)
```

If the contents of Index Register IX are 45 AD, and d in the instruction is 16 (1ØHex.), the required memory location is 45 BD. If the contents of the Accumulator are 22(Hex.) and the contents of memory location 45 BD are 18(Hex.), the effect of this instruction will be:

		Bits							
	Hex.	7	6	5	4	3	2	1	Ø
Accumulator	22	Ø	Ø	1	Ø	Ø	Ø	1	Ø
Memory Location 45 BD	18	Ø	Ø	Ø	1	1	Ø	Ø	Ø
Result	3A	Ø	Ø	1	1	1	Ø	1	Ø

Flags S, Z, H, N and C are RESET = Ø, while the P/V flag is SET = 1.

Addressing Mode: Indexed

Timing:

M Cycles	T States	μsec @ 2 MHz.
5	19	9.5

CHAPTER 6

Hints and Tips

Experienced programmers frequently develop and use methods of doing things within a program which are unlikely to occur to the newcomer, or indeed, to other skilled programmers. This chapter gives details of some of these which may prove useful to the reader.

Using a Register Pair as a Loop Counter

Decrementing a Register Pair as a loop counter requires specific code to test for a Zero condition. A simple way of achieving this, using Register Pair BC as the Loop Counter, is:

DEC BC — Decrement Register Pair BC (Loop Counter)
LD A,C — Load the contents of Register C into the Accumulator.
OR B — Perform a Logical OR between the contents of the Accumulator and the contents of Register B.
JR NZ,nn — Where nn is the address of the DEC BC instruction. This will repeat the loop until a Zero condition exists, which will only occur when the contents of both Register B and Register C are Zero.

Memory Switching

A convenient way of switching between two different areas of memory is to utilise the XOR (Exclusive OR) instruction:

XOR A — Clears the Accumulator to Zero.
XOR 96 — Makes the Accumulator = 6Ø(Hex.)
XOR 96 — Makes the Accumulator = Ø.

Incorporation in a program of a loop which XORs the Accumulator repeatedly with the same integer changes the contents of the Accumulator to that integer, then to zero, then back to the integer, etc. This can then be used to switch control between different areas of memory.

Loading a Single Byte into a Register Pair

Sometimes it is necessary to load an 8 Bit number into a Register Pair without knowing the sign of that number. For positive numbers, the Higher Order byte of the Register Pair should contain ØØ(Hex.), while for negative numbers that byte should contain FF(Hex.). An 8 Bit number in Register E can be loaded into Register Pair BC using the following Code:

LD C,E — Loads the contents of Register E into Register C, i.e. the Lower Order byte of Register Pair BC.

RL E Rotates Left Register E, placing the sign bit into the Carry Flag in the Flag Register.

SBC A,A Subtracts the contents of the Accumulator from itself, leaving a value of Ø but the sign from the Carry Flag affects the result so that, if the Carry Flag = Ø, the contents of the Accumulator become ØØ(Hex.), i.e. Ø, but if the Carry Flag = 1, the contents of the Accumulator become FF(Hex.), i.e. −Ø.

LD B,A Loads Register B with the contents of the Accumulator, i.e. ØØ(Hex.) or FF(Hex.) to match the original sign bit of Register E.

Similarly, if it is necessary to load a 16 Bit number into a 32 Bit field, the sign can be moved into the Carry Flag, then copied throughout Register Pair HL by using the instruction SBC HL,HL.

Rotating 16-Bit (Two Byte) Register Through the Carry Flag

There is no instruction to rotate a 16 Bit Register Pair Left through the Carry Flag, a facility which is sometimes necessary. This can be achieved, using the Register Pair HL, by using the instruction ADC HL,HL, which adds the contents of Register Pair HL to itself, with carry.

Converting ASCII Characters from Lower to Upper Case

The only differences between the binary representation of Upper and Lower Case ASCII characters is that the Upper Case character has Bit 5 RESET = Ø, while the equivalent Lower Case character has Bit 5 SET = 1. The instruction AND n, where n = DF(Hex.) – **11Ø11111** Binary, will RESET = Ø Bit 5 regardless of its original value, thus ensuring that the character in the Accumulator is Upper Case.

NOTE: Confusion may be caused when using this tip if the input character is non alphabetic.

Quick Division

The contents of a Register can be divided by any multiple of 2 by using the SRA r instruction (where r is the specified Register) one for each power of 2, e.g. 3 times to divide by 8. After each iteration of the SRA r instruction the remainder is placed in the Carry Flag in the Flag Register.

Quick Multiplication

A number can be multiplied by a multiple of 2 by using the appropriate SLA instruction, provided the result will not cause Overflow in the Register or Memory Location.

A number less than 256, contained in a Register Pair (say DE), can be multiplied by 256 by:

LD D,E Loads the contents of Register E (the Lower Order byte of the Register Pair, hence the number less than 256) into the Higher Order byte of the Register Pair.

LD E, +Ø Loads ØØ(Hex.) into the Lower Order byte of the Register Pair.

APPENDIX A

ASCII Codes

Binary				Binary				Binary			
MSD	LSD	Hex	Char	MSD	LSD	Hex	Char	MSD	LSD	Hex	Char
ØØØØ	ØØØØ	ØØ	NUL	ØØ1Ø	ØØØØ	2Ø	SP	Ø1ØØ	ØØØØ	4Ø	@
ØØØØ	ØØØ1	Ø1	SOH	ØØ1Ø	ØØØ1	21	!	Ø1ØØ	ØØØ1	41	A
ØØØØ	ØØ1Ø	Ø2	STX	ØØ1Ø	ØØ1Ø	22	"	Ø1ØØ	ØØ1Ø	42	B
ØØØØ	ØØ11	Ø3	ETX	ØØ1Ø	ØØ11	23	#	Ø1ØØ	ØØ11	43	C
ØØØØ	Ø1ØØ	Ø4	EOT	ØØ1Ø	Ø1ØØ	24	$	Ø1ØØ	Ø1ØØ	44	D
ØØØØ	Ø1Ø1	Ø5	ENQ	ØØ1Ø	Ø1Ø1	25	%	Ø1ØØ	Ø1Ø1	45	E
ØØØØ	Ø11Ø	Ø6	ACK	ØØ1Ø	Ø11Ø	26	&	Ø1ØØ	Ø11Ø	46	F
ØØØØ	Ø111	Ø7	BEL	ØØ1Ø	Ø111	27	'	Ø1ØØ	Ø111	47	G
ØØØØ	1ØØØ	Ø8	BS	ØØ1Ø	1ØØØ	28	(	Ø1ØØ	1ØØØ	48	H
ØØØØ	1ØØ1	Ø9	HT	ØØ1Ø	1ØØ1	29	)	Ø1ØØ	1ØØ1	49	I
ØØØØ	1Ø1Ø	ØA	LF	ØØ1Ø	1Ø1Ø	2A	*	Ø1ØØ	1Ø1Ø	4A	J
ØØØØ	1Ø11	ØB	VT	ØØ1Ø	1Ø11	2B	+	Ø1ØØ	1Ø11	4B	K
ØØØØ	11ØØ	ØC	FF	ØØ1Ø	11ØØ	2C	,	Ø1ØØ	11ØØ	4C	L
ØØØØ	11Ø1	ØD	CR	ØØ1Ø	11Ø1	2D	–	Ø1ØØ	11Ø1	4D	M
ØØØØ	111Ø	ØE	SO	ØØ1Ø	111Ø	2E	.	Ø1ØØ	111Ø	4E	N
ØØØØ	1111	ØF	SI	ØØ1Ø	1111	2F	/	Ø1ØØ	1111	4F	O
ØØØ1	ØØØØ	1Ø	DLE	ØØ11	ØØØØ	3Ø	Ø	Ø1Ø1	ØØØØ	5Ø	P
ØØØ1	ØØØ1	11	DC1	ØØ11	ØØØ1	31	1	Ø1Ø1	ØØØ1	51	Q
ØØØ1	ØØ1Ø	12	DC2	ØØ11	ØØ1Ø	32	2	Ø1Ø1	ØØ1Ø	52	R
ØØØ1	ØØ11	13	DC3	ØØ11	ØØ11	33	3	Ø1Ø1	ØØ11	53	S
ØØØ1	Ø1ØØ	14	DC4	ØØ11	Ø1ØØ	34	4	Ø1Ø1	Ø1ØØ	54	T
ØØØ1	Ø1Ø1	15	NAK	ØØ11	Ø1Ø1	35	5	Ø1Ø1	Ø1Ø1	55	U
ØØØ1	Ø11Ø	16	SYN	ØØ11	Ø11Ø	36	6	Ø1Ø1	Ø11Ø	56	V
ØØØ1	Ø111	17	ETB	ØØ11	Ø111	37	7	Ø1Ø1	Ø111	57	W
ØØØ1	1ØØØ	18	CAN	ØØ11	1ØØØ	38	8	Ø1Ø1	1ØØØ	58	X
ØØØ1	1ØØ1	19	EM	ØØ11	1ØØ1	39	9	Ø1Ø1	1ØØ1	59	Y
ØØØ1	1Ø1Ø	1A	SUB	ØØ11	1Ø1Ø	3A	:	Ø1Ø1	1Ø1Ø	5A	Z
ØØØ1	1Ø11	1B	ESC	ØØ11	1Ø11	3B	;	Ø1Ø1	1Ø11	5B	[
ØØØ1	11ØØ	1C	FS	ØØ11	11ØØ	3C	<	Ø1Ø1	11ØØ	5C	/
ØØØ1	11Ø1	1D	GS	ØØ11	11Ø1	3D	=	Ø1Ø1	11Ø1	5D	]
ØØØ1	111Ø	1E	RS	ØØ11	111Ø	3E	>	Ø1Ø1	111Ø	5E	∧
ØØØ1	1111	1F	US	ØØ11	1111	3F	?	Ø1Ø1	1111	5F	—

Binary			
MSD LSD		Hex	Char
Ø11Ø	ØØØØ	6Ø	'
Ø11Ø	ØØØ1	61	a
Ø11Ø	ØØ1Ø	62	b
Ø11Ø	ØØ11	63	c
Ø11Ø	Ø1ØØ	64	d
Ø11Ø	Ø1Ø1	65	e
Ø11Ø	Ø11Ø	66	f
Ø11Ø	Ø111	67	g
Ø11Ø	1ØØØ	68	h
Ø11Ø	1ØØ1	69	i
Ø11Ø	1Ø1Ø	6A	j
Ø11Ø	1Ø11	6B	k
Ø11Ø	11ØØ	6C	l
Ø11Ø	11Ø1	6D	m
Ø11Ø	111Ø	6E	n
Ø11Ø	1111	6F	o
Ø111	ØØØØ	7Ø	p
Ø111	ØØØ1	71	q
Ø111	ØØ1Ø	72	r
Ø111	ØØ11	73	s
Ø111	Ø1ØØ	74	t
Ø111	Ø1Ø1	75	u
Ø111	Ø11Ø	76	v
Ø111	Ø111	77	w
Ø111	1ØØØ	78	x
Ø111	1ØØ1	79	y
Ø111	1Ø1Ø	7A	z
Ø111	1Ø11	7B	{
Ø111	11ØØ	7C	
Ø111	11Ø1	7D	}
Ø111	111Ø	7E	~
Ø111	1111	7F	DEL

APPENDIX B

ASCII/Hexadecimal/Decimal Conversion

ASCII	Hex	Dec	ASCII	Hex	Dec	ASCII	Hex	Dec	ASCII	Hex	Dec
NUL	ØØ	Ø	SP	2Ø	32	@	4Ø	64	`	6Ø	96
SOH	Ø1	1	!	21	33	A	41	65	a	61	97
STX	Ø2	2	''	22	34	B	42	66	b	62	98
ETX	Ø3	3	#	23	35	C	43	67	c	63	99
EOT	Ø4	4	$	24	36	D	44	68	d	64	1ØØ
ENQ	Ø5	5	%	25	37	E	45	69	e	65	1Ø1
ACK	Ø6	6	&	26	38	F	46	7Ø	f	66	1Ø2
BEL	Ø7	7	'	27	39	G	47	71	g	67	1Ø3
BS	Ø8	8	(	28	4Ø	H	48	72	h	68	1Ø4
HT	Ø9	9	)	29	41	I	49	73	i	69	1Ø5
LF	ØA	1Ø	*	2A	42	J	4A	74	j	6A	1Ø6
VT	ØB	11	+	2B	43	K	4B	75	k	6B	1Ø7
FF	ØC	12	,	2C	44	L	4C	76	l	6C	1Ø8
CR	ØD	13	–	2D	45	M	4D	77	m	6D	1Ø9
SO	ØE	14	.	2E	46	N	4E	78	n	6E	11Ø
SI	ØF	15	/	2F	47	O	4F	79	o	6F	111
DLE	1Ø	16	Ø	3Ø	48	P	5Ø	8Ø	p	7Ø	112
DC1	11	17	1	31	49	Q	51	81	q	71	113
DC2	12	18	2	32	5Ø	R	52	82	r	72	114
DC3	13	19	3	33	51	S	53	83	s	73	115
DC4	14	2Ø	4	34	52	T	54	84	t	74	116
NAK	15	21	5	35	53	U	55	85	u	75	117
SYN	16	22	6	36	54	V	56	86	v	76	118
ETB	17	23	7	37	55	W	57	87	w	77	119
CAN	18	24	8	38	56	X	58	88	x	78	12Ø
EM	19	25	9	39	57	Y	59	89	y	79	121
SUB	1A	26	:	3A	58	Z	5A	9Ø	z	7A	122
ESC	1B	27	;	3B	59	[	5B	91	{	7B	123
FS	1C	28	<	3C	6Ø	\	5C	92	|	7C	124
GS	1D	29	=	3D	61	]	5D	93	}	7D	125
RS	1E	3Ø	>	3E	62	^	5E	94	~	7E	126
US	1F	31	?	3F	63	–	5F	95	DEL	7F	127

Special Character Codes

Code	Explanation	Code	Explanation
ACK	Acknowledge	FF	Form Feed
BEL	Bell or Alarm	FS	File Separator
BS	Backspace	GS	Group Separator
CAN	Cancel	HT	Horizontal Tabulation
CR	Carriage Return	LF	Line Feed
DC1	Device Control 1	NAK	Negative Acknowledge
DC2	Device Control 2	NUL	Null
DC3	Device Control 3	RS	Record Separator
DC4	Device Control 4	SI	Shift In
DEL	Delete	SO	Shift Out
DLE	Data Link Escape	SOH	Start of Heading
EM	End of Medium	SP	Space
ENQ	Enquiry	STX	Start of Text
EOT	End of Transmission	SUB	Substitute
ESC	Escape	SYN	Synchronous Idle
ETB	End of Transmission Block	US	Unit Separator
ETX	End of Text	VT	Vertical Tabulation

APPENDIX C
Quick Reference to Z80 Instruction Set

SINGLE BYTE (8 BIT) LOAD GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS S	Z	H	P/V	N	C	NO. OF BYTES	TIMING M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
LD r,r^1	Dependent on value of r(Bits 5,4,3) and r^1(Bits 2,1,0)		N	N	N	N	N	N	1	1	4	2	r and r^1 represent Registers A,B, C,D,E,H or L.	
	01 ← r →← r^1 →													
	(Binary)												r and r^1 Bit Pattern is:	
													A = 111	189
													B = 000	189
													C = 001	189
													D = 010	189
													E = 011	189
													H = 100	189
													L = 101	189
LD r, n			N	N	N	N	N	N	2	2	7	3.5		
r = A	3E n	062 n												188
r = B	06 n	006 n												188
r = C	0E n	014 n												188
r = D	16 n	022 n												188
r = E	1E n	030 n												188
r = H	26 n	038 n												188

SINGLE BYTE (8 BIT) LOAD GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
r = L	2E n	046 n												188
LD r, (HL)			N	N	N	N	N	N	1	2	7	3.5		
r = A	7E	126												191
r = B	46	070												191
r = C	4E	078												191
r = D	56	086												191
r = E	5E	094												191
r = H	66	102												191
r = L	6E	110												191
LD r, (IX + d)			N	N	N	N	N	N	3	5	19	9.5		
r = A	DD 7E d	221 126 d												193
r = B	DD 46 d	221 070 d												193
r = C	DD 4E d	221 078 d												193
r = D	DD 56 d	221 086 d												193
r = E	DD 5E d	221 094 d												193
r = H	DD 66 d	221 102 d												193
r = L	DD 6E d	221 110 d												193
LD r, (IY + d)			N	N	N	N	N	N	3	5	19	9.5		
r = A	FD 7E d	253 126 d												193
r = B	FD 46 d	253 070 d												193
r = C	FD 4E d	253 078 d												193
r = D	FD 56 d	253 086 d												193
r = E	FD 5E d	253 094 d												193
r = H	FD 66 d	253 102 d												193
r = L	FD 6E d	253 110 d												193
LD (HL), r			N	N	N	N	N	N	1	2	7	3.5		
r = A	77	119												212

SINGLE BYTE (8 BIT) LOAD GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
r = B	70	112												212
r = C	71	113												212
r = D	72	114												212
r = E	73	115												212
r = H	74	116												212
r = L	75	117												212
LD (IX + d), r			N	N	N	N	N	N	3	5	19	9.5		
r = A	DD 77 d	221 119 d												215
r = B	DD 70 d	221 112 d												215
r = C	DD 71 d	221 113 d												215
r = D	DD 72 d	221 114 d												215
r = E	DD 73 d	221 115 d												215
r = H	DD 74 d	221 116 d												215
r = L	DD 75 d	221 117 d												215
LD (IY + d), r			N	N	N	N	N	N	3	5	19	9.5		
r = A	FD 77 d	253 119 d												215
r = B	FD 70 d	253 112 d												215
r = C	FD 71 d	253 113 d												215
r = D	FD 72 d	253 114 d												215
r = E	FD 73 d	253 115 d												215
r = H	FD 74 d	253 116 d												215
r = L	FD 75 d	253 117 d												
LD (HL), n	36 n	054 n	N	N	N	N	N	N	2	3	10	5		211
LD (IX + d), n	DD 36 d n	221 054 d n	N	N	N	N	N	N	4	5	19	9.5		214
LD (IY + d), n	FD 36 d n	253 054 d n	N	N	N	N	N	N	4	5	19	9.5		214
LD A, (BC)	0A	010	N	N	N	N	N	N	1	2	7	3.5		186
LD A, (DE)	1A	026	N	N	N	N	N	N	1	2	7	3.5		187

SINGLE BYTE (8 BIT) LOAD GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
LD A, (nn)	3A n n	050 n n	N	N	N	N	N	N	3	4	13	6.5		185
LD (BC), A	02	002	N	N	N	N	N	N	1	2	7	3.5		210
LD (DE), A	12	018	N	N	N	N	N	N	1	2	7	3.5		210
LD (nn), A	32 n n	050 n n	N	N	N	N	N	N	3	4	13	6.5		205
LD A, I	ED 57	237 087	*	*	Ø	IFF	Ø	N	2	2	9	4.5		183
LD A, R	ED 5F	237 095	*	*	Ø	IFF	Ø	N	2	2	9	4.5		184
LD I, A	ED 47	237 071	N	N	N	N	N	N	2	2	9	4.5		195
LD R, A	ED 4F	237 079	N	N	N	N	N	N	2	2	9	4.5		196

FLAG KEY: N – Not affected.
Ø – RESET = Ø.
1 – SET = 1.
? – Unknown.
* – Affected according to the result.
IFF – Content of Interrupt Flip Flop 2 copied into flag.

TWO BYTE (16 BYTE) LOAD GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
LD, dd, nn			N	N	N	N	N	N	3	3	10	5		
dd = BC	01 nn	001												197
dd = DE	11 nn	017												197
dd = HL	21 nn	033												197
dd = SP	31	049												197
LD IX, nn	DD 21 n n	221 033 n n	N	N	N	N	N	N	4	4	14	7		198
LD IY, nn	FD 21 n n	253 033 n n	N	N	N	N	N	N	4	4	14	7		198
LD dd, (nn)			N	N	N	N	N	N	4	6	20	10		
dd = BC	ED 4B nn	237 075												199
dd = DE	ED 5B nn	237 091												199
dd = HL	ED 6B nn	237 107												199
dd = SP	ED 7B nn	237 123												199
LD IX (nn)	DD 2A n n	221 042 n n	N	N	N	N	N	N	4	6	20	10		201
LD IY, (nn)	FD 2A n n	253 042 n n	N	N	N	N	N	N	4	6	20	10		201
LD (nn), dd			N	N	N	N	N	N	4	6	20	10		
dd = BC	ED 43 n n	237 067 n n												206
dd = DE	ED 53 n n	237 083n n												206
dd = HL	ED 63 n n	237 099 n n												206
dd = SP	ED 73 n n	237 115 n n												206
LD (nn), IX	DD 22 n n	221 034 n n	N	N	N	N	N	N	4	6	20	10		208
LD (nn), IY	FD 22 n n	253 034 n n	N	N	N	N	N	N	4	6	20	10		208
LD SP, HL	F9	249	N	N	N	N	N	N	1	1	6	3		203
LD, SP, IX	DD F9	221 249	N	N	N	N	N	N	2	2	10	5		204

TWO BYTE (16 BYTE) LOAD GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
LD SP, IY	FD F9	253 249	N	N	N	N	N	N	2	2	10	5		204
PUSH rr			N	N	N	N	N	N	1	3	11	5.5		
rr = AF	F5	245												246
rr = BC	C5	197												246
rr = DE	D5	213												246
rr = HL	E5	229												246
PUSH IX	DD E5	221 229	N	N	N	N	N	N	2	4	15	7.5		248
PUSH IY	FD E5	253 229	N	N	N	N	N	N	2	4	15	7.5		248
POP rr			N	N	N	N	N	N	1	3	10	5		
rr = AF	F1	241												242
rr = BC	C1	193												242
rr = DE	D1	209												242
rr = HL	E1	225												242
POP IX	DD E1	221 225	N	N	N	N	N	N	2	4	14	7		244
POP IY	FD E1	253 225	N	N	N	N	N	N	2	4	14	7		244

FLAG KEY:		
	N	– Not affected.
	Ø	– Reset = Ø.
	1	– Set = 1.
	?	– Unknown.
	*	– Affected according to the result.
	IFF	– Content of Interrupt Flip Flop copied into flag.

EXCHANGE, BLOCK TRANSFER AND SEARCH GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
EX DE, HL	EB	235	N	N	N	N	N	N	1	1	4	2		149
EX AF, AF¹	08	008	N	N	N	N	N	N	1	1	4	2		148
EXX	D9	217	N	N	N	N	N	N	1	1	4	2		154
EX (SP), HL	E3	227	N	N	N	N	N	N	1	5	19	9.5		150
EX (SP), IX	DD E3	221 227	N	N	N	N	N	N	2	6	23	11.5		152
EX (SP), IY	FD E3	253 227	N	N	N	N	N	N	2	6	23	11.5		152
LDD	ED A8	237 168	N	N	Ø	*	Ø	N	2	4	16	8		217
LDDR	ED B8	237 184	N	N	Ø	Ø	Ø	N	2	5	21	11.5	If BC ≠ Ø	219
										4	16	8	If BC = Ø	
LDI	ED A0	237 160	N	N	Ø	*	Ø	N	2	4	16	8		221
LDIR	ED B0	237 176	N	N	Ø	Ø	Ø	N	2	5	21	11.5	If BC ≠ Ø	223
										4	16	8	If BC = Ø	
CPD	ED A9	237 169	*	*	*	*	1	N	2	4	16	8		129
CPDR	ED B9	237 185	*	*	*	*	1	N	2	5	21	10.5	If BC ≠ Ø and A ≠ (HL)	130
										4	16	8	If BC = Ø or A = (HL)	
CPI	ED A1	237 161	*	*	*	*	1	N	2	4	16	8		132
CPIR	ED B1	237 177	*	*	*	*	1	N	2	5	21	10.5	If BC ≠ Ø and A ≠ (HL)	133
										4	16	8	If BC = Ø or A = (HL)	

FLAG KEY:	N	– Not affected.	1	– SET = 1.	*	– Affected according to the result.
	Ø	– RESET = Ø.	?	– Unknown.	IFF	– Content of Interrupt Flip Flop copied into flag.

SINGLE BYTE (8 BIT) ARITHMETIC GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
ADC A, n	CE n	206	*	*	*	V	Ø	*	2	2	7	3.5	Adds with Carry	71
ADC A, r			*	*	*	V	Ø	*	1	1	4	2	Adds with Carry	
r = A	8F	143												73
r = B	88	136												74
r = C	89	137												74
r = D	8A	138												74
r = E	8B	139												74
r = H	8C	140												74
r = L	8D	141												74
ADC A, (HL)	8E	142	*	*	*	V	Ø	*	1	2	7	3.5		76
ADC A, (IX + d)	DD 8E d	221 142 d	*	*	*	V	Ø	*	3	5	19	9.5		78
ADC A, (IY + d)	FD 8E d	253 142 d	*	*	*	V	Ø	*	3	5	19	9.5		78
ADD A, n	C6 n	198 n	*	*	*	V	Ø	*	2	2	7	3.5		82
ADD A, r			*	*	*	V	Ø	*	1	1	4	2		
r = A	87	135												83
r = B	80	128												83
r = C	81	129												83
r = D	82	130												83
r = E	83	131												83
r = H	84	132												83
r = L	85	133												83
ADD A, (HL)	86	134	*	*	*	V	Ø	*	1	2	7	3.5		85
ADD A, (IX + d)	DD 86 d	221 134 d	*	*	*	V	Ø	*	3	5	19	9.5		86
ADD A, (IY + D)	FD 86 D	253 134 D	*	*	*	V	Ø	*	3	5	19	9.5		86
DEC d														

SINGLE BYTE (8 BIT) ARITHMETIC GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
d = A	3D	061							1	1	4	2		138
d = B	05	005							1	1	4	2		138
d = C	OD	013							1	1	4	2		138
d = D	15	021							1	1	4	2		138
d = E	1D	029							1	1	4	2		138
d = H	25	037							1	1	4	2		138
d = L	2D	045							1	1	4	2		138
DEC (HL)	35	053	*	*	*	V	I	N	1	3	11	5.5		140
DEC (IX + d)	DD 35 d	221 053 d	*	*	*	V	I	N	3	6	23	11.5		141
DEC (IY + d)	FD 35 d	253 053 d	*	*	*	V	I	N	3	6	23	11.5		141
INC r			*	*	*	V	Ø	N	1	1	4	2		
r = A	3C	060												162
r = B	04	004												162
r = C	0C	012												162
r = D	14	020												162
r = E	1C	028												162
r = H	24	036												162
r = L	2C	044												162
INC (HL)	34	052	*	*	*	V	Ø	N	1	3	11	5.5		165
INC (IX + d)	DD 34 d	221 052 d	*	*	*	V	Ø	N	3	6	23	11.5		166
INC (IY + d)	FD 34 d	253 052 d	*	*	*	V	Ø	N	3	6	23	11.5		166
SBC A, n	DE n	222 n	*	*	*	V	1	*	2	2	7	3.5	Subtract with Carry	301
SBC A, r			*	*	*	V	1	*	1	1	4	2	Subtract with Carry	
r = A	9F	159												302

SINGLE BYTE (8 BIT) ARITHMETIC GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
r = B	98	152												303
r = C	99	153												303
r = D	9A	154												303
r = E	9B	155												303
r = H	9C	156												303
r = L	9D	157												303
SBC A, (HL)	9E	158	*	*	*	V	1	*	1	2	7	3.5		305
SBC A, (IX + d)	DD 9E d	221 158 d	*	*	*	V	1	*	3	5	19	9.5		307
SBC A, (IY + d)	FD 9E d	253 158 d	*	*	*	V	1	*	3	5	19	9.5		307
SUB n	D6 n	214 n	*	*	*	V	1	*	2	2	7	3.5		334
SUB r			*	*	*	V	1	*	1	1	4	2		
r = A	97	151												336
r = B	90	144												337
r = C	91	145												337
r = D	92	146												337
r = E	93	147												337
r = H	94	148												337
r = L	95	149												337
SUB (HL)	96	150	*	*	*	V	1	*	1	2	7	3.5		339
SUB (IX + d)	DD 96 d	221 150 d	*	*	*	V	1	*	3	5	19	9.5		341
SUB (IY + d)	FD 96 d	253 150 d	*	*	*	V	1	*	3	5	19	9.5		341

FLAG KEY:

N	– Not affected	1	– SET = 1
P	– Contains the Parity of the result (1 = Parity Even)	?	– Unknown
V	– Contains the Overflow of the result (1 = Overflow)	*	– Affected according to the result
Ø	– RESET = Ø	IFF	– Content of Interrupt Flip Flop copied into flag.

TWO BYTE (16 BIT) ARITHMETIC GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
ADC HL, ss			*	*	*	*	0	*	2	4	15	7.5		
ss = BC	ED 4A	237 74												80
ss ≐ DE	ED 5A	237 90												80
ss = HL	ED 6A	237 106												80
ss = SP	ED 7A	237 122												80
SBC HL, ss			*	*	*	*	1	*	2	4	15	7.5		
ss = BC	ED 42	237 66												309
ss = DE	ED 52	237 82												309
ss = HL	ED 62	237 98												309
ss = SP	ED 72	237 114												309
ADD HL, ss			N	N	*	N	Ø	*	1	3	11	5.5		
ss = BC	09	009												88
ss = DE	19	025												88
ss = HL	29	041												88
ss = SP	39	057												88
ADD IX,pp			N	N	*	N	Ø	*	2	4	15	7.5		
pp = BC	DD 09	221 009												89
pp = DE	DD 19	221 025												90
pp = IX	DD 29	221 041												91
pp = SP	DD 39	221 057												93
ADD IY, rr			N	N	*	N	Ø	*	2	4	15	7.5		
rr = BC	FD 09	253 009												89
rr = DE	FD 19	253 025												90
rr = IY	FD 29	253 041												92
rr = SP	FD 39	253 057												93

TWO BYTE (16 BIT) ARITHMETIC GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
DEC ss			N	N	N	N	N	N	1	1	6	3		
ss = BC	OB	011												143
ss = DE	IB	027												143
ss = HL	2B	043												143
ss = SP	3B	059												143
DEC IX	DD 2B	221 043	N	N	N	N	N	N	2	2	10	5		144
DEC IY	FD 2B	253 043	N	N	N	N	N	N	2	2	10	5		144
INC ss			N	N	N	N	N	N	1	1	6	3		
ss = BC	03	003												164
ss = DE	13	019												164
ss = HL	23	035												164
ss = SP	33	051												164
INC IX	DD 23	221 035	N	N	N	N	N	N	2	2	10	5		168
INC IY	FD 23	253 035	N	N	N	N	N	N	2	2	10	5		168

FLAG KEY:

FLAG KEY:	N	– Not affected.
	Ø	– Reset = Ø.
	1	– Set = 1.
	?	– Unknown.
	*	– Affected according to the result.

LOGICAL GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
AND n	E6 n	230 n	*	*	1	P	Ø	Ø	2	2	7	3.5		94
AND r			*	*	1	P	Ø	Ø	1	1	4	2		
r = A	A7	167												95
r = B	AO	160												95
r = C	A1	161												95
r = D	A2	162												95
r = E	A3	163												95
r = H	A4	164												95
r = L	A5	165												95
AND (HL)	A6	166	*	*	1	P	Ø	Ø	1	2	7	3.5		98
AND (IX + d)	DD A6 d	221 166 d	*	*	1	P	Ø	Ø	3	5	19	9.5		99
AND (IY + d)	FD A6 d	253 166 d	*	*	1	P	Ø	Ø	3	5	19	9.5		99
CP n	FE n	n	*	*	*	V	1	*	2	2	7	3.5		122
CP r			*	*	*	V	1	*	1	1	4	2		
r = A	BF	181												123
r = B	B8	184												124
r = C	B9	185												124
r = D	BA	186												124
r = E	BB	187												124
r = H	BC	188												124
r = L	BD	189												124
CP (HL)	BE	190	*	*	*	V	1	*	1	2	7	3.5		126
CP (IX + d)	DD BE d	221 190 d	*	*	*	V	1	*	3	5	19	9.5		127
CP (IY + d)	FD BE d	253 190 d	*	*	*	V	1	*	3	5	19	9.5		127

LOGICAL GROUP TABLE (cont.)

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
OR n	F6 n	246 n	*	*	1	P	Ø	Ø	2	2	7	3.5		227
OR r			*	*	1	P	Ø	Ø	1	1	4	2		
r = A	B7	183												229
r = B	BO	176												229
r = C	B1	177												229
r = D	B2	178												229
r = E	B3	179												229
r = H	B4	180												229
r = L	B5	181												229
OR (HL)	B6	182	*	*	1	P	Ø	Ø	1	2	7	3.5		231
OR (IX + d)	DD B6 d	221 182 d	*	*	1	P	Ø	Ø	3	5	19	9.5		233
OR (IY + d)	FD B6 d	253 182 d	*	*	1	P	Ø	Ø	3	5	19	9.5		233
XOR n	EE n	238 n	*	*	1	P	Ø	Ø	2	2	7	3.5		343
XOR r			*	*	1	P	Ø	Ø	1	1	4	2		
r = A	AF	175												345
r = B	A8	168												347
r = C	A9	169												347
r = D	AA	170												347
r = E	AB	171												347
r = H	AC	172												347
r = L	AD	173												347
XOR (HL)	AE	174	*	*	1	P	Ø	Ø	1	2	7	3.5		349
XOR (IX + d)	DD AE d	221 174 d	*	*	1	P	Ø	Ø	3	5	19	9.5		351
XOR (IY + d)	FD AE d	253 174 d	*	*	1	P	Ø	Ø	3	5	19	9.5		351

FLAG KEY:					
N	– Not affected.	Ø	– RESET = Ø.	*	- Affected according to the result.
P	– Contains the Parity of the result (1 = Parity Even).	1	– SET = 1.		
V	– Contains the Overflow of the result (1 = Overflow).	?	– Unknown.		

GENERAL PURPOSE ARITHMETIC AND C.P.U. CONTROL GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
CCF	3F	063	N	N	?	N	Ø	*	1	1	4	2		121
CPL	2F	047	N	N	1	N	1	N	1	1	4	2		135
DAA	27	039	*	*	*	P	N	*	1	1	4	2		136
DI	F3	243	N	N	N	N	N	N	1	1	4	2		145
EI	FB	251	N	N	N	N	N	N	1	1	4	2		147
HALT	76	118	N	N	N	N	N	N	1	1	4	2		155
IM Ø	ED 46	237 070	N	N	N	N	N	N	2	2	8	4		156
IM 1	ED 56	237 086	N	N	N	N	N	N	2	2	8	4		157
IM 2	ED 5E	237 094	N	N	N	N	N	N	2	2	8	4		158
NEG	ED 44	237 068	*	*	*	V	1	*	2	2	8	4		225
NOP	00	000	N	N	N	N	N	N	1	1	4	2		226
SCF	37	055	*	*	Ø	*	Ø	1	1	1	4	2		311

FLAG KEY:		
	N	– Not affected.
	P	– Contains the Parity of the result (1 = Parity Even).
	V	– Contains the Overflow of the result (1 = Overflow).
	Ø	– RESET = Ø.
	1	– SET = 1.
	?	– Unknown.
	*	– Affected according to the result.

ROTATE AND SHIFT GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
RL r			*	*	Ø	P	Ø	*	2	2	8	4		
r = A	CB 17	203 023												263
r = B	CB 10	203 016												263
r = C	CB 11	203 017												263
r = D	CB 12	203 018												263
r = E	CB 13	203 019												263
r = H	CB 14	203 020												263
r = L	CB 15	203 021												263
RLA	17	023	N	N	Ø	N	Ø	*	1	1	4	2		269
RL (HL)	CB 16	203 022	*	*	Ø	P	Ø	*	2	4	15	7.5		265
RL (IX + d)	DD CB d 16	221 203 d 022	*	*	Ø	P	Ø	*	4	6	23	11.5		267
RL (IY + d)	FD CB d 16	253 203 d 022	*	*	Ø	P	Ø	*	4	6	23	11.5		267
RLC r			*	*	Ø	P	Ø	*	2	2	8	4		
r = A	CB 07	203 007												271
r = B	CB 00	203 000												271
r = C	CB 01	203 001												271
r = D	CB 02	203 002												271
r = E	CB 03	203 003												271
r = H	CB 04	203 004												271
r = L	CB 05	203 005												271
RLCA	07	07	N	N	0	N	0	*	1	1	4	2		277
RLC (HL)	CB 06	203 006	*	*	Ø	P	Ø	*	2	4	15	7.5		273
RLC (IX + d)	DD CB d 06	221 203 d 006	*	*	Ø	P	Ø	*	4	6	23	11.5		275
RLC (IY + d)	FD CB d 06	253 203 d 006	*	*	Ø	P	Ø	*	4	6	23	11.5		275

ROTATE AND SHIFT GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
RLD	ED 6F	237 111	*	*	Ø	P	Ø	N	2	5	18	9		279
RR r			*	*	Ø	P	Ø	*	2	2	8	4		
r = A	CB 1F	203 031												281
r = B	CB 18	203 024												281
r = C	CB 19	203 025												281
r = D	CB 1A	203 026												281
r = E	CB 1B	203 027												281
r = H	CB 1C	203 028												281
r = L	CB 1D	203 029												281
RRA	1F	31	N	N	0	N	0	*	1	1	4	2		287
RR (HL)	CB 1E	203 030	*	*	Ø	P	Ø	*	2	4	15	7.5		283
RR (IX + d)	DD CB d IE	221 203 d 030	*	*	Ø	P	Ø	*	4	6	23	11.5		285
RR (IY + d)	FD CB d IE	253 203 d 030	*	*	Ø	P	Ø	*	4	6	23	11.5		285
RRC r			*	*	Ø	P	Ø	*	2	2	8	4		
r = A	CB 0F	203 015												289
r = B	CB 08	203 008												289
r = C	CB 09	203 009												289
r = D	CB 0A	203 010												289
r = E	CB 0B	203 011												289
r = H	CB 0C	203 012												289
r = L	CB 0D	203 013												289
RRCA	0F	15	N	N	0	N	0	*	1	1	4	2		295
RRC (HL)	CB 0E	203 014	*	*	Ø	P	Ø	*	2	4	15	7.5		291
RRC (IX + d)	DD CB d 0E	221 203 d 014	*	*	Ø	P	Ø	*	4	6	23	11.5		293
RRC (IY + d)	FD CB d 0E	253 203 d 014	*	*	Ø	P	Ø	*	4	6	23	11.5		293

ROTATE AND SHIFT GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
RRD	ED 67	237 103	*	*	Ø	P	Ø	N	2	5	18	9		297
SLA r			*	*	Ø	P	Ø	*	2	2	8	4		
r = A	CB 27	203 039												316
r = B	CB 20	203 032												316
r = C	CB 21	203 033												316
r = D	CB 22	203 034												316
r = E	CB 23	203 035												316
r = H	CB 24	203 036												316
r = L	CB 25	203 037												316
SLA (HL)	CB 26	203 038	*	*	Ø	P	Ø	*	2	4	15	7.5		318
SLA (IY + d)	FD CB d 26	253 203 d 038	*	*	Ø	P	Ø	*	4	6	23	11.5		
SRA r			*	*	Ø	P	Ø	*	2	2	8	4		
r = A	CB 2F	203 047												322
r = B	CB 28	203 040												322
r = C	CB 29	203 041												322
r = D	CB 2A	203 042												322
r = E	CB 2B	203 043												322
r = H	CB 2C	203 044												322
r = L	CB 2D	203 045												322
SRA (HL)	CB 2E	203 046	*	*	Ø	P	Ø	*	2	4	15	7.5		324
SRA (IX + d)	DD CB d 2E	221 203 d 046	*	*	Ø	P	Ø	*	4	6	23	11.5		326
SRA (IY + d)	FD CB d 2E	253 203 d 046	*	*	Ø	P	Ø	*	4	6	23	11.5		326
SRL r			*	*	Ø	P	Ø	*	2	2	8	4		
r = A	CB 3F	203 063												328
r = B	CB 38	203 056												328
r = C	CB 39	203 057												328

ROTATE AND SHIFT GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
r = D	CB 3A	203 058												328
r = E	CB 3B	203 059												328
r = H	CB 3C	203 060												328
r = L	CB 3D	203 061												328
SRL (HL)	CB 3E	203 062	*	*	Ø	P	Ø	*	2	4	15	7.5		330
SRL (IX + d)	DD CBd 3E	221 203 d 062	*	*	Ø	P	Ø	*	4	6	23	11.5		332
SRL (IY + d)	FD CBld 3E	253 203 d 062	*	*	Ø	P	Ø	*	4	6	23	11.5		332

FLAG KEY:		
	N	– Not affected.
	P	– Contains the Parity of the result (1 = Parity Even).
	V	– Contains the Overflow of the result (1 = Overflow).
	Ø	– RESET = Ø.
	1	– SET = 1.
	?	– Unknown.
	*	– Affected according to the result.

BIT SET, RESET AND TEST (FLAG) GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
BIT b, r			?	*	1	?	Ø	N	2	2	8	4		
r = A, b = Ø	CB 47	203 071												101
b = 1	CB 4F	203 079												101
b = 2	CB 57	203 087												101
b = 3	CB 5F	203 095												101
b = 4	CB 67	203 103												101
b = 5	CB 6F	203 111												101
b = 6	CB 77	203 119												101
b = 7	CB 7F	203 127												101
r = B, b = Ø	CB 40	203 064												101
b = 1	CB 48	203 072												101
b = 2	CB 50	203 080												101
b = 3	CB 58	203 088												101
b = 4	CB 60	203 096												101
b = 5	CB 68	203 104												101
b = 6	CB 70	203 112												101
b = 7	CB 78	203 120												101
r = C, b = Ø	CB 41	203 065												101
b = 1	CB 49	203 073												101
b = 2	CB 51	203 081												101
b = 3	CB 59	203 089												101
b = 4	CB 61	203 097												101
b = 5	CB 69	203 105												101
b = 6	CB 71	203 113												101
b = 7	CB 79	203 121												101
r = D, b = Ø	CB 42	203 066												101
b = 1	CB 4A	203 074												101

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
b = 2	CB 52	203 082												101
b = 3	CB 5A	203 090												101
b = 4	CB 62	203 098												101
b = 5	CB 6A	203 106												101
b = 6	CB 72	203 114												101
b = 7	CB 7A	203 112												101
r = E, b = Ø	CB 43	203 067												101
b = 1	CB 4B	203 075												101
b = 2	CB 53	203 083												101
b = 3	CB 5B	203 091												101
b = 4	CB 63	203 099												101
b = 5	CB 6B	203 107												101
b = 6	CB 73	203 115												101
b = 7	CB 7B	203 123												101
r = H, b = Ø	CB 44	203 068												101
b = 1	CB 4C	203 076												101
b = 2	CB 54	203 084												101
b = 3	CB 5C	203 092												101
b = 4	CB 64	203 100												101
b = 5	CB 6C	203 108												101
b = 6	CB 74	203 116												101
b = 7	CB 7C	203 124												101
r = L, b = Ø	CB 45	203 069												101
b = 1	CB 4D	203 077												101
b = 2	CB 55	203 085												101
b = 3	CB 5D	203 093												101
b = 4	CB 65	203 101												101

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
b = 5	CB 6D	203 109												101
b = 6	CB 75	203 117												101
b = 7	CB 7D	203 125												101
BIT b, (HL)			?	*	1	?	Ø	N	2	3	12	6		
b = Ø	CB 46	203 070												103
b = 1	CB 4E	203 078												103
b = 2	CB 56	203 086												103
b = 3	CB 5E	203 094												103
b = 4	CB 66	203 102												103
b = 5	CB 6E	203 110												103
b = 6	CB 76	203 118												103
b = 7	CB 7E	203 126												103
BIT b, (IX + D)			?	*	1	?	Ø	N	4	5	20	10		
b = Ø	DD CB d 46	221 203 d 070												105
b = 1	DD CB d 4E	221 203 d 078												105
b = 2	DD CB d 56	221 203 d 086												105
b = 3	DD CA d 5E	221 203 d 094												105
b = 4	DD CB d 66	221 203 d 102												105
b = 5	DD CB d 6E	221 203 d 110												105
b = 6	DD CB d 76	221 203 d 118												105
b = 7	DD CB d 7E	221 203 d 126												105
BIT b, (IY + D)			?	*	1	?	Ø	N	4	5	20	10		
b = Ø	FD CB d 46	253 203 d 070												105
b = 1	FD CB d 4E	253 203 d 078												105
b = 2	FD CB d 56	253 203 d 086												105
b = 3	FD CB d 5E	253 203 d 094												105
b = 4	FD CB d 66	253 203 d 102												105

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

			FLAGS							TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	NO. OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
b = 5	FD CB **d** 6E	253 203 **d** 110												105
b = 6	FD CB **d** 76	253 203 **d** 118												105
b = 7	FD CB **d** 7E	253 203 **d** 126												105
RES b, r			N	N	N	N	N	N	2	2	8	4		
r = A, b = Ø	CB 87	203 135												250
b = 1	CB 8F	203 143												250
b = 2	CB 97	203 151												250
b = 3	CB 9F	203 159												250
b = 4	CB A7	203 167												250
b = 5	CB AF	203 175												250
b = 6	CB B	203 183												250
b = 7	CB BF	203 191												250
r = B, b = Ø	CB 80	203 128												250
b = 1	CB 88	203 136												250
b = 2	CB 90	203 144												250
b = 3	CB 98	203 152												250
b = 4	CB AO	203 160												250
b = 5	CB A8	203 168												250
b = 6	CB BO	203 176												250
b = 7	CB B8	203 184												250
r = C, b = Ø	CB 81	203 129												250
b = 1	CB 89	203 137												250
b = 2	CB 91	203 145												250
b = 3	CB 99	203 153												250
b = 4	CB A1	203 161												250
b = 5	CB A9	203 169												250
b = 6	CB B1	203 177												250
b = 7	CB B9	203 185												250

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
r = D, b = Ø	CB 82	203 130												250
b = 1	CB 8A	203 138												250
b = 2	CB 92	203 146												250
b = 3	CB 9A	203 154												250
b = 4	CB A2	203 162												250
b = 5	CB AA	203 170												250
b = 6	CB B2	203 178												250
b = 7	CB BA	203 186												250
r = E, b = Ø	CB 83	203 131												250
b = 1	CB 8B	203 139												250
b = 2	CB 93	203 147												250
b = 3	CB 9B	203 155												250
b = 4	CB A3	203 163												250
b = 5	CB AB	203 171												250
b = 6	CB B3	203 179												250
b = 7	CB BB	203 187												250
r = H, b = Ø	CB 84	203 132												250
b = 1	CB 8C	203 140												250
b = 2	CB 94	203 148												250
b = 3	CB 9C	203 156												250
b = 4	CB A4	203 164												250
b = 5	CB AC	203 172												250
b = 6	CB B4	203 180												250
b = 7	CB BC	203 188												250
r = L, b = Ø	CB 85	203 133												250
b = 1	CB 8D	203 141												250
b = 2	CB 95	203 149												250

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	µSEC @ 2MHZ		
b = 3	CB 9D	203 157												250
b = 4	CB A5	203 165												250
b = 5	CB AD	203 173												250
b = 6	CB B5	203 181												250
b = 7	CB BD	203 189												250
RES b, (HL)			N	N	N	N	N	N	2	4	15	7.5		
b = Ø	CB 86	203 134												251
b = 1	CB 8E	203 142												251
b = 2	CB 96	203 150												251
b = 3	CB 9E	203 158												251
b = 4	CB A6	203 166												251
b = 5	CB AE	203 174												251
b = 6	CB B6	203 182												251
b = 7	CB BE	203 190												251
RES b,(IX+d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	DD CB d 86	221 203 d 134												253
b = 1	DD CB d 8E	221 203 d 142												253
b = 2	DD CB d 96	221 203 d 150												253
b = 3	DD CB d 9E	221 203 d 158												253
b = 4	DD CB d A6	221 203 d 166												253
b = 5	DD CB d AE	221 203 d 174												253
b = 6	DD CB d B6	221 203 d 182												253
b = 7	DD CB d BE	221 203 d 190												253
RES b,(IY+d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	FD CB d 86	253 203 d 134												253
b = 1	FD CB d 8E	253 203 d 142												253
b = 2	FD CB d 96	253 203 d 150												253

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
b = 3	FD CB d 9E	253 203 d 158												253
b = 4	FD CB d A6	253 203 d 166												253
b = 5	FD CB d AE	253 203 d 174												253
b = 6	FD CB d B6	253 203 d 182												253
b = 7	FD CB d BE	253 203 d 190												253
SET b, r			N	N	N	N	N	N	2	2	8	4		
r = A, b = Ø	CB C7	203 199												312
b = 1	CB CF	203 207												312
b = 2	CB D7	203 215												312
b = 3	CB DF	203 223												312
b = 4	CB E7	203 231												312
b = 5	CB EF	203 239												312
b = 6	CB F7	203 247												312
b = 7	CB FF	203 255												312
r = B, b = Ø	CB CO	203 192												312
b = 1	CB C8	203 200												312
b = 2	CB DO	203 208												312
b = 3	CB D8	203 216												312
b = 4	CB EO	203 224												312
b = 5	CB E8	203 232												312
b = 6	CB FO	203 240												312
b = 7	CB F8	203 248												312
r = C, b = Ø	CB C1	203 193												312
b = 1	CB C9	203 201												312
b = 2	CB D1	203 209												312
b = 3	CB D9	203 217												312
b = 4	CB E1	203 225												312

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
b = 5	CB E9	203 233												312
b = 6	CB F1	203 241												312
b = 7	CB F9	203 249												312
r = D, b = Ø	CB C2	203 194												312
b = 1	CB CA	203 202												312
b = 2	CB D2	203210												312
b = 3	CB DA	203 218												312
b = 4	CB E2	203 226												312
b = 5	CB EA	203 234												312
b = 6	CB F2	203 242												312
b = 7	CB FA	203 250												312
r = E, b = Ø	CB C3	203 195												312
b = 1	CB CB	203 203												312
b = 2	CB D3	203 211												312
b = 3	CB DB	203 219												312
b = 4	CB E3	203 227												312
b = 5	CB EB	203 235												312
b = 6	CB F3	203 243												312
b = 7	CB FB	203 251												312
r = H, b = Ø	CB C4	203 196												312
b = 1	CB CC	203 204												312
b = 2	CB D4	203 212												312
b = 3	CB DC	203 220												312
b = 4	CB E4	203 228												312
b = 5	CB EC	203 236												312
b = 6	CB F4	203 244												312
b = 7	CB FC	203 252												312

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
r = L, b = Ø	CB C5	203 197												312
b = 1	CB CD	203 205												312
b = 2	CB D5	203 213												312
b = 3	CB DD	203 221												312
b = 4	CB E5	203 229												312
b = 5	CB ED	203 237												312
b = 6	CB F5	203 245												312
b = 7	CB FD	203 253												312
SET b, (HL)			N	N	N	N	N	N	2	4	15	7.5		
b = Ø	CB C6	203 198												313
b = 1	CB CE	203 206												313
b = 2	CB D6	203 214												313
b = 3	CB DE	203 222												313
b = 4	CB E6	203 230												313
b = 5	CB EE	203 238												313
b = 6	CB F6	203 246												313
b = 7	CB FE	203 254												313
SET b,(IX + d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	DD CB d C6	221 203 d 198												314
b = 1	DD CB d CE	221 203 d 206												314
b = 2	DD CB d D6	221 203 d 214												314
b = 3	DD CB d DE	221 203 d 222												314
b = 4	DD CB d E6	221 203 d 230												314
b = 5	DD CB d EE	221 203 d 238												314
b = 6	DD CB d F6	221 203 d 246												314
b = 7	DD CB d FE	221 203 d 254												314

BIT SET, RESET AND TEST (FLAG) GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
SET b,(IY + d)			N	N	N	N	N	N	4	6	23	11.5		
b = Ø	FD CB d C6	253 203 d 198												314
b = 1	FD CB d CE	253 203 d 206												314
b = 2	FD CB d D6	253 203 d 214												314
b = 3	FD CB d DE	253 203 d 222												314
b = 4	FD CB d E6	253 203 d 230												314
b = 5	FD CB d EE	253 203 d 238												314
b = 6	FD CB d F6	253 203 d 246												314
b = 7	FD CB d FE	253 203 d 254												314

FLAG KEY: N – Not affected.
P – Contains the Parity of the result (1 = Parity Even).
V – Contains the Overflow of the result (1 = Overflow).
Ø – RESET = Ø.
1 – SET = 1.
? – Unknown.
* – Affected according to the result.

JUMP, (SUB-ROUTINE) CALL AND RETURN GROUP TABLE

			FLAGS						NO.	TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
CALL pq	CD pq	205 pq	N	N	N	N	N	N	3	5	17	8.5		109
CALL cc, pq			N	N	N	N	N	N	3	5	17	8.5	If cc is true	
										3	10	5	If cc is false	
cc = NZ	C4 pq	196 pq												117
cc = Z	CC pq	204 pq												116
cc = NC	D4 pq	212 pq												112
cc = C	DC pq	220 pq												111
cc = PO	E4 pq	228 pq												120
cc = PE	EC pq	236 pq												119
cc = P	F4 pq	244 pq												113
cc = M	FC pq	252 pq												115
DJNZ e	10 e-2	16 e-2	N	N	N	N	N	N	2	2	8	4	If Register B = Ø	146
										3	13	6.5	If Register B ≠ Ø	
JP nn	C3 nn	195 nn	N	N	N	N	N	N	3	3	10	5		175
JP cc, pq			N	N	N	N	N	N	3	3	10	5		
cc = NZ	C2 qp	194 qp												178
cc = Z	CA qp	202 qp												178
cc = NC	D2 qp	210 qp												178
cc = C	DA qp	218 qp												178
cc = PO	E2 qp	226 qp												178
cc = PE	EA qp	234 qp												178
cc = P	F2 qp	242 qp												178
cc = M	FA qp	250 qp												178
JP (HL)	E9	233	N	N	N	N	N	N	1	1	4	2		176
JP (IX)	DD E9	221 233	N	N	N	N	N	N	2	2	8	4		177
JP (IY)	FD E9	253 233	N	N	N	N	N	N	2	2	8	4		177
JR e	18 e-2	024 e-2	N	N	N	N	N	N	2	3	12	6		

JUMP, (SUB-ROUTINE) CALL AND RETURN GROUP TABLE (cont.)

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
JR C, e	38 e-2	056 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	180
										2	7	3.5	If condition not met	181
JR NC, e	30 e-2	048 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	
										2	7	3.5	If condition not met	181
JR NZ, e	20 e-2	032 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	
										2	7	3.5	If condition not met	181
JR Z, e	28 e-2	040 e-2	N	N	N	N	N	N	2	3	12	6	If condition is met	
										2	7	3.5	If condition not met	181
RET	C9	201	N	N	N	N	N	N	1	3	10	5		225
RET cc			N	N	N	N	N	N	1	3	11	5.5	If cc is true	
										1	5	2.5	If cc is false	
cc = NZ	C0	192												257
cc = Z	C8	200												257
cc = NC	D0	208												257
cc = C	D8	216												257
cc = PO	E0	224												257
cc = PE	E8	232												257
cc = P	F0	240												257
cc = M	F8	248												257
RET I	ED 4D	237 077	N	N	N	N	N	N	2	4	14	7		259
RET N	ED 45	237 069	N	N	N	N	N	N	2	4	14	7		261
RST P			N	N	N	N	N	N	1	3	11	5.5		
p = 00 (Hex.)	C7	199												299
p = 08 (Hex.)	CF	207												299
p = 10														

JUMP, (SUB-ROUTINE) CALL AND RETURN GROUP TABLE (cont.)

			FLAGS							TIMING				
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	NO. OF BYTES	M CYCLES	T STATES	μSEC @ 2MHZ	COMMENTS	CH.5 REF.
(Hex.)	D7	215												299
p = 18														
(Hex.)	DF	223												299
p = 20														
(Hex.)	E7	231												299
p = 28														
(Hex.)	EF	239												299
p = 30														
(Hex.)	F7	247												299
p = 38														
(Hex.)	FF	255												299

FLAG KEY: N – Not affected.

INPUT AND OUTPUT GROUP TABLE

SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	FLAGS						NO. OF BYTES	TIMING			COMMENTS	CH.5 REF.
			S	Z	H	P/V	N	C		M CYCLES	T STATES	μSEC @ 2MHZ		
IN A, (N)	DB N	219 N	N	N	N	N	N	N	2	3	11	5.5		159
IN r, (C)			*	*	*	P	Ø	N	2	3	12	6		
r = A	ED 78	237 120												160
r = B	ED 40	237 064												160
r = C	ED 48	237 072												160
r = D	ED 50	237 080												160
r = E	ED 58	237 088												160
r = H	ED 60	237 096												160
r = L	ED 68	237 104												160
IND	ED AA	237 170	?	*	?	?	1	N	2	4	16	8		169
INI	ED A2	237 162	?	*	?	?	1	N	2	4	16	8		172
INIR	ED B2	237 172	?	1	?	?	1	N	2	5	21	10.5	If Register B ≠ 0	170
										4	16	8	If Register B = 0	
INDR	ED BA	237 186	?	1	?	?	1	N	2	5	21	10.5	If Register B ≠ Ø	235
										4	16	8	If Register B = Ø	
OTDR	ED BB	237 187	?	1	?	?	1	N	2	5	21	10.5	If Register B ≠ Ø	173
										4	16	8	If Register B = Ø	
OTIR	ED B3	237 179	?	*	?	?	1	N	2	5	21	10.5	If Register B ≠ Ø	236
										4	16	8	If Register B = Ø	
OUT (n), A	D3 n	211 n	N	N	N	N	N	N	2	3	11	5.5		239
OUT (C), r			N	N	N	N	N	N	2	3	12	6		
r = A	ED 79	237 121												238
r = B	ED 41	237 065												238
r = C	ED 49	237 073												238
r = D	ED 51	237 081												238
r = E	ED 59	237 089												238
r = H	ED 61	237 097												238

INPUT AND OUTPUT GROUP TABLE (cont.)

			FLAGS						NO.		TIMING			
SOURCE CODE	OBJECT CODE (HEX)	DECIMAL	S	Z	H	P/V	N	C	OF BYTES	M CYCLES	T STATES	µSEC @ 2MHZ	COMMENTS	CH.5 REF.
r = L	ED 69	237 105												238
OUTD	ED AB	237 171	?	*	?	?	1	N	2	4	16	8		240
OUTI	ED A3	237 163	?	*	?	?	1	N	2	4	16	8		241

FLAG KEY: N – Not affected.
P – Contains the Parity of the result (1 = Parity Even).
V – Contains the Overflow of the result (1 = Overflow).
Ø – RESET = Ø.
1 – SET = 1.
? – Unknown.
* – Affected according to the result.

The Z80 Reference Guide is an essential book for programmers involved in Z80 machine language programming.

The well laid out format of this book will make it clearer for readers to understand the capabilities of the Z80 instruction set.

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